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Interfacial Electrical Properties of Ion-Beam Sputter Deposited Amorphous Carbon on Silicon

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Abstract—**Amorphous, "diamond-like" Carbon films have been deposited on Si substrates, using ion-beam sputtering. The interfacial properties are studied using capacitance and conductance measurements. Data are analyzed using existing theories for interfacial electrical properties. The density of electronic states at the interface, along with corresponding time constants are determined, and the density of interface states is unusually low for an as yet unoptimized**

I. Introduction

AMORPHOUS, "DIAMOND-LIKE" Carbon films have been studied at least since 1971, when Aisenberg and Chabot reported on the successful deposition of such films using an ion-beam technique [1]. Since then amorphous Carbon films, which are hard and semi-transparent (thus the "diamond-like" description), have been deposited using a number of other techniques. Among these are cracking of hydrocarbons in a glow discharge (both dc and RF) [2]-[4], ion-beam sputtering from a Carbon target [5], etc. It is no surprise, then, that the physico-chemical properties of such films comprise a wide range. In general, these Carbon films produced by any technique are characterized by their smooth and hard surface, high electrical resistivity, optical transparency (visible and/or IR, depending on the method of preparation), excellent resistance to corrosive chemicals, high dielectric strength, contollable refractive index, good adhesion to diverse substrate materials, and low thermal expansion. These properties are highly desirable in a number of application, e.g., protective coatings on optical components, AR coatings for solar cells, laser windows in the IR regime, etc. [6]. Most of the available literature therefore deals with the investigation of various deposition techniques and the physico-chemical properties of the resulting deposits.

In their first paper dealing with diamond-like Carbon films (also called i-Carbon), Aisenberg and Chabot [1] reported on the ability of these films to form a barrier against sodium ion migration using a bias-temperature (BT) stress test. They also calculated the interface state density using flat-band voltage shifts of the capacitance. To our knowledge no serious efforts to study interfacial properties of i-Carbon films on Si or any other substrate have been made to date. In this letter, we report on what we believe to be the first results on the electronic properties of the Al/C/Si MIS structure.

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II. Experimental

Wafers of 3-in-diameter P-Si with (111) orientation were used as substrates. Amorphous, "diamond-like" Carbon films were deposited at the NASA Lewis Research Center by ion-beam sputtering from a Carbon target [7]. Wafers were loaded into the diffusion-pumped (10^{-6} mm) deposition chamber and cleaned *in situ* for 60 s with an ion-beam etch. From previous experiments, the SiO_2 etch rates were known to be ≅80 Å per minute, and the oxide thickness was known to be ≅30 Å. Thus the oxide was removed and some etch of the silicon surface took place. Some heating of the surface was evident during etching but the temperature was not measured. Thus slight self-annealing could have taken place during etching. There was no deliberate voltage biasing or heating of the substrate. During deposition the beam current was 55 mA at 1 KV with a beam diameter of 10 cms. The resulting films were pale yellow, shiny smooth, and hard with excellent adhesion to the substrate. These wafers were then diced into 12 by 12-mm pieces for further processing. Some samples were used for Raman, IR absorption, and ellipsometric studies. The physico-chemical properties of the films inferred from these experiments will be described in a future communication [8]. Aluminum dots were evaporated on other samples using a clean ion-pumped vacuum system. Capacitance and conductance measurements were taken on these samples. The frequency range of 100 Hz to 10 MHz was used in all experiments. Measurements below 1 KHz were, however, not very successful due to noise problems. Thickness and refractive index were found using ellipsometry.

III. Theory of Conductance Measurements [9]

The normalized equivalent parallel conductance of a single level interface state characterized by the time constant τ can be written as

$$\frac{G_p}{\omega C_I} = \frac{qD_{it}\omega\tau}{(1+\omega^2\tau^2)C_I}. \tag{1}$$

It is highly unlikely, however, than an insulator–Si interface will introduce a single level in the Si bandgap. It is more likely

TABLE I

Wavelength	n	k	Thickness
6328Å	2.07	-.0.087	1376Å
5640Å	2.05	-0.130	1376Å
3650Å	2.07	-0.346	1376Å

that the induced levels will appear as a continuum distributed over the entire bandgap. In this case one gets

$$\frac{G_p}{\omega C_I} = \frac{qD_{it}}{2\omega\tau C_I} \ln(1 + \omega^2\tau^2). \tag{2}$$

From (1), the maximum value of $G_p/\omega C_I$ occurs at $\omega\tau = 1$, while from (2) it occurs at $\omega\tau = 1.98$. These conditions are used to directly extract interface state time constants from the measured data. In the specific case of the Si-SiO_2 interface, it is well known that the interface states not only form a continuum, but that the time constant dispersion is much greater than is expected on the basis of a simple continuum ((2)) of states. This enhancement is due to random fluctuations of the Si surface potential in the plane of the interface.

IV. Results

The initial estimates of the thickness and refractive index made by a Rudolph Research automatic ellipsometer at 6328 Å were found to be 900 Å and 2.69, respectively. These crude numbers were used as initial estimates in a detailed multiple angle of incidence ellipsometric study to be reported elsewhere [8]. Table I lists results of these measurements on one sample. (n is the index of refraction, k the extinction coefficient.)

The breakdown field is estimated to be $\sim 5 \times 10^5$ V/cm and resistivity around 10^9 Ω·cm.

A typical C-V plot taken at 10 KHz is shown in Fig. 1. In general, C-V plots are characterized by negligible hysteresis, sharp transition (from depletion to accumulation), and small flat-band voltage shifts. There is, however, considerable frequency dispersion in accumulation. A frequency versus maximum capacitance plot is shown in Fig. 2 to illustrate frequency dispersion of capacitance. The density of interface states was determined by curve fitting to (1) and (2). The density of states versus gate bias is shown in Fig. 3. Unfortunately, we cannot precisely relate gate voltage to Si surface potential in these early samples due to charge leakage, which makes it difficult to obtain reasonable quasistatic C-V characteristics. Hence, the graph should be taken as a qualitative feature of results from this (Al/C/Si) system. The charge leakage, however, was not enough to cause any problem in other measurements reported here. The most interesting result of this study is shown in Figs. 4 and 5. These figures indicate that over the entire range of gate bias investigated, the $G_p/\omega C_I$ versus log f data show good fit to theory only if either a) a single time constant or b) a continuum of states is assumed. The curve fitting in these cases is done as follows. The maximum value of $G_p/\omega C_I$ is obtained experimentally at each fixed bias, and the frequency corresponding to this maximum is recorded. These values are

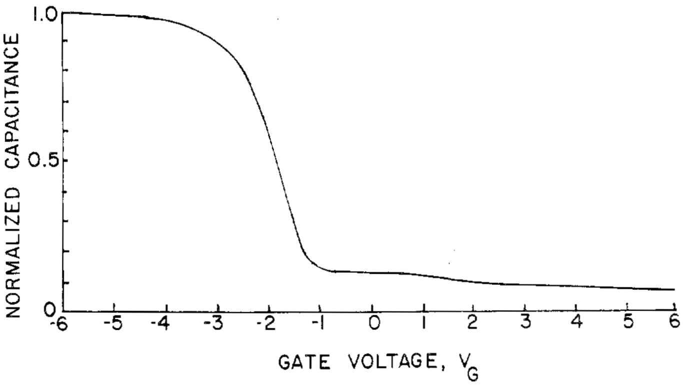

Fig. 1. C-V characteristics of Al/i-C/Si MIS structure at 10 kHz.

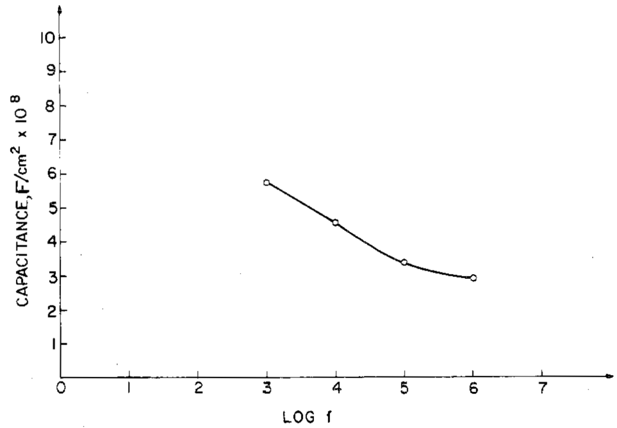

Fig. 2. Frequency dispersion of capacitance in strong accumulation.

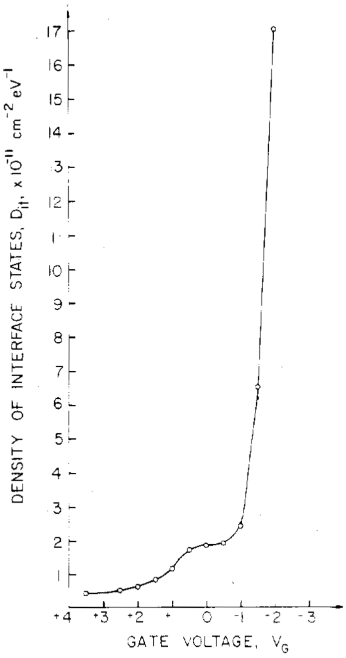

Fig. 3. Density of interface states D_{it} as a function of gate voltage.

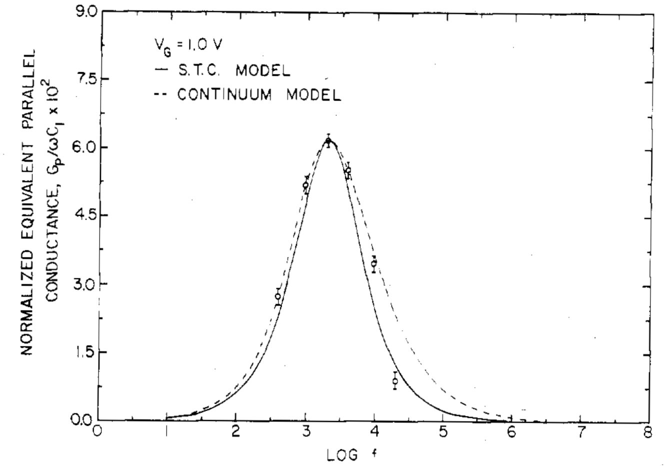

Fig. 4. Normalized equivalent parallel conductance versus log frequency at a gate voltage of 1.0 V.

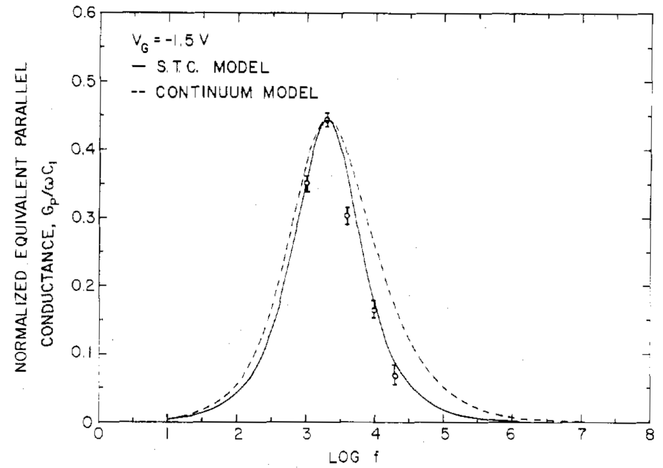

Fig. 5. Normalized equivalent parallel conductance versus log frequency at a gate voltage of -1.5 V.

then substituted into (1) to evaluate D_{it} based on a single time constant model and into (2) to evaluate D_{it} based on a continuum model. These values are then substituted again into (1) and (2), respectively, to generate theoretical $G_p/\omega C_I$ versus $\log f$ plots. It is clear that the experimental data fall on predictions of these two models only. This is surprising in view of the fact that the SiO_2-Si interface exhibits a large time constant dispersion in the depletion region. A single time constant behavior is observed only in the weak inversion region, where it is due to the presence of minority carriers. We have observed the same type (single time constant/continuum) behavior at all other values of the gate bias in the range $-3.5\ V \leqslant V_G \leqslant 3.5$ V, although the fit is not quite as good.

Finally, interface state time constants evaluated from these measurements (using conditions on $\omega\tau$ mentioned above) are plotted as a function of gate bias in Fig. 6. Notice that some of the points are scattered around the straight line. This is due to the fact that the measuring instruments HP4274A and HP4275A measure conductance only at a few discrete values of the frequency. Hence, the exact value at which the conductance peaks at a given value of the gate bias cannot be located with certainty. This also explains the systematic displacements of measured data from the theoretical $G_p/\omega C_I$ versus $\log f$ curves (not shown) at these bias values.

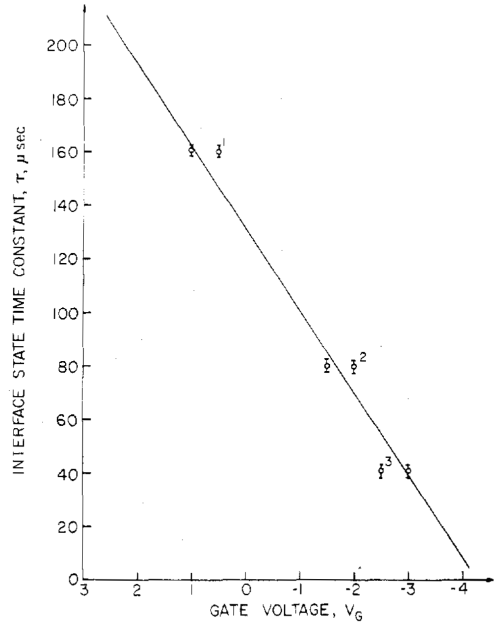

Fig. 6. Interface state time constant τ versus gate voltage. Note the scatter of points due to the inability to sweep the frequency continuously, e.g., points marked 1, 2, and 3 will fall on the line if the peak value of $G_p/\omega C_I$ is assumed to occur at 2.1, 2.2, and 2.9 kHz at these values of the bias.

V. Summary and Conclusions

We have studied the electrical propertties of the i-Carbon/Si interface. We find it very interesting that this interface does not exhibit the large dispersion of interface state time constants commonly associated with the SiO_2/Si interface [9]. Similar behavior (the lack of time constant dispersion) has, however, been reported in other MIS structures [10], [11]. The frequency dispersion in accumulation is disturbing, but its magnitude is much less than is commonly observed in most other MIS structures (except metal/SiO_2/Si) [12]-[14]. It is usually attributed to the classical Maxwell-Wagner effect [15], i.e., to the formation of a highly resistive layer at the interface. In our case, such a layer could have been formed as a result of the surface damage during *in situ* cleaning, although these problems make it doubtful if the conventional equivalent circuit [16] is truly applicable. It is possible that other loss mechanisms (besides interface states, such as tunnelling into insulator states) may also be contributing to the data presented. It is important to notice, however, that the total ac loss is so small that a first-order (continuum of states) calculation yields D_{it} values, which are reasonably low from a device point of view. Since we have only used a few samples so far, the D_{it} can possibly be reduced further by optimization of surface preparation and annealing procedures. Experiments are underway to improve reproducibility, reduce charge leakage problems, and study annealing behavior of these films. We are also investigating dc sputter deposited a-C films on Si. Preliminary results are encouraging.

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