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Computer & Electronics Engineering, Department of

1-1-2007

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Design of a 1.8V 8-bit 500MSPS Folding-Interpolation CMOS A/D Converter with a Folder Averaging Technique

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Abstract − **In this paper, a CMOS analog-to-digital converter (ADC) with an 8-bit 500MSPS at 1.8V is designed. The architecture of the proposed ADC is based on a Folding ADC with a cascaded-folding and a cascaded-interpolation structure. A self-linearized pre-amplifier with source degeneration technique and a folder averaging technique for the high-performance are introduced. Further, a novel auto-switching encoder is also proposed. The chip has been fabricated with 0.18μm 1-poly 5-metal CMOS technology. The active chip area is 0.79mm² and it consumes about 200mW at 1.8V power supply. The DNL and INL are within ±0.6/±0.6LSB, respectively. The measured result of SNDR is 47.05dB.**

I. INTRODUCTION

The demands for analog-digital interface are now being increased, due to the development of SOC (System-On-a Chip) technique. Specially, a high speed and low power A/D Converters (ADC) are key elements in next-generation communication systems. In the field of high speed ADC, full flash type architecture is known to be the most popular one. However, it consumes large chip area and power dissipation, because of many comparators. In order to overcome the drawbacks of the flash type ADC, folding and interpolation techniques are proposed [1]-[5]. The folding-interpolation type ADC has the advantage of small number of comparators and chip area, while the operating speed is same as that of flash type [2]. For that reason, we propose a low power ADC using folding and interpolation technique for UWB system in this paper.

II. ARCHITECTURE

The block diagram of the proposed ADC is shown in Fig. 1. It consists of the pre-processing block, the coarse ADC (3-bit), the fine ADC (5-bit), and the digital signal processing block including a digital error correction. With the principle of folding-interpolation architecture, the MSB 3-bit and the LSB 5-bit are divided into a coarse ADC and a fine ADC, respectively. Further, the fine ADC is composed of the proposed cascaded-folding cascaded-interpolation for a high-speed operation. The pre-processing block is needed to amplify the analog input signal. A proposed self-linearized pre-amplifier with source degeneration technique is adopted for the high-linearity performance in the pre-processing block. Moreover, in the folding block a folding amplifier with averaging folder are described. Also, we introduced a novel auto-switching encoder for the efficient digital processing.
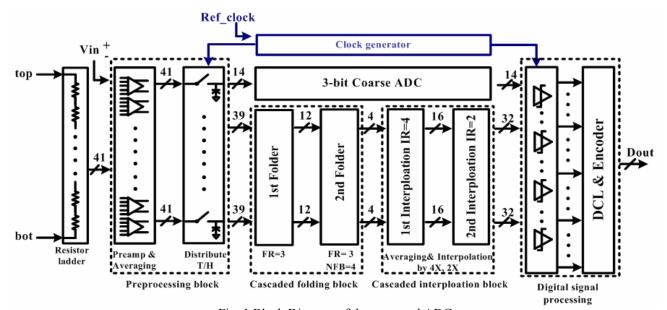

Fig .1 Block Diagram of the proposed ADC

III. CIRCUIT DESIGN

A. Self-Linearized Pre-Amplifier

The linearity of the pre-amplifier [4] is more important than the voltage gain in the pre-processing block. Therefore, a self-linearized pre-amplifier with the source degeneration technique is proposed for the high-linearity performance. As shown in Fig 2 (a), a degeneration resistor is inserted into the source terminal of input MOSFET. Thus, the linearity of input signal is increased by the degeneration function. Due to the principle of degeneration, the voltage of R_s is drop by I_D, when the V_{in} is increasing. Since the gate-source overdrive input voltage is protected at the degeneration resistor R_s, a smoother variation of I_D appears at the output node. Fig. 2 (b) shows the input range of the proposed pre-amplifier with Rs=0 and Rs≠0.

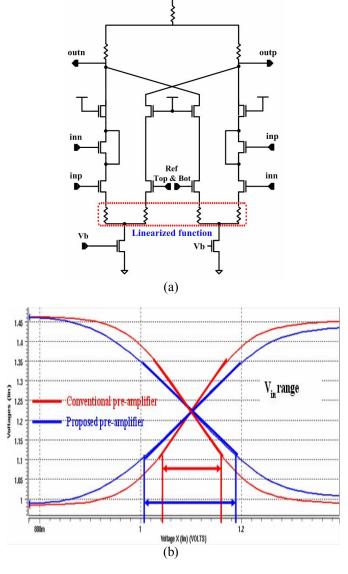### B. Folder Averaging Technique

The distribution of the current at the folding blocks is asymmetrical because of the mismatching problems at the folding input transistors. The asymmetric errors cause the non-linearity errors of the folding signals and decrease the performance of ADC. In conventional ones, a dummy folder is inserted to reduce the mismatching problems for the odd number of the folding amplifiers, as shown in Fig. 3 (a). In this paper, to reduce the non-linearity errors, a folding amplifier with a folder averaging is proposed in Fig. 3 (b). The averaging folder is composed of both the last folder and an inserted folder. Further, two folders are connected by common unit current source. Therefore, the size of the proposed averaging folder is half of the other differential pairs. Since the input of the averaging folder is driven by the over range of the pre-processing block, the current of the folding output is averaged with symmetry. Consequently, the zero-crossing error is reduced and the linearity of the folding signal is improved, compared to the conventional ones. As shown in Fig. 4, the asymmetric errors of the proposed folding signals are significantly decreased by the averaging folders.

(a)

(b)

Fig. 2 Self-Linearized Pre-Amplifier
(a) Circuit Diagram (b) Input Range with R_S=0 and R_S≠0
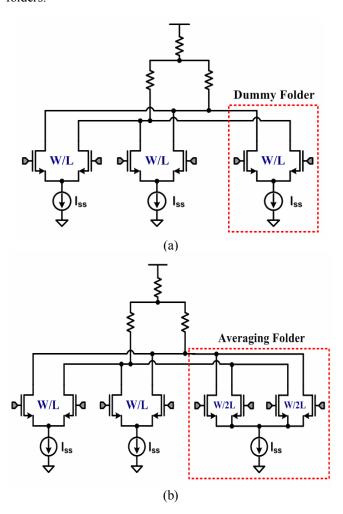

(a)

(b)

Fig. 3 Folder Averaging Circuit
(a) Conventional Dummy Folder in FR=2
(b) Proposed Folder Averaging in FR=2
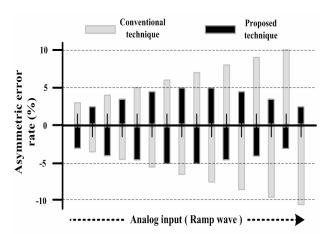
Fig. 4 Asymmetric Error Comparison for Folder Averaging

Fig. 6 Auto-Switching Encoder

C. Auto-Switching Encoder

Conventionally, the output of the folding block has the reverse-thermometer codes in the folding-interpolation ADC. Thus the digital block of the folding-interpolation ADC must include a switching block for the conversion of the reverse-thermometer code. However, it is very complicated and hard to implement. In this paper, a novel auto-switching encoder to convert the reverse-thermometer code into the binary code is proposed. The efficient digital algorithm used in the proposed auto-switching encoder is described in Fig. 5. It is a simple example for an algorithm of 3-bit auto-switching encoder. Initially, the thermometer codes, the outputs of comparator, are converted to "1" at the boundary of "0" and "1" by an XOR gate. As shown in Fig. 6, then, the converted digital code generates the output code through an OR gate. Consequently, the proposed algorithm generates the desired digital output code without any unnecessary switching blocks.

D. Cascaded-Folding Cascaded-Interpolation Structure

In general, 3+5 structure is employed by FR (Folding Rate)=8, NFB(Num. of Folding Block)=4, and IR (Interpolation Rate)=8 in an 8-bit F/I ADC [1][2]. But if 8 of FR and 8 of IR are chosen, the input signal bandwidth is limited by the folding rate [3], and the output of the folding signal has a large load capacitance by the interpolation rate.
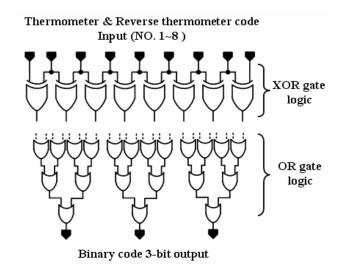
It is a drawback for a high-speed F/I ADC. As a consequence, we proposed cascaded-folding (FR=3x3) cascaded-interpolation (IR=4x2) structure. The proposed cascaded-folding cascaded-interpolation structure has a wide input bandwidth and a small load capacitance, compared to the conventional 3+5 structure (FR=8, IR=8). Thus, the proposed cascaded-folding cascaded-interpolation is appropriate for high-speed operation.

IV. EXPERIMENTAL RESULTS

The proposed folding-interpolation ADC has been fabricated with a 0.18μm 1-poly 5-metal CMOS technology. Fig. 7 shows the layout drawing of the proposed ADC. The active chip area is 0.79 mm^2. Further, the ADC consumes 200mW from 1.8V supply when the clock is 500MHz. As shown in Fig. 8 (a), the measured SNDR is 47.05dB when the input frequency is 30MHz at 300MHz clock frequency. The measured INL and DNL are within 0.6LSB respectively in Fig 8 (b). The experimental results indicate that the proposed folding-interpolation ADC has the desired performance.

Thermometer code (MSB)							Encoder		
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	0	1	0
0	0	0	0	1	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	1	0	0	0	0	1	0	1
0	1	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	1	1	1

Thermometer code							Encoder		
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	0	1	0
0	0	0	0	1	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	1	0	0	0	0	1	0	1
0	1	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	1	1	1

Thermometer code (LSB)							Encoder		
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	0	1	0
0	0	0	0	1	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	1	0	0	0	0	1	0	1
0	1	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	1	1	1

Fig. 5 The Proposed Algorithm Converted the Thermometer Codes into the Binary Codes
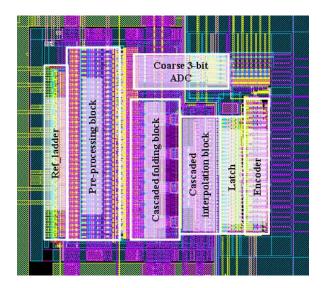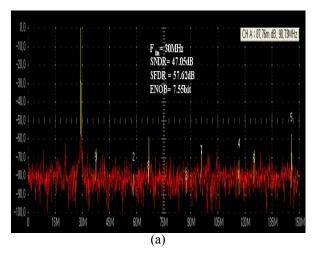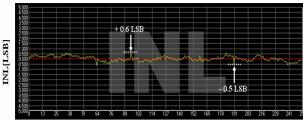
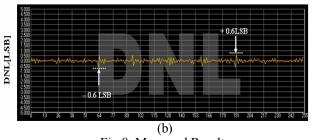Fig. 7 Chip Layout Drawing of the proposed ADC

(a)

(b)

Fig 8. Measured Results
(a) Measured FFT (b) Measured INL&DNL

V. CONCLUSION

A 1.8V 8-bit 500MSPS CMOS ADC has been described. The architecture of the proposed ADC was based on a folding ADC using a cascaded-folding cascaded-interpolation structure. The self-linearized pre-amplifier with source degeneration technique, the folder averaging technique, and an auto-switching encoder were discussed for the desired performance of the ADC. The effective chip area was 0.79mm^2, the ADC consumed 200mW at 1.8V supply. The measured ENOB of the proposed ADC was 7.55bits when the input frequency was 30MHz at 500MSPS. The measured results of the ADC are summarized in Table 1.

Table 1. Measured Results of the proposed ADC

Resolution	8-bit
Sampling Freq.	500MSPS
Power Supply	1.8V (Analog + Digital)
Analog Input Range	Diff. 1Vpp
DNL / INL (Measured Data)	±0.6LSB / ±0.6LSB
ENOB (Measured Data)	7.55bits (Fs=300MHz)
Power	200mW
Core Area	920um × 860um
Process	Samsung 0.18um CMOS

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