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A Small Chip Area 12-b 300MS/s Current Steering CMOS D/A Converter Based on a Laminated-Step Layout Technique

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Abstract- A 12-b 300MSPS Current-Steering DAC with 0.13 μ m CMOS technology is presented. In order to reduce the chip area, a laminated-step layout technique is proposed. Based on this technique, the occupied DAC core size is only 0.26mm² even in 12-b resolution. Further, a current auto-averaging technique, an output impedance enhancement circuit, and the novel latched switching cell logic are discussed to keep the desired 12-b DAC performance. The measured results are within ± 1 LSB for DNL. The measured SFDR is 70dB under Nyquist output frequency with 50mW power dissipation at 3.3V power supply.

I. INTRODUCTION

The demands for analog/digital interface are now being increased, as the development of SOC (System-On-Chip) technique is improved. Specially, a high performance and a low spurious Digital-to-Analog Converter (DAC) have a great role to convert digital data into analog data in the fields of communication systems and other applications. Further, most of the DAC are now fabricated with the technology of CMOS process to satisfy the condition of an Intellectual Property (IP) in a large CMOS SOC.

There exist many kinds of design technique to implement a CMOS DAC such as a decoder based design with an operational amplifier, a two-switch type design, a current steering type design, and so on. However, the most widely used design technique is a current steering type [1]-[8], because it has the capability of driving resistive loads without any special buffers like operational amplifiers and it has the suitability for simple CMOS implementation. Further, it has a high-speed operation and it consumes low power in comparison with other types.

Nowadays, the research trends for current steering DAC are focused on high performance like a small integral non-linearity error (INL) and differential non-linearity error (DNL) [4][5]. Further, a frequency response with a large Spurious Free Dynamic Range (SFDR) is required to satisfy the condition of high-quality video communication systems. In order to implement this requirement, an intrinsic accuracy technique, low deglitching circuits, a self-trimming technique, a matrix cell relocation technique, and many techniques have been presented.

Until now, most of the conventional current steering DAC have adopted two dimensional current cell relocation techniques. Through a symmetrical relocation of the current cells, a lot of non-linearity errors were drastically improved.

Thus a symmetrical current cell relocation technique now becomes an important rule to design a current steering DAC [6][7][8]. However, the chip area is much increased due to the metal routing, even though the chip performance is improved due to the symmetrical cell relocation. The chip area with the symmetrical current cell relocation technique is almost two or three times bigger than the chip area without the symmetrical cell relocation technique.

In this paper, a small chip area current steering DAC without the symmetrical current cell relocation technique is presented. In order to reduce the chip area, a direct metal routing and a non-symmetrical relocation technique are proposed. Further, a laminated-step layout technique to improve the non-linearity errors is described. Based on this technique, a small chip area of 0.26mm² current steering 12-b DAC is obtained, even though a 6+6 full matrix segmented architecture is used.

The contents of the paper are as follows. In section II, the architecture of the current steering 12-b DAC is described. In Section III, circuit design of the proposed block is discussed. The fabrication results and experimental results are described in Section IV. Finally, the conclusions are summarized in Section V.

II. ARCHITECTURE

The architecture and block diagram for the 12-b Current-Steering DAC (CS-DAC) is shown in Figure 1. It is composed of a 6-bit full matrix type MSB and a 6-bit full matrix type LSB to optimize the 12-b full structure. All the digital codes drive the latched switching cell logic through the thermometer type decoder. In the thermometer decoder block, the 12-bit input digital data are divided into 4 groups. Then each 3-bit digital data is converted into 8-bit thermometer digital data. The converted thermometer digital data choose the optimized circuits in the block of the latched switching cell logic. In the block of the latched switching cell logic, the selected cell logic activated by the input digital data drive the analog current cell. Finally, the analog current cells are controlled by the switching signals of digital block. When we design the analog current cells, many dummy matching cells to compensate the mismatching problems have been inserted [1][2]. Namely, a symmetrical current cell relocation technique has been widely used. In Figure 1, however, the LSB current cells are located among MSB current cells. It is not a symmetrical relocation technique. We will discuss it in Section III.

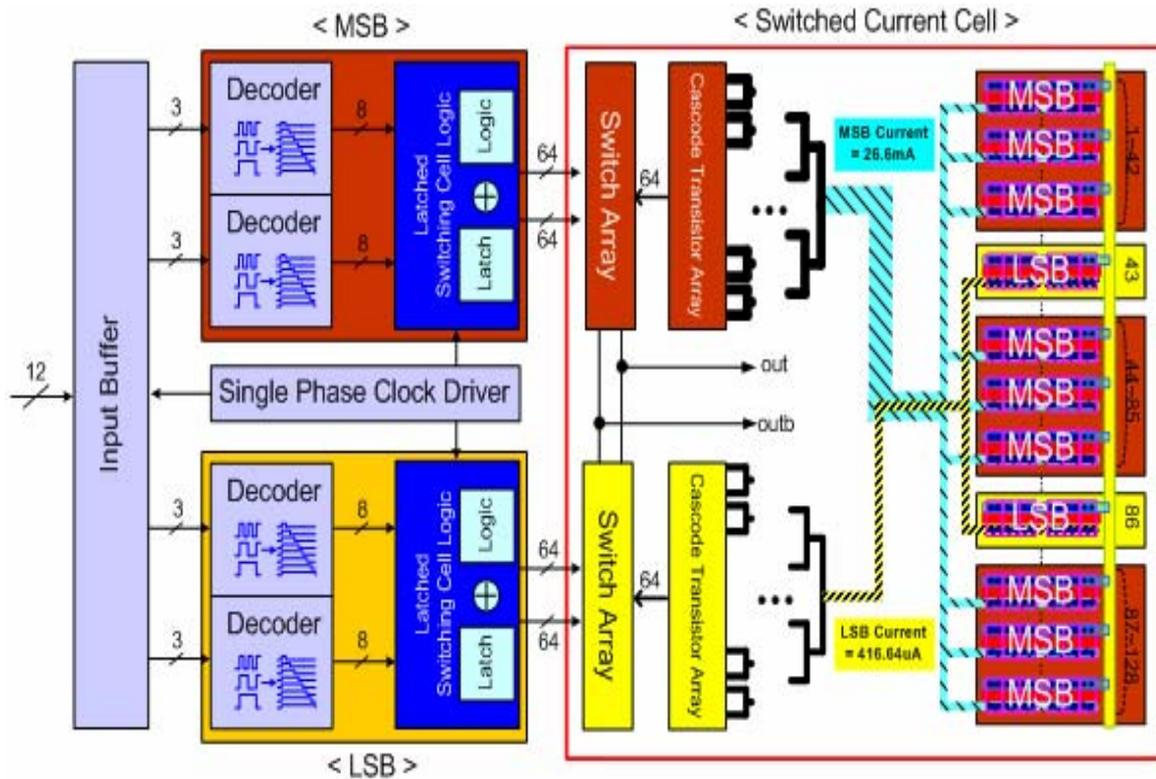


Figure 1 : Block Diagram for the 12-bit Current Steering DAC

III. CIRCUIT DESIGN

A. The proposed Laminated-Step Layout Technique

In order to obtain a compact layout and an improved matching result for analog current cells, a laminated-step layout technique is proposed as shown in Figure 2. All the analog current cells including both MSB block and LSB block are composed of a unit current cell. While the LSB block has a unit cell, the MSB block has 64 unit cells. Since 64 unit cells make a current cell in MSB block, mismatching problems between a LSB current cell and a MSB current cell are serious. The proposed laminated-step layout technique reduces the mismatching problems, because two LSB current cells are located at the end of MSB current cell as shown in Figure 1. Without any dummy matching cells and an intentional symmetrical current cell relocation technique, we can obtain equivalent symmetrical current cells. Therefore, the dynamic performance and the matching characteristics of analog current cell are improved without any dummy matching cells and a symmetrical current cell relocation technique. Further, the LSB current cell is regularly inserted into MSB arrays as an order of switching signal. Thus the layout size is drastically reduced by about 50% smaller than the conventional ones that the MSB and LSB cells are separated by different wells. Finally, a layout floor for auto-averaging current cell is introduced. The layout like a tree structure is proposed to obtain the same parasitic value of resistance and capacitance. The LSB current cells are located in the point of 1/3, 2/3 from the full block of current cell. Therefore, it minimizes the current difference between the block of MSB and the block of LSB. Due to the effects of auto-averaging current cell, the linearity errors are improved.

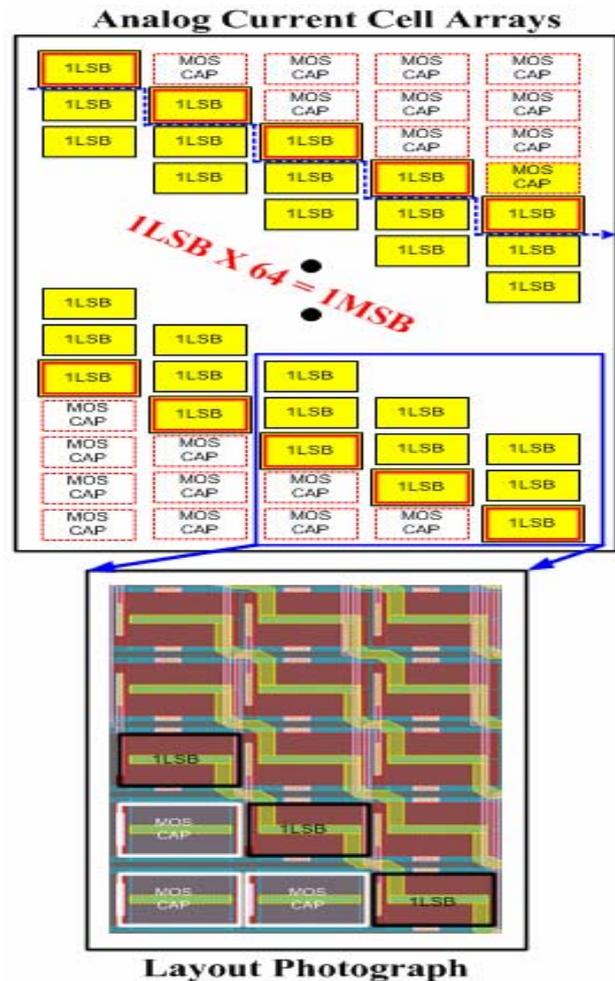


Figure 2 : The proposed Laminated-Step Layout

B. Latched Switching Cell Logic and Current Cell

Conventionally, the latched switching cell logic consists of a separated switching logic, a separated deglitching circuit for high speed operation, and a separated latch. Thus, it occupies large chip area and consumes large power dissipation. To overcome the disadvantages, simple and all-merged switching cell logic is shown in Figure 3. The novel latched switching cell logic has a role of a switching logic, a deglitching circuit, and a latch, simultaneously. The cell logic is designed with the binary decision diagram (BDD) technique and the differential cascode voltage switch logic. The power dissipation and the chip area of digital block are reduced by 50% and 30%, respectively.

In general, the analog current cell of a high-resolution DAC needs a cascode transistor connection for the high output impedance. However, a simple cascode connection is not enough, because the output impedance of more than $300M\Omega$ is necessary to obtain 0.5LSB INL & DNL for 12-bit DAC [3]. Thus a feedback bias structure shown in Figure 3 is presented. The feedback loop is designed with a folded-cascode amplifier and a cascode transistor connection for the high impedance (over $300M\Omega$) of output current cell.

Therefore, the output impedance of the current cells is maintained uniformly, even though the input frequency is increasing. Based on this high output impedance current cell, we can obtain a desired performance for 12-bit 300MSPS DAC.

IV. MEASURED RESULTS

Figure 4 shows the full layout diagram and packaged chip photograph for the 12-bit DAC with 0.13 μ m thick gate CMOS technology. The core size is smaller than 510 μ m x 510 μ m. The size of the MSB digital block is the same as the size of the LSB digital block. The size of the current cell is smaller than that of the digital block, because a laminated-step layout technique is used in the analog block. Figure 5 shows measured results for linearity errors and frequency spectrums. The measured SFDR is about 75dB at 1MHz output frequency when the sampling frequency is 100MSPS. The measured SFDR is above 40dB under Nyquist output frequency when the sampling frequency is 300MSPS. Further, the measured INL is within ± 3 LSB and DNL is within ± 1 LSB.

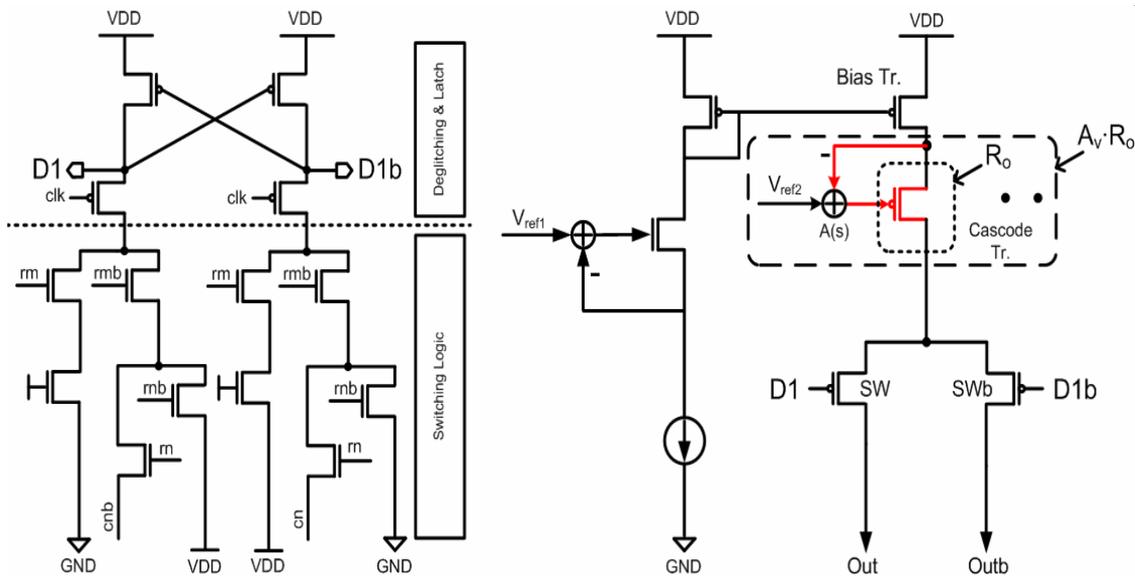


Figure 3 : Circuit Diagram for Latched Switching Cell and 2nd Feedback Bias Current Cell

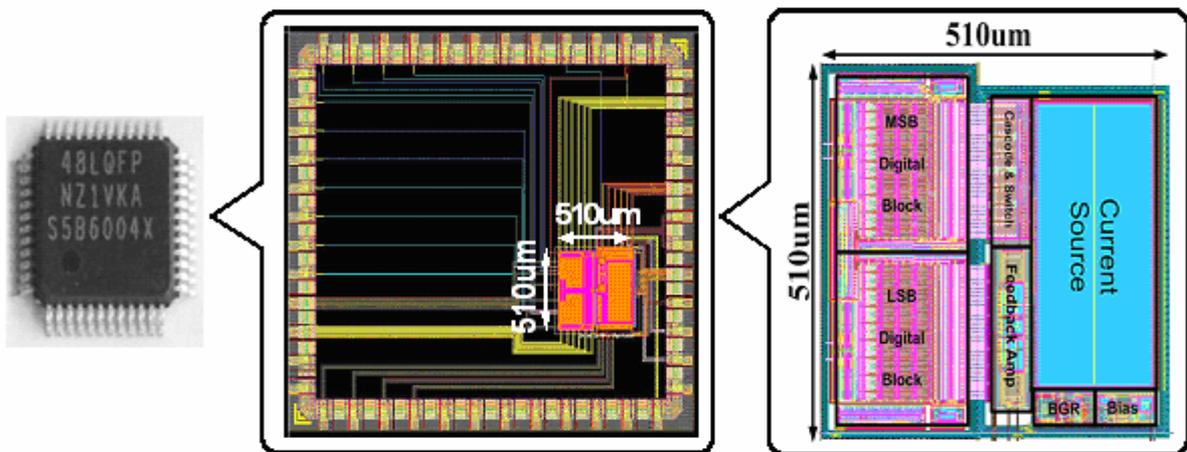


Figure 4 : Packaged Chip Photo and Layout the DAC

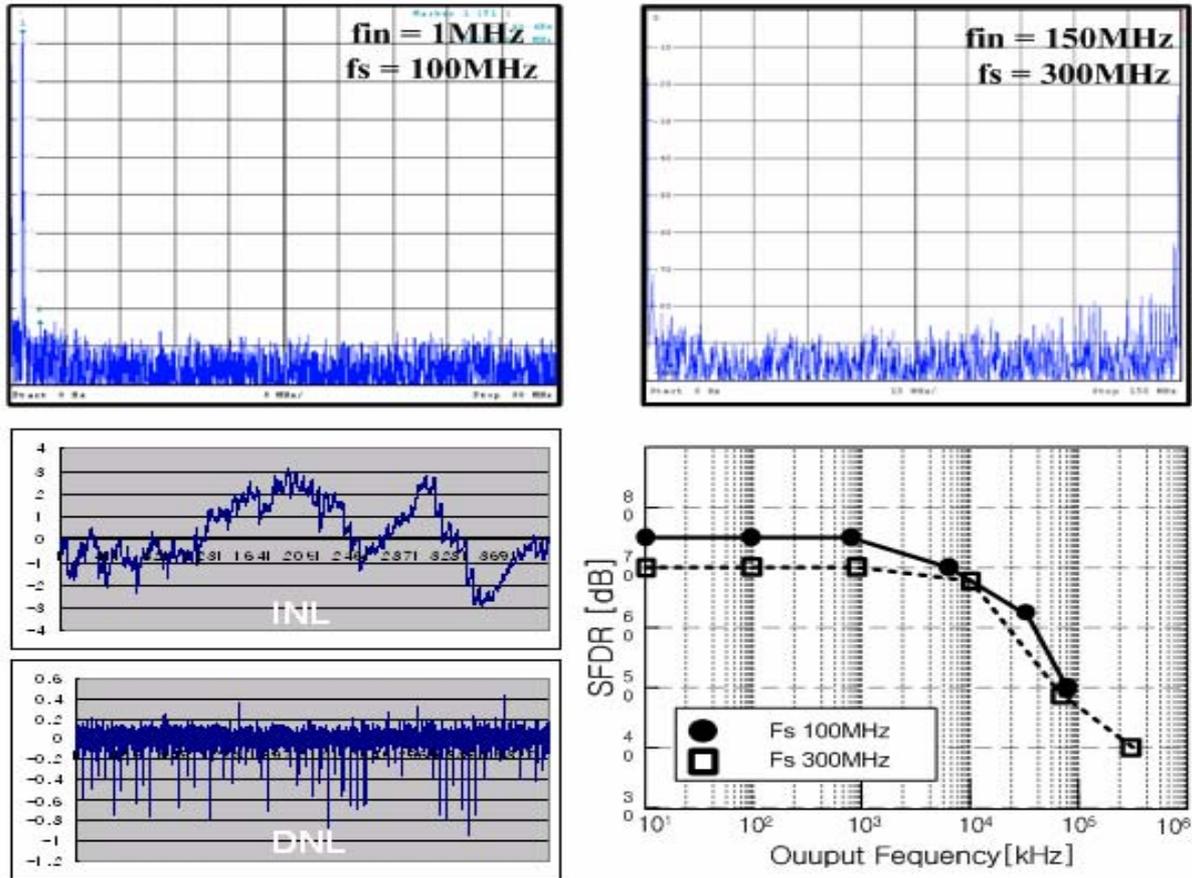


Figure 5 : Measured Results

V. CONCLUSION

A small chip area 12-bit 300MS/s CMOS DAC was discussed. In order to reduce the chip area, a laminated-step layout technique was proposed. Further, all-merged switching cell logic and an improved analog current cell were introduced for low power and well-optimized matching characteristics. The active chip occupied an area of 0.26mm² in 0.13um CMOS technology. The performance of the DAC was summarized in Table 1.

Table 1 : Performance Summary

| | | |
|-------------------|----------------------|------|
| Process | 0.13um CMOS | |
| Resolution | 12-bit | |
| Power Supply | 3.3V | |
| Update Rate | < 300MS/s | |
| INL / DNL | < 3/1 LSB | |
| Power Consumption | 50mW | |
| SFDR (300MS/s) | Fin=1MHz | 75dB |
| | Fin=150MHz | 40dB |
| Chip Area | 0.26 mm ² | |

ACKNOWLEDGEMENT

The authors are thankful for the support from Samsung Electronics Co. Ltd., and the support from Seoul Nano-Cluster Development Center.

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