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Fabrication of Pillar-Structured Thermal Neutron Detectors

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Abstract— Pillar detector is an innovative solid state device structure that leverages advanced semiconductor fabrication technology to produce a device for thermal neutron detection. State-of-the-art thermal neutron detectors have shortcomings in achieving simultaneously high efficiency, low operating voltage while maintaining adequate fieldability performance. By using a 3-dimensional silicon PIN diode pillar array filled with isotopic boron 10, (^{10}B) a high efficiency device is theoretically possible. The fabricated pillar structures reported in this work are composed of 2 μm diameter silicon pillars with a 4 μm pitch and pillar heights of 6 and 12 μm . The pillar detector with a 12 μm height achieved a thermal neutron detection efficiency of 7.3% at 2V.

I. INTRODUCTION

Thermal neutron detection is routinely carried out by utilizing helium 3 (^3He) tubes. Conventional ^3He tube neutron detectors can achieve very high thermal neutron detection efficiency; 2" diameter tube filled with 10 atm ^3He gas can reach greater than 80% detection efficiency. However, due to long term stability problems (gas leakage and build-up of electronegative "poison" in the gas) as well as the inconvenience to replace pure ^3He gas, these tube detectors normally operate at lower pressure setting, thereby reducing their detection efficiency. Furthermore, the use of these proportional counter type devices is encumbered by the required high voltage (1000 V), sensitivity to microphonics, large device footprint, and high tube pressure, all of which result in significant complications for routine deployment and air transport. These operating conditions make ^3He tubes difficult to use in field. To overcome these problems, several solid state thermal neutron detector concepts have been recently developed [1]-[3].

Moving from a gas-based medium to a solid-state medium can dramatically reduce the size of the device because of the increase in the density of the material. Table 1 shows candidate materials that have relatively significant thermal neutron cross-sections, and high-energy charged carrier particles from the reaction. One approach for solid state thermal neutron detection is to coat the thermal neutron converter material on top of a semiconductor material [4], [5],

(see Fig.1). Here, the neutron converter material is ^{10}B which has a very high thermal neutron cross section of 3837 barns. When the thermal neutrons interact with ^{10}B , the energetic charged particles that are produced (alpha and $^7\text{Li}^+$) can then create electron-hole pairs within the semiconductor. From simulations it has been determined that the alpha particles are responsible for the majority of the detectible signal. The detection efficiency of this ^{10}B coated device structure is limited to about 3 to 5 % because the travel range of the as-produced alpha particles is approximately 3 μm in ^{10}B . At the same time the ^{10}B film thickness of approximately 50 μm is needed to absorb the majority of the incoming thermal neutron flux. Fabrications of ^{10}B loaded semiconductors have also been reported using evaporation and powder filling [6]. To date, the ability to fill high aspect ratio structures with ^{10}B remains a challenge.

Building up thicker regions of the converter material is required to achieve high efficiency for the semiconductor thermal neutron detector. One approach involves the use of boron carbide [3]. Another approach utilizes ^6LiF as the neutron converter material [4]. The contradiction in scale lengths (3 μm versus 50 μm) is the hurdle to be overcome for producing high efficiency thermal neutron detectors using ^{10}B as the converter material. This conundrum can be resolved with our three dimensional device coined 'pillar detector.' The fabrication process, electrical characteristics and radiation response of an epitaxially grown silicon p+, intrinsic, n+ (P-I-N) diode pillar detector filled with conformal coated ^{10}B is reported [3].

TABLE I
COMPARISON OF CONVERTER MATERIALS FOR NEUTRON TO CHARGED PARTICLE REACTION

Element	Q value (MeV)	σ_t (b) (thermal neutrons)	State of material	Reaction
Natural Boron	2.78	767	Solid	$^{10}\text{B}(n, \alpha)^7\text{Li}$
Boron 10	2.78	3837	Solid	$^{10}\text{B}(n, \alpha)^7\text{Li}$
Natural boron carbide	2.78	644	Solid	$^{10}\text{B}(n, \alpha)^7\text{Li}$
Boron 10 carbide	2.78	3223	Solid	$^{10}\text{B}(n, \alpha)^7\text{Li}$
Helium 3	0.765	5327	Gas	$^3\text{He}(n, p)^3\text{H}$
Lithium 6	4.78	940	Solid	$^6\text{Li}(n, \alpha)^3\text{H}$
Lithium 6 Fluoride	4.78	940	Solid	$^6\text{Li}(n, \alpha)^3\text{H}$

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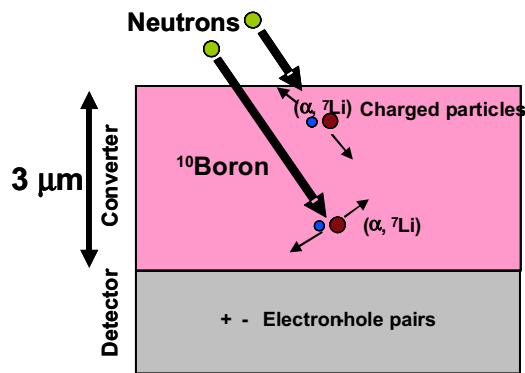


Fig. 1. Planar ^{10}B coated detector.

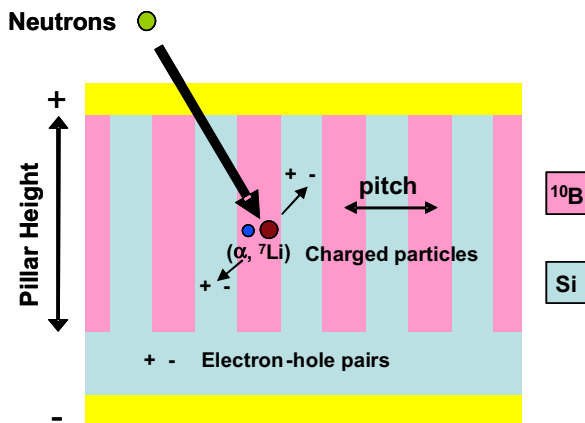


Fig. 2. Three dimensional pillar structured thermal neutron detector.

II. PILLAR DETECTOR DESIGN

The pillar detector consists of etched silicon pillars of P-I-N diodes which are grown on a planar silicon substrate. The neutron-converter (^{10}B) and the detector material (silicon) are inter-digitated (Fig. 2) such that charged particles from the ^{10}B reaction have a high probability of impinging the intrinsic region on the silicon due to the close proximity. Here the thickness of converter material is not fundamentally restricted, since the preponderance of the charged particles is detected by the adjacent pillars. Additionally the geometrical constraints on the ^{10}B thickness are separated by defining the *pillar height* (etch depth) to fully absorb the neutron flux; while the *pillar pitch* is defined lithographically to have the highest possible interaction of the alpha particles with the semiconductor pillar to insure charged carrier generation in the pillars.

Monte Carlo N Particle transport code (MCNP) was used to simulate a near-by neutron point source interaction with the neutron-converter (^{10}B) embedded in the pillar structure, after which the range of the as-produced charged particles was computed by using Ion-Range-In-Matter (IRMA) code (Fig. 3). By utilizing micrometer-size pillar diameters and spacing, the probability of neutron induced charged particles striking the semiconductor detector is simulated to be high when compared to the planar design. By scaling the intrinsic region of the P-I-N diode and thus the pillar height to 100 μm , an efficiency of 90% is predicted for the structure with 2 μm diameter pillars and 4 μm pitch, assuming that all charged

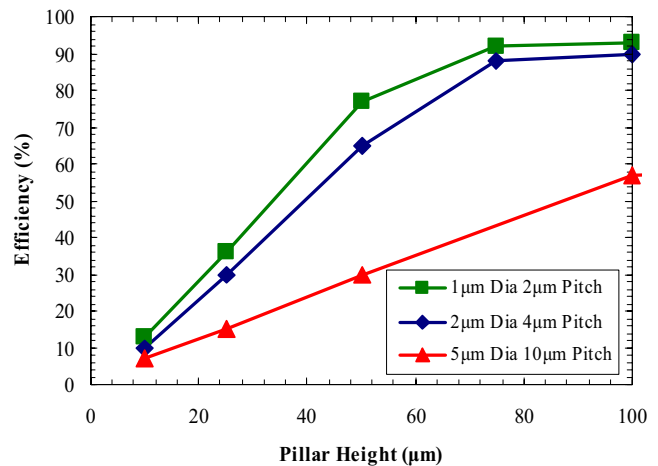


Fig. 3. MCNP and IRMA simulations of thermal neutron capture efficiency versus pillar height for several pillar diameters and pitches.

particles reaching the P-I-N diode with energy greater than 100 keV generate a detectable signal. The geometry of the predicted 90% efficiency device has an aspect ratio of 50:1. Deep trench structures with aspect ratios of up to 100:1 have been demonstrated using similar etching technology and filled with LPCVD polysilicon for MEMS devices [7].

III. FABRICATION

The multi-step fabrication used for the pillar detector is illustrated in Fig. 4. The starting silicon substrates consisted of a P-I-N layer structure grown epitaxially on an n+ silicon substrate. The first two steps involved the pillar definition and pillar etching. Adequate masking materials and vertical etched features with smooth sidewalls were required. Step 1 involved the photolithographic definition of the pillar arrays which have 2 μm diameters and a 4 μm pitch. The epitaxial Si was dry etched by high density plasma to form the pillar structure (Fig. 4, step 2). High density plasma systems were employed to etch such structures because the high density plasma can provide a large ion flux with small ion energy that yields low-damage etching. For example, electron cyclotron resonance (ECR) and inductively coupled plasma (ICP) systems fall into this category. Unlike reactive ion etching (RIE) which has the ion density coupled to the bias voltage, high density plasma etchers have these two parameters uncoupled to enable highly anisotropic etching with smooth features. For the pillar detector the plasma etching was done by a deep RIE system [3] with an ICP plasma source and time-multiplexed “Bosch Process”, which uses SF_6 to etch silicon and C_4F_8 for the passivation step. Afterwards, an isotropic wet chemical etch was carried out followed by a silicon dioxide deposition to remove plasma-generated damage and passivate the surface.

The next two steps involved boron processing: conformal coating of boron on the pillar array (Fig. 4, step 3) and the “etch-back” process to expose the top of the p+ silicon for contact formation (Fig. 4, step 4). The converter material (^{10}B) was deposited on the sample in the space between the pillars (Fig. 2.) The ability to deposit conformal and uniform

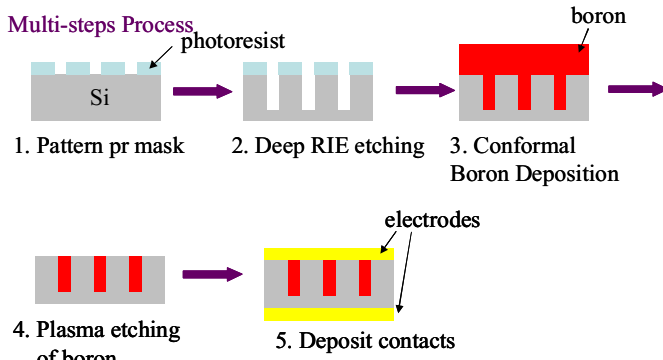


Fig. 4. Multi-step fabrication sequence for the Pillar detector.

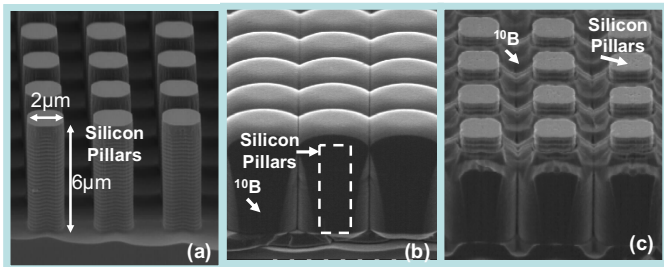


Fig. 5. Cross sectional SEMs of (a) etched pillar array, (b) after CVD of ¹⁰B and (c) after ¹⁰B etch back.

coating of ¹⁰B is one of the key steps to the success of the proposed neutron semiconductor detector. Since the charged particles are generated by the ¹⁰B (n, α) reaction, any air gap between the semiconductor and the boron layer will decrease the detector sensitivity. The semiconductor pillar platform requires complete filling of the high-aspect-ratio space between the pillars with boron. This has been developed utilizing chemical vapor deposition (CVD) with ¹⁰B enriched decaborane as the precursor and argon as the carrier gas at 425 °C. After the ¹⁰B was conformally coated on the pillar array, the “etch-back” was carried out using electron cyclotron resonance etching (ECR) with a tri-source plasma of CF₄/H₂/O₂ gas mixtures. Lastly aluminum was sputtered on to the structures to fabricate the electrodes. (Fig. 4, step 5) Cross-sectional SEMs are shown in Fig. 5 to illustrate the pillar detector processing scheme.

IV. CHARACTERIZATION

To perform electrical characterization of the pillar P-I-N diodes, a test device was fabricated using photoresist for planarizing the pillar array and sputtered aluminum for the electrodes. Current versus voltage (IV) and capacitance versus voltage (CV) measurements were performed on a Cascade REL 6100 probe station with a Keithly 4200 semiconductor parameter analyzer. The IV characteristics of the pillar arrays with 6 µm pillar height, 2 µm pillar diameter, 4 µm pitch, and an active area of 2.6 mm x 2.8 mm are shown on a linear scale in Fig. 6. Rectifying behavior was achieved with low leakage current. A comparison of the reverse bias leakage current between a pillar device and a planar device without the converter layer is shown in Fig. 7. The reverse bias leakage current was comparable to planar diodes. Fig. 8

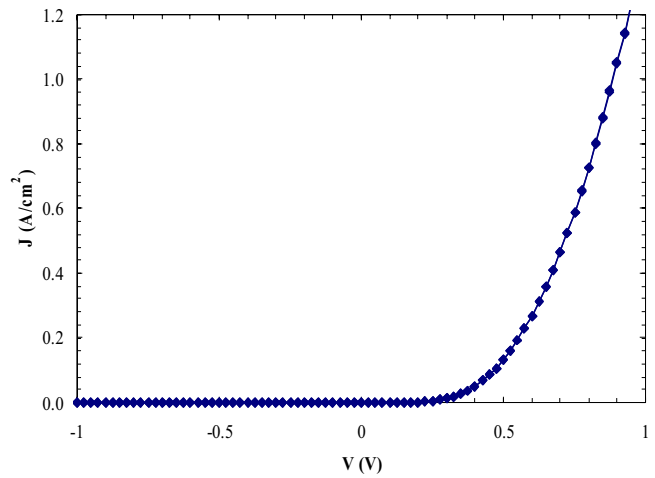


Fig. 6. Current versus voltage measurement of a 6 µm tall pillar P-I-N diode.

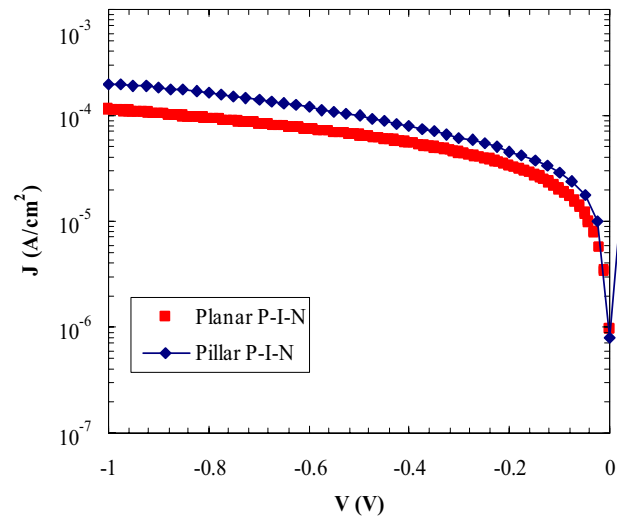


Fig. 7. Comparison of reverse bias leakage current of a 6 µm tall pillar structured diode with a planar P-I-N diode.

shows the capacitance versus voltage measurement of the pillar P-I-N diode. The device was fully depleted at a reverse bias of -0.1 V demonstrating low-voltage operation.

An alpha spectrum was obtained for this device using a ²⁴²⁻²⁴³Cm source. For this measurement, the detector was placed in a vacuum chamber with an uncollimated 0.2 µCi ^{243,244}Cm alpha source. The detector was attached to Ortec 142PC preamplifier followed by an Ortec 485 amplifier with 3 x coarse gain using 2 µs integration time. The data acquisition time was 30 minutes. When the chamber was pumped down to less than 1 mtorr, the 5.8 MeV alpha particles could strike the sample surface without being blocked by the air molecules as in the case under ambient conditions. The resulting data is shown in Fig. 9. The energy deposition of the alpha particles in the pillars, after compensating the energy loss in the photoresist, was approximately what was expected from alpha particles generated by neutron interaction with ¹⁰B (i.e., ~1.7 MeV). The collection efficiency of the pillar detector indicate

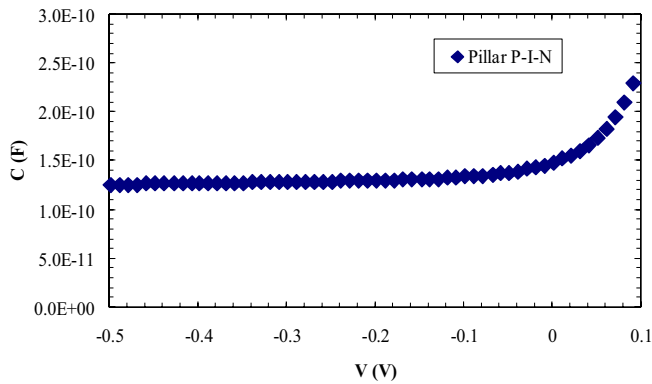


Fig. 8. Capacitance versus voltage curve for 6 μm tall pillar structured P-I-N diode.

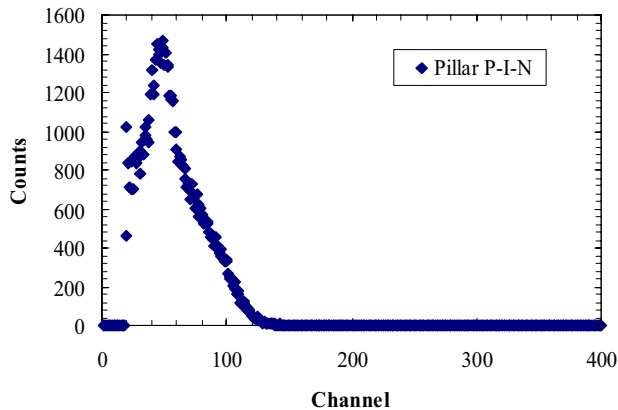


Fig. 9. Alpha spectrum of a 6 μm tall pillar P-I-N diode from $^{242-243}\text{Cm}$ source, 2V bias, 30 min. sample time.

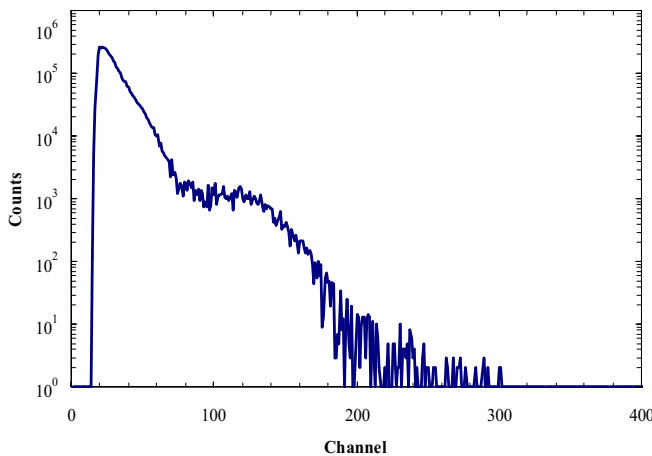


Fig. 10. The energy response of a ^{10}B filled 12 μm tall Pillar Detector from neutron interaction with ^{10}B . A ^{252}Cf neutron source moderated via polyethylene was used in the measurement with a 2V bias.

an efficiency of about 25% when compared to the data taken with a planar P-I-N diode of the same dimensions.

Neutron measurements were performed using a 12 μm pillar detector filled with the ^{10}B converter material, as shown in Fig. 10. A ^{252}Cf neutron source with neutron flux of 2.3×10^6 n/s was embedded in 15 cm thick polyethylene blocks for the measurement. The measurement time was 20 h. To obtain the thermal neutron efficiency, the observed events were

compared with results from a Monte Carlo simulation. The thermal neutron detection efficiency is estimated to be 7.3 % with an error of 1.4 %.

V. SUMMARY

A new approach has been outlined for thermal neutron detection by shifting the device structure paradigm from a planar device structure to a 3-dimensional matrix of silicon P-I-N detector pillars filled with ^{10}B converter material. Coupled MCNP-IRMA simulations showed that the thermal neutron detection efficiency of such a device structure can potentially achieve over 75 %. As a demonstration of concept, such detectors have been fabricated with the deepest etch depth of 12 μm for a 2 μm diameter pillar arrays with a 4 μm pitch. Current-voltage measurements shows that the pillar array can be fabricated without a significant increase in leakage current which can result from the plasma etch process. Neutron tests of these devices indicated an efficiency of 7.3 % for a pillar height of 12 μm . Future work will involve scaling of the device geometry to deeper heights for larger detection efficiency and optimization of the detector operation parameters. These devices have benefit to the detection of special nuclear materials by providing a thermal neutron detector that can achieve high efficiency, low voltage, small device footprint and compatibility with deployment.

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