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Future of Semiconductor Based Thermal Neutron Detectors

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ABSTRACT

Thermal neutron detectors have seen only incremental improvements over the last decades. In this paper we overview the current technology of choice for thermal neutron detection – ^{3}He tubes, which suffer from, moderate to poor fieldability, and low absolute efficiency. The need for improved neutron detection is evident due to this technology gap and the fact that neutrons are a highly specific indicator of fissile material. Recognizing this need, we propose to exploit recent advances in microfabrication technology for building the next generation of semiconductor thermal neutron detectors for national security requirements, for applications requiring excellent fieldability of small devices. We have developed an innovative pathway taking advantage of advanced processing and fabrication technology to produce the proposed device. The crucial advantage of our *Pillar Detector* is that it can simultaneously meet the requirements of high efficiency and fieldability in the optimized configuration, the detector efficiency could be higher than 70%.

Keywords: thermal neutron detector, high aspect ratio etching, pillar

1 NEUTRON DETECTION BACKGROUND

Conventional ^{3}He tube neutron detectors can achieve very high thermal neutron detection efficiency, for example, a 2" diameter tube filled with 10atm ^{3}He gas can reach > 80% detection efficiency. However, for long term stability (leakage, buildup of electronegative poison in the gas) as well as inconvenience in the replacement of very pure ^{3}He gas, the detector normally operates at a lower pressure setting thereby reducing the efficiency to ~15-30 %. For handheld operation, the common 1" tubes are normally used yielding thermal neutron detection efficiency of about 10-15%. Furthermore, the use of these proportional counter type devices is encumbered by the required high voltage operation (1000 V), sensitivity to microphonics, large device footprint, and high pressure; resulting in significant complications in air transport and deployment. By moving from gas to solid state media one gains considerable advantage in material density, which can yield a device with a smaller size, which is desirable for many applications. For solid state detectors there are two choices, scintillator and semiconductor based. Scintillator based devices can have good thermal neutron detection efficiency; however, their ability to achieve adequate neutron/gamma discrimination is limited. Additionally, due to the required photomultiplier tube the ruggedness is poor and the required operating voltage is large. These two factors significantly impede the fieldability of these devices for certain applications. In contrast, semiconductor based devices can have a low operating voltage, small device footprint and excellent stability. The remaining dilemma is how to best utilize semiconductors to design the optimized thermal neutron detector.

2 SEMICONDUCTOR OPTIONS

One approach to this dilemma is a planar structured device [1][2], as illustrated in Figure 1a, where a semiconductor is coated with the converter material. Boron with an isotopic mass of 10 (^{10}B) is frequently used as a converter material due to its excellent microscopic thermal neutron absorption cross section of 3840 barns. However, these devices are limited in efficiency due to the conflicting requirements of the ^{10}B neutron converter material. The thermal neutron ^{10}B reaction which populates mostly to the first excited state of ^{7}Li, produces an alpha particle (1.47 MeV) and ^{7}Li (0.84 MeV). These charged particles subsequently enter the semiconductor detector to create electrons and holes for generation of the electrical signal. However, these particles can travel inside the converter material only for a short distance (3.3 μm). Thus, if the boron layer is too thick, the charged particles will be absorbed before they reach the semiconductor material. This is a design conundrum because the converter material needs to be sufficiently thick to capture most of the incoming thermal neutrons. This problem results in a device that has inefficient charged carrier production, which directly translates into low neutron detection efficiency.

Building up thicker regions of the converter material and at the same time not loosing these generated alpha particles is required in order to achieve a high efficiency semiconductor thermal neutron detector. One approach to this is led by a group of researchers at the University of Nebraksa, which involves the use of boron carbide [3] this is an elegant approach to detection because this material can both convert neutrons to alphas and generate an electrical signal. However this material is not single crystal and the transport issue of the electrons and holes in the amorphous material could cause nonideal diode behavior.

Another approach, led by Doug McGregor of Kansas State University, utilizes a via hole technology to increase the adhesion of the ^{10}B converter material to the semiconductor. However, the reported hole geometry increases the neutron detection efficiency to 3.9% which is only a slight increase over the efficiency of the planar device, 2.9 % [4]. This "via hole" approach can be looked at as a general 3D approach to combining the converter material with the semiconductor detector device. We have developed an innovative pathway to fabricate an optimized 3D device to finally be able to deliver a high efficiency thermal neutron detector, which to date has been infeasible. Our device design [5] is shown in Figure 1b, and is discussed in the next section.

3   LLNL PILLAR CHIP

Our proposed design is a technology advance that can increase the neutron detection efficiency from the current semiconductor devices 2-5% [2] towards greater than 70%. The platform consists of etched pillars of P-I-N diodes which are grown on a planar semiconductor substrate. The converter material and the detector material are inter-digitated such that charged particles from the thermal neutron ^{10}B reaction have a significantly higher probability of impinging the detector material due to the close proximity. Moreover, the thickness of active converter material is not limited, since the preponderance of the charged particles is detected by the adjacent pillars. In our *Pillar Detector* we are able to separate the constraints on the boron thickness via defining the pillar height (etch depth) which defines the material that will absorb the neutron flux. At the same time we are able to define the pitch of the pillars lithographically to have the highest possible interaction of the alphas with the semiconductor pillar to insure charged carrier generation in the pillars (see Figure 1b).

Preliminary simulations that used results from a Monte Carlo based code (MCNP: Monte Carlo n-particle) to generate neutron interaction histories and then incorporated these histories into TRIM codes (transport of ions in matter) for changed-particles energy loss calculations, are shown in Figure 2a, indicate that the detector efficiency could reach 65 % with an etch depth of 50μm and a pillar width and spacing of 2μm. A further increase in efficiency can be achieved with even smaller features.

A comparison between our proposed device and ^{3}He tubes is shown in Table 1. The use of ^{3}He tubes is encumbered by the required high voltage operation (1000 V), sensitivity to microphonics, large device footprint, and high pressure; resulting in significant complications in air transport and deployment. The crucial advantage of our *Pillar Detector* is that it can simultaneously meet the requirements of high efficiency and fieldability. The estimation in cost for the *Pillar Detector* is based on the price of silicon photodetectors which use similar fabrication technology.

4   FABRICATION METHODS

Figure 3 shows the process flow for our *Pillar Detector*. Step one involves conventional contact lithography to pattern our pillar array. This technology is inexpensive and scalable to large wafers. The next step involves the ability to etch highly anisotropic and smooth features into the silicon wafer. This is carried out by plasma processing. Our requirements for plasma etching are based on the relationship between detection efficiency and etch depth, as shown in Figure 2a. This requires anisotropic features with an etch depth of 50μm with an aspect ratio of 1:25 for the 2μm diameter pillar detector geometry, which is our device design that has both high efficiency and ease of lithography. Adequate masking materials and vertical etched features with smooth sidewalls are also required. These requirements can be met with high density plasma systems which employ high density plasma to provide a large ion flux with small ion energy that yields low-damage etching [6][7]. Figure 2b shows a representative SEM image of our etching capability. Our current etching technology scales to 10 μm etch depths, and work is currently being done to scale the etch depth to our long term goal of 50μm. Our initial devices employ a silicon based detector with etching done by a deep RIE system with an ICP plasma source and the time-multiplexed "Bosch Process", which uses SF_6 to etch silicon and C_4F_8 for the passivation step. With a large etch depth and backfill with boron, a near complete thermal neutron capture is theoretically possible. The backfill with boron is shown in step 3. We are currently developing a high temperature CVD process [8] to coat these high aspect ratio features (however sputter and e-beam deposition methods can also be used). Step 4 and 5 are required to expose the top of the PIN semiconductor material for contact formation (step 6).

5   CONCLUSION

We have outlined a new approach to the detection of thermal neutrons by moving from a planar device structure to a 3-dimentional matrix of PIN detector pillars, with converter material filling this matrix. With this structure we have shown *via* simulations that the detector efficiency can have a revolutionary increase from roughly 2-5% towards over 70%. This efficiency can be realized by micron sized features, however further improvements can be achieved by shrinking the device geometry to the nanoscale. Furthermore, by covering a wide range of device sizes, the transport of both radiation and charged carriers can be exploited. This will make possible important advances in neutron detection.

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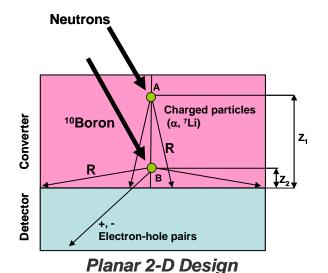
Figure 1a Schematic of planar semiconductor thermal neutron detector [1].
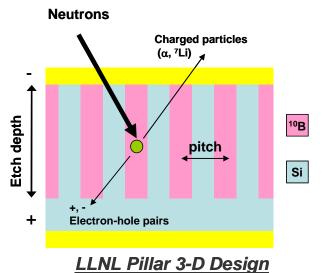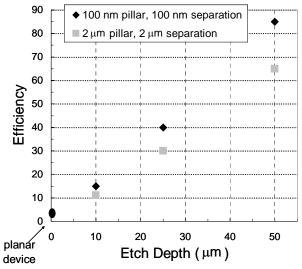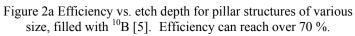
Figure 1b Proposed *Pillar Detector* with ^{10}B in a semiconductor detector matrix [5].

Figure 2a Efficiency vs. etch depth for pillar structures of various size, filled with ^{10}B [5]. Efficiency can reach over 70 %.
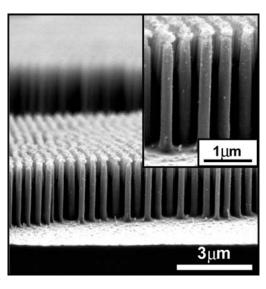

Figure 2b A representative cross-sectional SEM photomicrograph of etched silicon pillars [6].

Table 1: Comparison of ^{3}He tubes with our proposed solid state pillar structured detector.

	^{3}He Tube	LLNL 3-D Pillar detector
Efficiency (fieldable)	< 30 %	70%
Cost	$ 4K	$ 0.2K
Required voltage	1000 V	< 10 V
Size (probe)	(5 ϕ) cm x 10 cm	1 x 1 x 0.1 cm^3
Weight (includes power)	700 g	10 g
Fieldability	Microphonics, HV, air transport	Not commercially available

Multi-step Process

1. Pattern SiO$_2$ mask

2. Deep RIE etching

$Si + SF_6 \rightarrow SiF_4 + SF_2$

3. Boron Deposition

4. Boron planarization
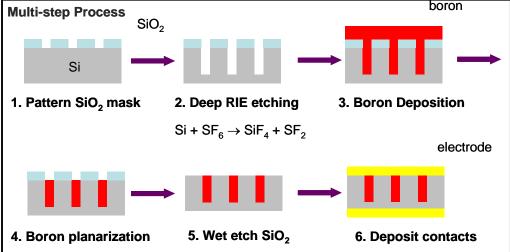
5. Wet etch SiO$_2$

6. Deposit contacts

Figure 3 Multi-step fabrication process for our *Pillar Detector* [5].