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Low-voltage operation of metal-ferroelectric-insulator-semiconductor diodes incorporating a ferroelectric polyvinylidene fluoride copolymer Langmuir-Blodgett film

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We report the electrical characteristics of metal-ferroelectric-insulator-semiconductor structures, where the ferroelectric layer is a Langmuir-Blodgett film of a copolymer of 70% vinylidene fluoride and 30% trifluoroethylene. The 36-nm thick copolymer films were deposited on thermally oxidized (10 nm SiO_2) *p*-type silicon and covered with a gold gate electrode. Polarization-field hysteresis loops indicate polarization switching in the polymer film. The device capacitance shows hysteresis when cycling the applied voltage between ±3 V, exhibiting a zero-bias on/off capacitance ratio of over 3:1 and a symmetric memory window 1 V wide, with little evidence of bias that can arise from traps in the oxide. Model calculations are in good agreement with the data and show that film polarization was not saturated. The capacitance hysteresis vanishes above the ferroelectric-paraelectric transition temperature, showing that it is due to polarization hysteresis. The retention time of both the on and off states was approximately 15 min at room temperature, possibly limited by leakage or by polarization instability in the unsaturated film. These devices provide a basis for nonvolatile data storage devices with fast nondestructive readout. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2218463]

INTRODUCTION

If the gate insulator of a conventional metal-oxide field-effect transistor (MOSFET) is replaced by a ferroelectric material, a so-called ferroelectric field effect transistor (FeFET) is obtained. The reversible polarization of the ferroelectric layer is used to switch the resistance of the semiconductor source-drain channel at zero gate bias between low and high values representing "0" and "1" logic states. Since the polarization of the ferroelectric layer is bistable, the device retains its state even when power is removed and is therefore suitable for integration into nonvolatile ferroelectric random-access memory (NV-FRAM). The attractive features of the FeFET as a memory element include nondestructive readout, nanosecond write, read and erase times, a small device area, and low energy consumption.[1] Although the FeFET was proposed in 1963,[2] no commercial products incorporating FeFETs have yet been realized. Most studies have focused on complex inorganic oxide ferroelectrics, e.g., $PbZr_xTi_{1-x}O_3$, $SrBa_2Ta_2O_9$, or $BiMgF_4$, integrated with complementary metal oxide semiconductor (CMOS) silicon technology.[1] The high deposition temperatures and oxygen pressures required in preparation of the oxide ferroelectrics promote chemical reactions and layer interdiffusion that degrade the semiconductor and insulator layers and create charge traps. These processes reduce the performance of a FeFET and lead to degradation of state contrast (fatigue), drift in the device states (imprint), and ultimately device failure. The incorporation of additional high-*k* oxide buffer layers and other fabrication features in metal-ferroelectric-insulator-semiconductor (MFIS) structures has helped mitigate these problems, but this has the disadvantage of increasing device complexity and fabrication cost.[3] Moreover, insufficient compensation of the ferroelectric bound charge leads to a high depolarization field[4] and probably to electron injection, which both contribute to the low retention times of MFIS and FeFET device states. Recent reports give retention times of a few days at best.[5–7]

Ferroelectric polymers are promising alternatives to perovskites for use in NV-FRAMs because of their chemical stability and low dielectric constants. The most extensively studied ferroelectric polymer system is based on vinylidene fluoride and its copolymers with trifluoroethylene

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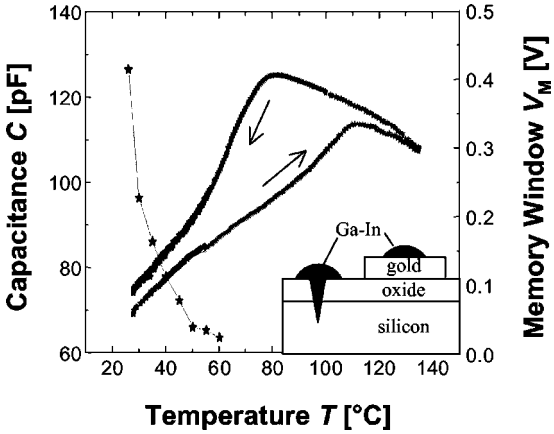

FIG. 1. The MFIS capacitance measured as the temperature was cycled across the ferroelectric-paraelectric phase transition (line, left axis) and the memory window as a function of temperature (stars, right axis). Inset: Schematic cross section of the MFIS showing the locations of the GaIn ground and gate contacts.

P(VDF-TrFE).[8] These polymers have moderately high remanent polarization $P_r \approx 100\ \mathrm{mC/m^2}$, enabling large device contrast, low dielectric constants $\kappa \approx 10$, which can reduce operating voltages compared to the high-κ ferroelectric oxides.[9] There have been encouraging laboratory demonstrations of nonvolatile memory elements made by adding a P(VDF-TrFE) layer to the gate dielectric of silicon MFIS (Refs. 10–13) and FeFET (Ref. 10) structures. Two groups have recently demonstrated all-organic FeFET devices incorporating a P(VDF-TrFE) gate and with an organic semiconductor of pentacene[14] or a polyphenylene vinylene variant (MEH-PPV).[12,15] These are very encouraging developments, but operating voltages for ferroelectric polymer memories made by solvent spin coating are still quite high (>50 V) because of the relatively high coercive field (>50 MV/m) and the relatively thick films (~1 μm). Much lower operating voltages, and higher film quality, can be achieved by using Langmuir-Blodgett deposition to make ultrathin ferroelectric films.[16] We recently demonstrated MFIS devices consisting of a 170-nm thick P(VDF-TrFE) Langmuir-Blodgett (LB) film and a 100-nm-thick silicon oxide layer on *n*-type silicon, which operate between ±25 V.[17] Here we report the fabrication and characterization of a *p*-type silicon MFIS device containing a 36-nm-thick ferroelectric polymer layer and operating between ±3 V.

EXPERIMENTAL METHODS

The MFIS devices, which are shown schematically in the inset to Fig. 1, were made as follows. The substrates of commercial *p*-type Si with (100) crystal orientation, a diameter of 2.5 cm, and a resistivity of 1–10 Ω cm were pretreated by the Radio Corporation of America (RCA) cleaning method[18] to remove metal and organic contaminants from the silicon surface. The SiO_2 insulating layer was thermally grown to a thickness of 10±2 nm, as determined by ellipsometry. The substrates were then annealed in forming gas (90% N_2+10% H_2) at 450 °C for 10 min to saturate dangling bonds and minimize charge-trapping defects. The ferroelectric films consisted of the copolymer P(VDF-TrFE 70:30) deposited by LB deposition from a water subphase held at a surface pressure of 5 mN/m and a temperature of 25 °C. Under these conditions, the 20-layer LB films should be 36±1.4 nm thick.[19] The substrate with LB film was annealed at 130 °C for 1 h to improve the polymer crystallinity.[20] Further details of the ferroelectric LB film preparation are given elsewhere.[16,21] A circular Au gate electrode with diameter of 60 μm was deposited by vacuum evaporation through a shadow mask. An Ohmic contact was made on top of the silicon substrate to one side of the gate by scratching into the silicon and contacting with a Ga(85%)In(15%) liquid eutectic. The Au gate electrode was also covered with the GaIn eutectic. For electrical measurements two Au tips were inserted into the liquid eutectics. In this way the mechanical force on the device, especially on the PVDF film, was minimized. This quasi-stress-free contacting method avoids piezoelectric perturbations of the ferroelectric film polarization and mechanical damage to the film. All measurements were made at room temperature unless otherwise noted.

The MFIS device capacitance C is given by the series combination,

$$\frac{1}{C} = \frac{1}{C_F} + \frac{1}{C_I} + \frac{1}{C_S}, \tag{1}$$

where C_S is the (variable) capacitance of the semiconductor, C_I is the capacitance of the insulating layer, and $C_F = \kappa\varepsilon_0 A/t$ is the capacitance of the ferroelectric film. Here A is the area of the gate electrode and t is the thickness of the LB film. The device capacitance C was measured with an HP LCR4284A impedance analyzer as a function of frequency, gate bias voltage V_g, and temperature I. The small signal excitation amplitude was fixed at 50 mV for all measurements and the gate bias voltage slew rate was less than 2 V/min.

The ferroelectric state of the LB film in the MFIS was probed by measuring the device capacitance as a function of temperature at a rate of 2–3 °C/min at a constant gate bias of −3.0 V. The *p*-type semiconductor was in the accumulation region where $C_S \gg C_F$, C_I so that the semiconductor made a negligible contribution to the device capacitance. The device temperature was controlled by thermally contacting it to a temperature-stabilized hot plate. The capacitance C_I of the SiO_2 insulating layer has only a weak temperature dependence, so the dependence of the device capacitance on temperature is due mostly to the changing dielectric constant of the LB copolymer film.[16] The capacitance of the MFIS device exhibits distinct peaks at 110 °C on heating and 80 °C on cooling (see Fig. 1), corresponding to the ferroelectric-paraelectric and paraelectric-ferroelectric phase transitions, respectively. The large thermal hysteresis is also typical of VDF copolymers and is due to metastability of the two phases near the transition temperature T_c in the case of a first order phase transition.[9]

RESULTS

The operation of the MFIS differs from an ordinary metal-oxide-semiconductor (MOS) diode because the rema-

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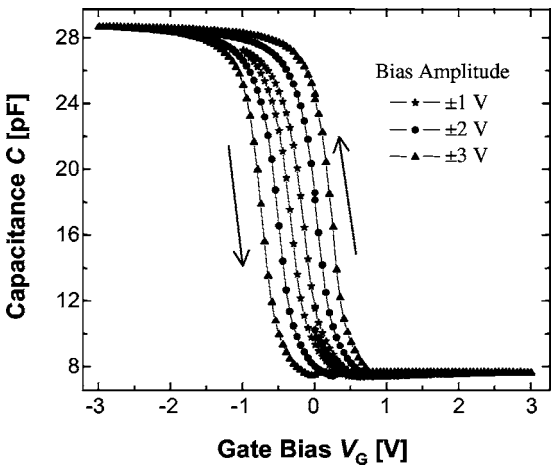

FIG. 2. *C-V* measurements of a MFIS structure at room temperature as a function of the gate bias voltage with respect to the ground contact (see Fig. 1, inset), cycled with amplitudes of 1, 2, and 3 V. The capacitance was measured with a small signal amplitude of 50 mV and a frequency of 100 kHz.

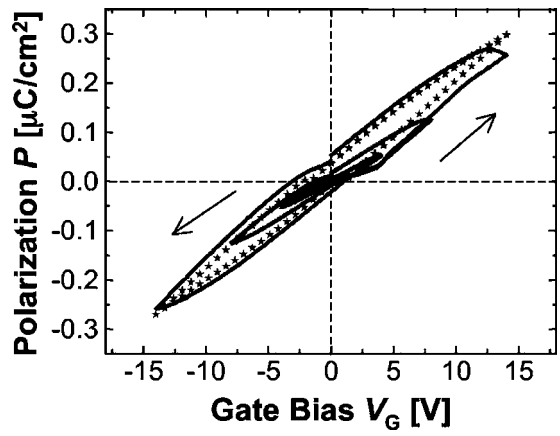

FIG. 3. *P-V* measurements for gate voltage sweep amplitudes of 3.75, 7.5, and 15 V (solid line) at a sweep frequency of 0.1 Hz. For the *P-V* curve with ±15 V gate bias amplitude. The results of the simulation with sweep amplitude 15 V are indicated by the dotted line.

nent polarization P_r of the ferroelectric film produces an additional potential drop across the ferroelectric $\Delta V_F = \pm P_r t/\kappa\varepsilon_0$, where the $\pm$ sign denotes the direction of the polarization with respect to the gate electrode. The ferroelectric film polarization can be set to either state by applying a sufficiently large positive or negative gate bias $\pm V_g$. Figure 2 shows a set of C-V_g curves recorded at a frequency of 100 kHz and an amplitude of 50 mV as the gate bias V_g was cycled between ±1, ±2, and ±3 V. At −3 V, the semiconductor is in accumulation mode, and therefore $C_S \gg C_F$, C_I and the device capacitance is highest. At +3 V, the semiconductor develops a depletion layer under the gate, and therefore has a finite capacitance, reducing the device capacitance. The capacitance cycled counterclockwise, which is consistent with a polarization switching mechanism and contrary to the hysteresis developed by charge injection. The shape of the curves follows that of an ideal MOS capacitor and can be fully understood in terms of MOS physics,[22] except for the hysteresis due to the reversal of the ferroelectric film polarization. The size of the hysteresis V_M, the so-called memory window, was calculated from the difference between the flatband voltages measured in the two device states,

$$V_M = V_{\mathrm{FB}}{}^{+} - V_{\mathrm{FB}}{}^{-}, \tag{2}$$

where the flatband voltage $V_{\mathrm{FB}}^{\pm}$ was determined by using the peak in the ac loss and verified by a linear extrapolation of a $1/C^2$ vs V plot in the depletion region.

The C-V_g hysteresis memory window is centered at 0 V, indicating that there is negligible voltage offset due to, e.g., charge trapping in the oxide layer.[17] In addition, there was no evident smearing on the depletion side (negative) of the cycle, indicating a low interface state density.[19] The low processing temperature during copolymer deposition as well as the low annealing temperature of approximately 130 °C did not affect the SiO_2 interface. This is an important advantage compared to oxide ferroelectrics, which must be annealed at much higher temperatures that alter the other device components.[23] The counterclockwise C-V_g hysteresis became larger with increasing bias voltage due to the increase in the remanent polarization of the ferroelectric polymer layer.

One temperature-dependent quantity is the memory window V_M, which should be proportional to the remanent polarization of the ferroelectric film.[24] The memory window should decrease with increasing temperature as the remanent polarization decreases, vanishing in the paraelectric state. The memory window of the MFIS device decreased steadily as the device was heated, as shown in Fig. 1, vanishing well below the ferroelectric-paraelectric phase transition temperature of 110 °C. It is likely that the vanishing of the memory window well below the transition temperature is due to the lack of polarization saturation, so that the remanent polarization goes to zero even though the film is still ferroelectric, because it is unstable against formation of opposing domains. This is probably connected with the short retention time, as will be discussed below. Therefore, we conclude that the memory window is due to the switchable remanent polarization of the ferroelectric film.

The polarization of the ferroelectric film in the MFIS structure was obtained from *P-V* measurements made at a frequency of 0.1 Hz with a variable triangular voltage sweep. This measurement was made with an Aixacct model TF 2000 ferroelectric device analyzer. Figure 3 depicts a set of polarization-voltage $P(V)$ measurements recorded with varied gate voltage sweep amplitudes. The kinks in the middle of the hysteresis loops are caused by the abrupt change of the silicon capacitance as it crosses into the depletion region.[24] The polarization hysteresis increased with increasing voltage, but even at the highest voltage sweep amplitude of ±15 V, the hysteresis was not saturated. This is consistent with polarization measurements on similar MFM structures,[25] where 30 V was needed to completely switch ferroelectric films of comparable thickness. In addition, we focused on simulations of the polarization in a MFIS system using a FeFET model programed into the ferroelectric device analyzer.[26] The simulation of the polarization hysteresis $P(V_g)$ as the device voltage is cycled between ±15 V is shown in Fig. 4 (dotted curve) and is in good agreement with the measurements. The simulation parameters were

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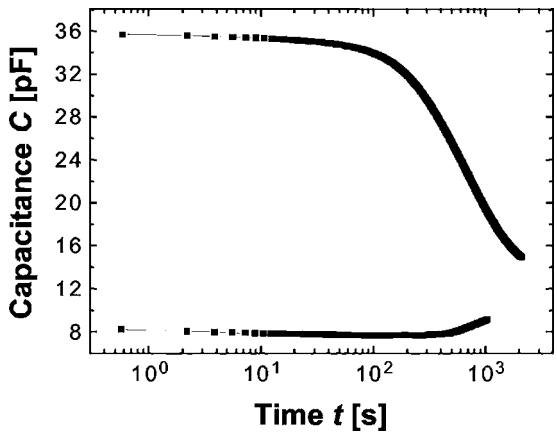

FIG. 4. State retention tests by measuring the evolution of the MFIS capacitance at zero gate bias after poling the sample with a bias voltage pulse of either positive or negative 4 V applied for 1000 s.

10^{16} cm^{-3} for the silicon doping level and 17 nm for the oxide thickness, which is somewhat thicker than the values determined from ellipsometry (10 nm), but it does result in a better fit to the device properties. The copolymer layer properties used in the model fit were $P_s=5\ \mu\mathrm{C/cm}^2$, $P_r=4\ \mu\mathrm{C/cm}^2$, $E_C=500$ kV/cm, $\kappa=13$, and $t=36$ nm for the spontaneous polarization, remanent polarization, coercive field, dielectric constant, and thickness, respectively.

Another important parameter for FeFETs is the state retention time, which is defined as the longest time after the end of a state-setting pulse that the on and off states are distinguishable. The retention measurements were performed by applying either a positive or negative voltage pulse to set the device state and subsequently measuring the capacitance in the middle of the memory window, which happens to be at zero gate bias for this device (see Fig. 1). Because of the large initial on:off ratio of 3:1 at zero bias, it is possible to distinguish the two states. Figure 4 shows an exemplary retention measurement for the MFIS structure. A voltage pulse of positive or negative 4 V was applied for 1000 s to set the device in the on or off states, respectively. The retention times recorded under these conditions were typically in the range of 15–20 min. The relatively short retention time may be a result of polarization instability of the unsaturated ferroelectric film or to leakage currents that charge up the ferroelectric-insulator interface.[17] Polarization instability is the spontaneous formation of opposing domains, thus reducing the net polarization in a single-domain film due to uncompensated surface charge at the ferroelectric-oxide interface. Charge leakage through the oxide would compensate this surface charge by charging the ferroelectric-oxide interface. Either mechanism would reduce the voltage across the ferroelectric layer and therefore reduce hysteresis as zero bias. Charge trapped in the oxide could contribute to screening, but this would also produce a horizontal offset in the capacitance-voltage hysteresis, whereas the data in Fig. 2 show no significant shift.

CONCLUSIONS

We have described measurements of the electrical properties of MFIS structures consisting of 20 deposited layers of ferroelectric P(VDF-TrFE 70:30) copolymer LB film and a 10 nm thin SiO_2 insulating layer on a *p*-type silicon substrate. Liquid metal contacts were used to reduce mechanical stress on the PVDF during measurements. The *P*-*V* and *C*-*V* measurements exhibit counterclockwise hysteresis indicative of ferroelectric polarization reversal. The capacitance hysteresis widens with increasing cycle voltage due to the increase of remanent polarization. The memory window at room temperature was approximately 1 V, with a corresponding zero-bias on:off ratio of 3:1, for an operating voltage of ±3 V. The films exhibit key features of the first order ferroelectric-paraelectric phase transition, which is evident in the thermal hysteresis of the device capacitance in accumulation mode. Hysteresis in both *C*-*V* and *P*-*V* curves vanishes at higher temperature, as it should, when the samples are heated into the paraelectric phase. Retention measurements indicate relatively short storage times, likely due to instability of the unsaturated film polarization. We will next focus on alternative high-*k* gate oxides with high dielectric constants such as HfO_2, $DyScO_3$, or CeO_2 to keep the operation voltage below 10 V while increasing the oxide thickness in order to reduce leakage currents. The low phase transition temperature, approximately 80 °C,[25] of the copolymer films, makes it easy to show that the C-V_g hysteresis is due to polarization hysteresis. However, this will limit the operating temperature range of the device. The operating range can be extended by using a copolymer with higher VDF content, which would raise the transition temperature to 145 °C.

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