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Timothy J. Reece
University of Nebraska, reecetj@unk.edu

Stephen Ducharme
University of Nebraska, sducharme1@unl.edu

Modeling of metal-ferroelectric-insulator-semiconductor structures based on Langmuir–Blodgett copolymer films

Timothy J. Reece[a] and Stephen Ducharme[b]
Department of Physics and Astronomy, Nebraska Center for Materials and Nanoscience, University of Nebraska, Lincoln, Nebraska 68588-0111, USA

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Among the ferroelectric thin films used in field-effect transistor devices; the ferroelectric copolymer of polyvinylidene fluoride (PVDF) ($-CH_2-CF_2-$), with trifluoroethylene (TrFE) ($-CHF-CF_2-$), has distinct advantages, including low dielectric constant, low processing temperature, low cost, and compatibility with organic semiconductors. The operation of a metal-ferroelectric-insulator-semiconductor structure with P(VDF-TrFE) as the ferroelectric layer was analyzed and optimized by numerical solution of the Miller and McWhorter model. A model device consisting of 20 nm PVDF/TrFE on a 10-nm-thick high-k dielectric buffer exhibits a memory window of 5 V with an operating voltage of ± 15 V. The operating voltage can be reduced to ± 12 V by reducing the ferroelectric and dielectric thicknesses to 10 and 5 nm, respectively. © *2009 American Institute of Physics*. [doi:10.1063/1.3271581]

I. INTRODUCTION

A promising material class for use in nonvolatile memories consists of ferroelectric polymers, such as polyvinylidene fluoride (PVDF, consisting of $C_2H_2-C_2F_2$ monomers) and its copolymers with trifluoroethylene ($-CHF-CF_2-$).[1] The VDF copolymers have a large spontaneous polarization, approximately 0.1 C/m^2, excellent polarization stability, and switching times as short as 25 ns.[2] Their high resistivity of up to 1000 Ω cm means low leakage, suitable for nondestructive readout applications. Furthermore, they do not require high-temperature processing, have outstanding chemical stability, low fabrication costs, and are nontoxic. Ferroelectric polymers have been incorporated into nonvolatile memory devices, such as metal-ferroelectric-insulator-semiconductor (MFIS, see Fig. 1 inset) capacitors and ferroelectric field-effect transistor (Fe-FET) structures, in both spun film[3–5] and Langmuir–Blodgett (LB) form.[6,7]

Miller and co-workers[8,9] provided a useful model for the device characteristics of MFIS and Fe-FET structures by combining the charge-sheet model for the semiconductor surface potential[10] with a *tanh* function representation of the ferroelectric polarization hysteresis.[11] This model provides insight into the nonlinear and hysteretic interplay between the polarization state of the ferroelectric and the surface charge of the semiconductor to illustrate, for example, the importance of high doping to achieve high polarization remanence after biasing the semiconductor into strong inversion,[12] and how minor hysteresis loops in the ferroelectric result in different device state paths.[13] The Miller–McWhorter model has previously been applied to model MFIS (Ref. 14) and Fe-FET (Ref. 15) structures containing oxide ferroelectrics such as lead zirconate-titanate. The present work extends this model to ferroelectric polymer LB films, which have very different operating characteristics.[16]

II. SUMMARY OF THE MODEL

The electrostatic model for the MFIS capacitor structure (Fig. 1 inset) is obtained from Maxwell's equations, the constitutive relations for each layer, and appropriate boundary conditions. For all layers, the electric field E and the electric potential ϕ are related by $E=-\nabla\phi$, where the total potential drop across the device, the gate bias voltage, is

$$V_G = \Phi_{MS} - \frac{\sigma_S}{C} - \frac{P_f d_f}{\varepsilon_0 \varepsilon_f} + \phi_S, \tag{1}$$

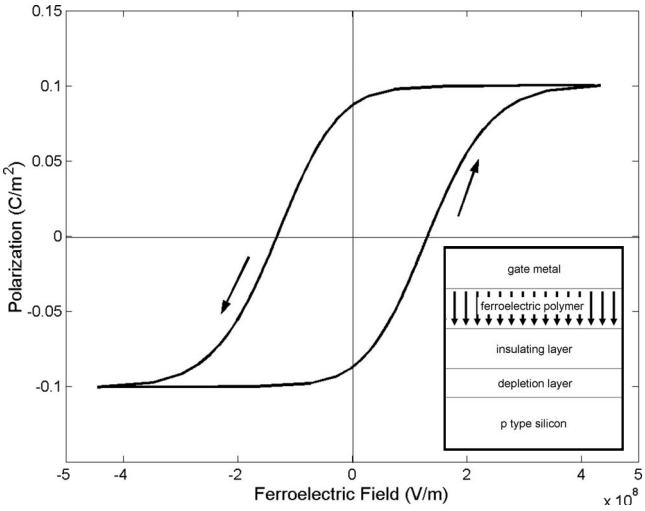

FIG. 1. Polarization-electric field (P-E) hysteresis loop for a ferroelectric film modeled from Eq. (3) using parameters listed in Table I. Inset: Structure of an MFIS consisting of a doped silicon wafer, passive oxide layer, ferroelectric layer, and gate electrode.

[a]Electronic mail: reecet@unlserve.unl.edu.
[b]Electronic mail: sducharme1@unl.edu.

$$C = \left(\frac{d_i}{\varepsilon_0 \varepsilon_i} + \frac{d_f}{\varepsilon_0 \varepsilon_f} \right)^{-1}, \tag{2}$$

where ϕ_S is the semiconductor surface potential, σ_S is the semiconductor surface charge, P_f is the ferroelectric polarization, ε_0 is the vacuum permittivity, $\varepsilon_{f,i}$ is the dielectric constant and $d_{f,i}$ is the thickness of the ferroelectric or insulating layer, and Φ_{MS} is the work function difference between the gate metal and the semiconductor.

While the insulating layer is adequately described by a linear dielectric constant (as represented in Eq. (2)), the semiconductor and ferroelectric layers introduce both nonlinearity and hysteresis. The electric displacement of the ferroelectric layer $D_o = \varepsilon_0 \varepsilon_f E_f + P_f(E)$ consists of contributions from linear polarizability plus the ferroelectric polarization $P_f(E)$, which depends on both the magnitude and history of the electric field E. In the case of saturated hysteresis loops, we choose the hyperbolic tangent (tanh) form of the (P-E) hysteresis loop[8,9]

$$P_f(E) = \pm P_S \tanh\left[\frac{(\pm E - E_C)}{2\delta} \right], \tag{3}$$

where P_S is the saturation polarization and the loop shape parameter

$$\delta = E_C \left[\ln\left(\frac{1 + P_R/P_S}{1 - P_R/P_S} \right) \right]^{-1} \tag{4}$$

depends also on the remanent polarization P_R. The $\pm$ signs refer to sweeping the field toward negative and positive saturation, respectively. The tanh form of the P-E hysteresis loop (Fig. 1) described by Eq. (2) is a good fit to data from polycrystals and crystals that support a large number of domains during switching.[8]

The semiconductor state is defined by performing an iteration in the surface potential and through the following expression,[8] which relates the silicon surface charge density σ_S to the silicon surface potential ϕ_S through the expression

$$\sigma_S = \mp \sqrt{2 q_e N_A \varepsilon_0 \varepsilon_S} \times \left[\sqrt{e^{2\phi_F/\phi_t}(-\phi_t + \phi_S + \phi_t e^{-\phi_S/\phi_t}) - \phi_t - \phi_S + \phi_t e^{\phi_S/\phi_t}} \right], \tag{5}$$

where $\phi_t = kT/e$, ε_S is the dielectric constant of the semiconductor, N_A is the dopant concentration, and ϕ_F is the quasi-Fermi potential

$$\phi_F = \frac{kT}{e} \ln\left(\frac{N_A}{n_i} \right). \tag{6}$$

Saturation of the ferroelectric polarization requires a larger voltage (than in accumulation) because of the potential drop across the depletion layer.[13] The gate voltage required to saturate the ferroelectric film can be determined by noting that the semiconductor potential in the strong inversion mode is twice the Fermi potential, $\phi_S = 2\phi_F$.

The recommended device operating voltage would be the minimum gate voltage required to saturate the ferroelectric film, and can be determined by inserting the saturation values, P_S and E_S into Eq. (1) to yield the following expression:

$$V_{GB}^S = \Phi_{MS} + \frac{\varepsilon_0 \varepsilon_f E_S}{C} + \frac{P_S d_i}{\varepsilon_0 \varepsilon_i} + 2\phi_F. \tag{7}$$

The saturation field of the ferroelectric film E_S is conservatively set at 150% of the nominal coercive field E_C, the half width of the hysteresis loop. While the polarization and dielectric constant are insensitive to thickness, the coercive field depends strongly on thickness, ranging from 50 MV/m in thick films, to 500 MV/m in films of 15 nm or thinner.[17] The device operation voltage, therefore, depends on both the ferroelectric film thickness and the thickness and dielectric constant of the insulating layer. This is illustrated in Fig. 2 for two insulators. For silicon oxide [$\varepsilon_i = 3.9$, Fig. 2(a)], the saturation gate voltage is quite high, even with thickness 10 nm. For hafnium oxide [$\varepsilon_i = 25$, Fig. 2(b)], the saturation voltage is significantly reduced, and is more sensitive to the thickness of the ferroelectric layer.

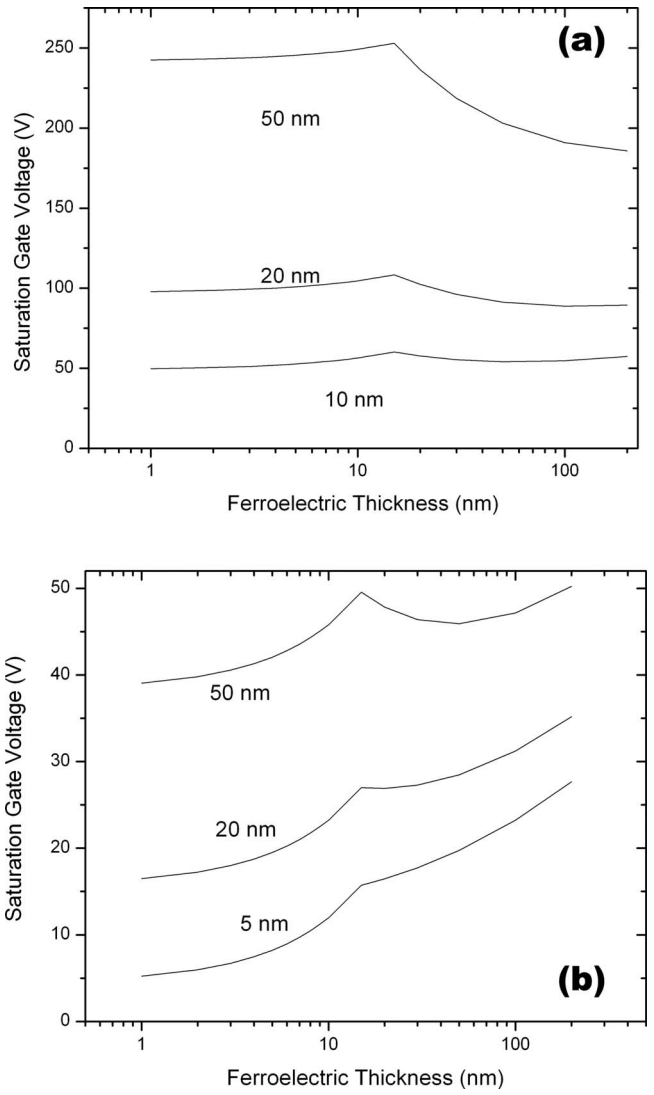

FIG. 2. The required saturation gate voltage as a function of ferroelectric film thickness for different thicknesses of silicon oxide (a) and hafnium oxide (b).

TABLE I. Parameters used in the model.

Parameter	Value
Silicon doping level N_A	1×10^{16} cm^{-3} (p-type)
Insulating layer dielectric constant ε_i	25 (hafnium oxide)
	3.9 (silicon oxide)
Insulating layer thickness d_i	10 nm
Ferroelectric layer dielectric constant ε_f	10
Ferroelectric layer saturation polarization P_S	0.1 C/m^2
Ferroelectric layer remanent polarization P_R	0.09 C/m^2
Ferroelectric layer coercive field E_C	125 MV/m
Ferroelectric layer thickness d_f	20 nm

III. MODEL APPLICATION TO FERROELECTRIC COPOLYMER FILMS

In this section, the model developed by Miller and McWhorter[9] will be applied to investigate a particular MFIS device involving a 20-nm-thick PVDF copolymer film. The model takes into account the properties of the ferroelectric copolymer LB films,[6,16,18] as summarized in Table I. A nominal coercive field of 125 MV/m suffices, and the remainder of the modeling will use this value. The hysteresis loop for the ferroelectric layer (Fig. 1) is difficult to measure directly in MFIS structures but it is readily extracted from the model as shown in Fig. 3(a), where the field in the ferroelectric film reached a maximum of 450 MV/m (or about 2.6 times the coercive field) in the accumulation mode. Because of the hysteresis in this field plot, a significant field exists in the ferroelectric layer even at zero gate bias. This zero-bias field tends to destabilize the polarization state and thus it is referred to as the "depolarization field." The depolarization field arises because the oxide or semiconductor that is in direct contact with the ferroelectric cannot provide enough charges to fully compensate for the surface charge of the polarized ferroelectric. The depolarization field is the cause for the reduced remanent polarization evident in a narrowing of the hysteresis loop shown in Fig. 3(b), compared to the one from the simple MFM capacitor (Fig. 1), where the metal electrodes (ideally) provide complete compensation of the polarization. The depolarization field in the MFIS is larger after saturating the sample in strong inversion (125 MV/m) with positive gate bias than in accumulation (100 MV/m) with negative gate bias and therefore the MFIS should be slightly more stable in the negative-bias polarization state. The depolarization field will tend to further reduce film polarization and consequently reduce the capacitance hysteresis over time, making the states less distinct. Film depolarization is therefore an important issue in state retention. It should be noted that this model assumes that electrostatic steady state is always established within the device structure. This may not be the case if higher ramp rates are used and the ferroelectric film (or semiconductor surface charge) is not given enough time to come to equilibrium. In those situations, minority carriers in inversion mode may not respond to the applied signal and the remanent polarization would be reduced. That is, the finite minority carrier response time or polarization switching time, or both, will tend to shrink the memory window under high-speed operation.[19]

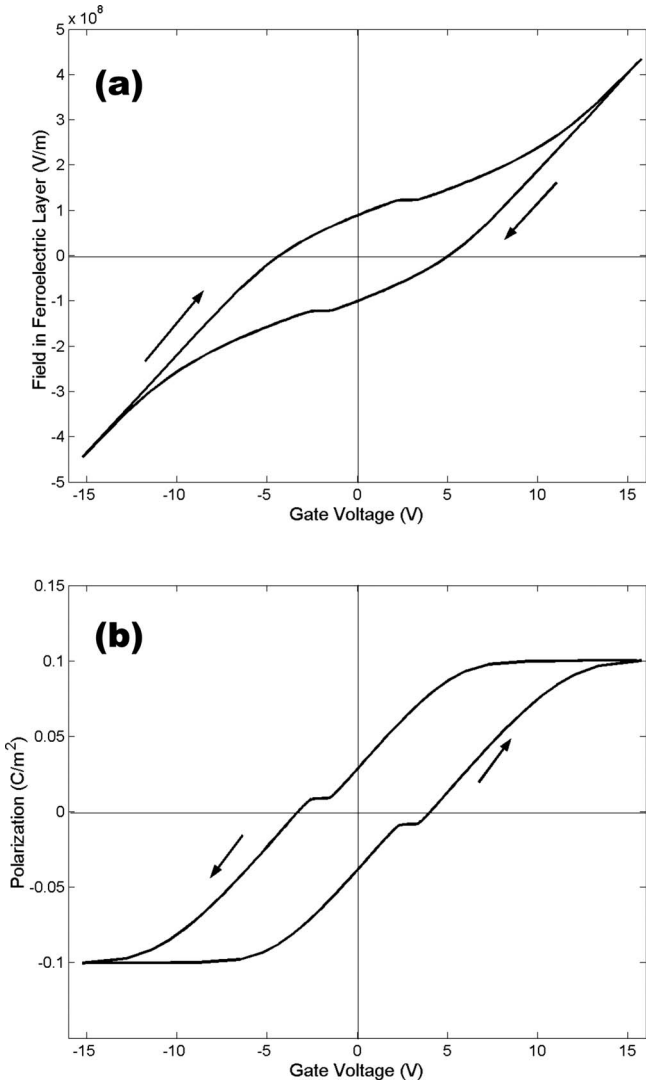

FIG. 3. State of the ferroelectric layer in the MFIS as the gate voltage is cycled: (a) electric field; (b) electric polarization.

The capacitance-voltage curve (Fig. 4) of the MFIS structure reveals the same features as those seen in a typical capacitance-voltage hysteresis loop for a metal-oxide-semiconductor device but with hysteresis due to the switch-

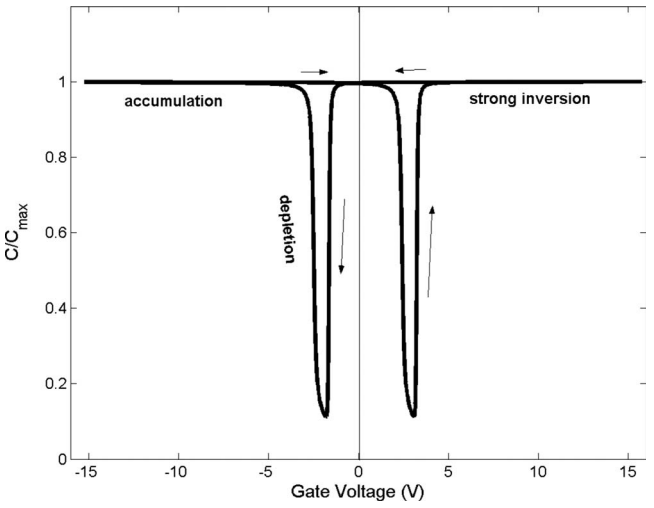

FIG. 4. Capacitance-voltage hysteresis of an MFIS capacitor.

able polarization of the ferroelectric. (If the capacitance is measured at a frequency higher than the reciprocal minority carrier response time, then the capitance stays low in inversion, as is often observed.[6,10]) Because of this hysteresis, the value of the flat band (the point where the silicon surface potential is zero) and threshold (boundary between depletion and inversion) voltages depends on the electrical history of the sample. The amount of hysteresis is quantified by the horizontal voltage shift, called the "memory window," where the maximum memory window is achieved when the polarization is saturated in both states. The maximum width of the memory window $\Delta V_{\mathrm{TH}}=2E_C d_F$ depends only on the properties of the ferroelectric layer. For the capacitance hysteresis loop in Fig. 4, which was obtained with a coercive field of 125 MV/m and ferroelectric film thickness of 10 nm, the memory window is 5 V. Although hysteresis is clearly shown in the *C-V* characteristics of the modeled MFIS capacitor, it is more difficult to achieve a significant zero gate bias on/off ratio in the source-drain current of a ferroelectric field effect transistor memory because of the requirement of strong inversion mode for source-drain current. The capacitance data do show that at zero bias one of the states remains in the strong inversion mode (high source-drain conductivity) while the other remains in accumulation. Thus, the model implies a measurable, nonvolatile on/off ratio in drain current for the corresponding ferroelectric field effect transistor.

In summary, we evaluated ferroelectric polymer based gate structures and determined that an operating voltage of 12 V is expected for a fully saturated 10 nm LB ferroelectric layer on a 5 nm insulating layer with a large dielectric constant. In the case of ferroelectrics that have large coercive fields, such as PVDF and its copolymers, a large memory window is easily achieved due to the large coercive field of the copolymer but this comes at the expense of large operating voltages. The copolymer's relatively low permittivity ($\varepsilon_f=10$) results in a smaller voltage drop across the buffer layer compared to perovskite ferroelectrics, which have a much higher dielectric permittivity ($\varepsilon_f=250$). The large remanent polarization is favorable because it can lead to higher drain-source currents in the Fe-FET structure. However, this also means that the ferroelectric cannot be fully polarized with low voltage operation, and less–stable subloops are present. Regarding the dielectric layer, it should have a high permittivity and breakdown field so that the ferroelectric can be polarized as much as possible without experiencing breakdown. This extra dielectric layer can reduce the current density through the capacitor stack and prohibit charge injection, particularly if the semiconductor and ferroelectric band gaps are a mismatch; but it separates the ferroelectric polarization from the compensation charge in the semiconductor, which is limited even without the buffer layer. Since both the properties of the ferroelectric and insulating layers prohibit saturation at low voltages in field effect devices based on ferroelectric polymers, much attention should be given to the retention times in such structures. It is interesting to note that a saturation voltage of 6 V has been achieved for a MFIS consisting of a 100 nm 77/23 copolymer spun film on a 3 nm Ta_2O_5 insulator with approximate dielectric constant of 25.[5]

ACKNOWLEDGMENTS

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