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High temperature superconducting Josephson junctions in a stacked bicrystal geometry

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Bicrystal grain boundary Josephson junctions were fabricated in a stack of two layers of $\text{YBa}_2\text{Cu}_3\text{O}_x$ separated by epitaxial SrTiO_3 . Weak link behavior was observed in the bridges formed in both layers that had similar shunted-junction characteristics but significantly different critical currents. Characteristic voltages up to 1.9 mV were measured at 4.5 K. The resonant structure was seen in the current–voltage characteristics of the upper-layer junctions, and interactions between junctions in the two layers were evident. © 1997 American Institute of Physics.
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We have fabricated grain boundary Josephson junctions in a stacked geometry using a multilayer of $\text{YBa}_2\text{Cu}_3\text{O}_x$ (YBCO) and SrTiO_3 (STO) on a 24° STO bicrystal substrate. The fabrication process we developed enables us to test the properties of each layer separately. Both YBCO layers showed weak-link Josephson behavior after patterning into bridge structures that spanned the bicrystal boundary. This is evidence that the grain boundary propagates vertically through the multilayer. The junctions in both layers have similar properties to those observed in single-layer films grown on a bicrystal substrate.

Grain boundary Josephson junctions in high temperature superconducting (HTS) thin films grown on bicrystal substrates^{1,2} have been studied extensively for fundamental science and for many applications. Bicrystal junctions can probe HTS material properties such as the nature of weak links^{3,4} and grain boundary coupling,⁵ penetration depth, and surface resistance.^{6,7} Our experiments allowed us to investigate the propagation of grain boundaries in a multilayer structure. This is an important material science issue itself because many practical devices require multilayer circuits consisting of crossovers, via connections,^{8,9} and stacked superconducting paths over bicrystal grain boundaries. Bicrystal Josephson junctions are promising in device applications such as superconducting quantum interference devices (SQUIDS)¹⁰ and voltage standards.¹¹ Our stacked grain boundary structure could be used to make devices such as low inductance dc SQUIDS, phase-locked Josephson junctions, and possible three-terminal devices. These potential circuits are possible because the junctions are separated only by the thickness of the insulating film.

Figure 1 is a representation of the wiring scheme of our multilayer test structure showing contacts made independent of each of the YBCO layers containing the desired grain boundary junctions. As in most HTS multilayer circuits, our test samples include crossovers and via connections that require low-angle edges to prevent unwanted grain boundary formation.¹² We have developed a technique for forming

such shallow edges using a proximity exposure process suitable for our relatively thick multilayer films. A $2\text{-}\mu\text{m}$ -thick positive photoresist layer is exposed in a contact mask aligner using a multistep procedure. The mask is aligned in contact, then backed off the photoresist by approximately $80\ \mu\text{m}$ and exposed. This results in a defocused image. After development, the photoresist pattern has low-angle edges of about 15° relative to the film surface. The underlying film is then etched by Ar ion milling, usually at normal incidence. The shallow edges in the photoresist pattern are reproduced in the film; they have a slight difference in angle due to the difference in the ion-milling rates of the photoresist and the film.

The YBCO and STO films were grown by KrF pulsed laser deposition. The YBCO films were deposited at $760\text{--}775^\circ\text{C}$ with $27\ \text{Pa}$ ($200\ \text{mTorr}$) of O_2 . The STO films were deposited at 740°C with $53\ \text{Pa}$ ($400\ \text{mTorr}$) of O_2 . The resistivity of the STO ranged from 2.8×10^5 to $4.6 \times 10^7\ \Omega\ \text{cm}$ on several test samples. Typical breakdown voltages ranged from 50 to 100 mV in films 180 nm thick. We fabricated our junction test sample on a 10 mm

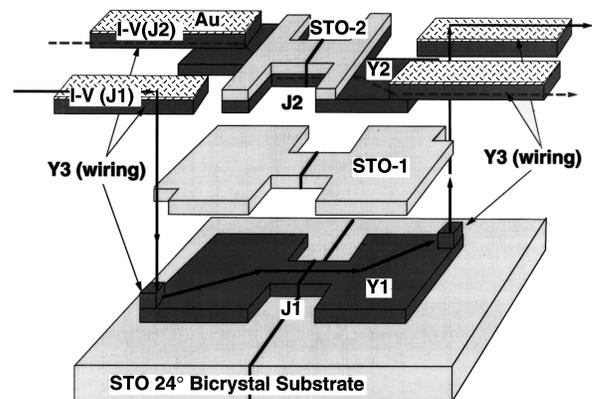


FIG. 1. A schematic drawing of the junction test structure. The drawing is not to scale but instead shows an exploded view of the scheme we used to contact the upper (Y2) and lower (Y1) YBCO layers independently using a single wiring layer Y3. The solid lines with arrows indicate the direction of current flow used to test junction J1 in Y1 and the dashed lines are the path for testing junction J2 in Y2.

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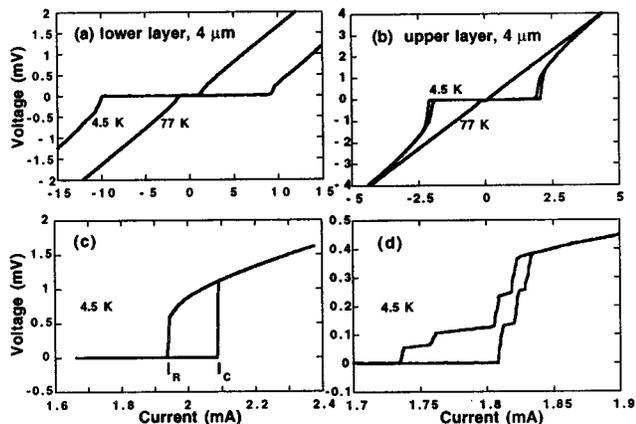


FIG. 2. Current–voltage characteristics of the stacked junctions. Note that the current and voltage scales are different in each of the plots. (a) The I – V curves of junction J1 in the lower YBCO layer Y1 at 4.5 and 77 K. (b) I – V curves at 4.5 and 77 K for J2 in the upper YBCO layer Y2. (c) Expanded current scale showing the hysteresis in J2 at 4.5 K. I_R is the return current and I_C is the switching current. (d) Expanded scale showing both hysteresis and self-resonant steps (no external microwaves applied) in another 4 μm junction in Y2 at 4.5 K.

$\times 10$ mm STO bicrystal with a misorientation angle of 24° . We first deposited a four-layer stack composed of 180 nm YBCO (Y1 in Fig. 1), 180 nm STO (STO-1), 180 nm YBCO (Y2), and finally 60 nm STO (STO-2). The STO-2 layer served as a protecting cap for the layers below and as a seed layer for subsequent epitaxial films.¹³ This four-layer film was patterned as described above to form seven isolated $60 \mu\text{m} \times 100 \mu\text{m}$ rectangles that cross the grain boundary in the substrate and that have low-angle edges. After the ion milling, the photoresist was removed by ultrasonic cleaning in acetone and by oxygen plasma ashing. Another layer of 180 nm of STO (STO-3, not shown in Fig. 1), was deposited after a final cleaning by low voltage ion milling. This STO layer was used to insulate the exposed edges of Y1 and Y2 in the rectangular stacks. The Y2 layer was ion milled to isolate Y1 as indicated by the corner cutouts in the schematic of Fig. 1. Openings were made through STO-3, STO-2, Y2, and STO-1 by ion milling at 45° through a low-angle resist mask. Next, after the removal of photoresist and cleaning of the chip, a third layer of 180 nm of YBCO and 60 nm of Au (Y3 in Fig. 1) was deposited and patterned to provide independent superconducting contacts to Y1 and Y2 in the stacks. On the four-layer stacks only the openings to Y1 and Y2 were covered by the Y3 layer after patterning by ion milling. After the photoresist was removed, the sample was patterned for the last time to form 4- and 8- μm -wide microbridges across the grain boundary. At this stage of the process sharp edges are desired on the sides of the bridges so that the two layers have the same cross-sectional area and the junction thickness is approximately uniform across its width.

We will now discuss the results of electrical characterization of the junctions in the two different layers. The current–voltage (I – V) characteristics of this system are rich in features such as hysteresis, resonances, and coupled-junction Shapiro steps. Figure 2(a) shows the I – V characteristics at 4.5 and 77 K of a 4- μm -wide junction J1 in the Y1

layer. The I – V characteristics of J2 (in the Y2 layer directly above J1) are shown in Fig. 2(b). Both J1 and J2 showed simple resistively shunted junction (RSJ) behavior¹⁴ at higher temperatures, as seen in the 77 K data of Figs. 2(a) and 2(b). The normal resistances are approximately independent of temperature, and no excess current is apparent in the I – V curves. At low temperature their I – V characteristics deviated from the simple RSJ model curves, especially as seen in Fig. 2(a). This can be qualitatively explained in terms of junction width. The simple RSJ model only applies to pointlike junctions with a width $W < 4\lambda_J$, where $\lambda_J = (h/4\pi e \mu_0 J_c t)^{1/2}$ is the Josephson penetration depth¹⁴ and t is roughly twice the London penetration depth λ_L . Typical values for our YBCO films are $\lambda_L = 200$ nm at 4.2 K and 380 nm at 77 K. We obtain the λ_J of J1 to be $0.22 \mu\text{m}$ at 4.5 K and $0.44 \mu\text{m}$ at 77 K, and the λ_J of J2 to be $0.47 \mu\text{m}$ at 4.5 K and $1.11 \mu\text{m}$ at 77 K. The widths ($4 \mu\text{m}$) of J1 and J2 are less than or approximately equal to $4\lambda_J$ at 77 K, but much bigger than $4\lambda_J$ at 4 K. Therefore, we expect deviation from simple RSJ behavior at low temperature; this would be apparent in the microwave and magnetic field response of the junctions.

We observed hysteretic I – V characteristics in both J1 and J2 at 4.5 K. This results in part from the relatively large capacitance due to the STO substrate and the STO insulating films.¹⁵ The expanded scale of Fig. 2(c) shows the hysteretic behavior of J2 at 4.5 K. The return current I_R is 1.89 mA and the I_C is 2.12 mA. From the relation between I_R/I_C and the McCumber parameter $\beta_C = (4\pi e/h)I_C R_N^2 C$ as shown in Ref. 16, we obtain a value of $\beta_C = 0.9$ for J2 at 4.5 K. This in turn gives us the capacitance C of J2 of approximately 2×10^{-13} F. This inferred capacitance is the parallel combination of the intrinsic capacitance of the junctions and the additional capacitance due to the leads and the STO layers. An accurate estimate of the lead capacitance requires electromagnetic analysis of the four-layer structure. This will be needed to extract an estimate for the relative dielectric constant of the STO and will be the subject of future work.

We observed clear self-resonant steps in the I – V characteristics for a wide temperature range from 4.5 to 60 K in some of the junctions in the Y2 layer. Figure 2(d) shows the I – V characteristic at 4.5 K of one junction in the Y2 layer without external microwave radiation or applied magnetic field (although some trapped flux in the YBCO films may be present which would produce a small dc field). Hysteresis is evident, and we can see a series of current steps at voltages of 60, 120, 230, and 360 μV . These steps are due to resonances in the circuit, with a fundamental frequency corresponding to the 120 μV step. The 60 μV step then corresponds to a 1/2 harmonic. From the Josephson relation $f = (2e/h) V$, we obtain a fundamental frequency of 58 GHz. The current step heights vary with temperature, but their voltage positions and therefore the resonance frequencies remain unchanged from 4.5 to 60 K. The resonance frequencies are independent of the junction width; both 4- and 8- μm -wide junctions show a similar structure in their I – V curves. The origin of the resonances is still under investigation. This independence of frequency to junction width probably rules out long junction modes such as zero-field steps and Fiske modes.^{7,14,17,18} The large relative dielectric con-

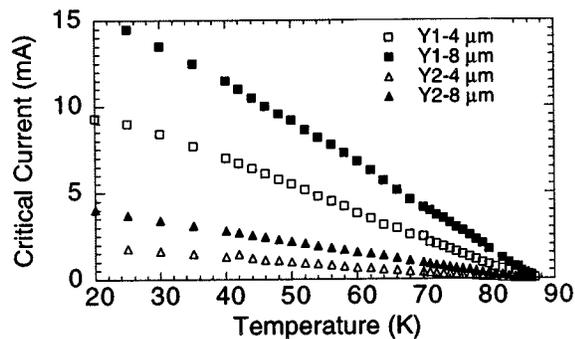


FIG. 3. A family of I_C vs T curves: The triangles correspond to a 4 and a 8 μm junction in layer Y2 and the squares to junctions in layer Y1. The closed symbols are for the 4- μm -wide junctions in both layers and the open symbols are the data for the 8- μm -wide junctions.

stant ϵ_R of the STO makes either a lumped low contraction LC resonance or a transmission line resonance between YBCO layers a likely candidate as the cause of the observed behavior.

Our test sample is composed of seven stacked junction pairs, four 8- μm -wide junctions, and three 4- μm -wide junctions. The $I_C(T)$ dependences of four junctions in two stacked pairs of 4 and 8 μm in width are shown in Fig. 3. The square symbols are for the Y1 layer and the triangular symbols for the Y2 layer. The closed symbols are for the 4 μm junctions and the open symbols for 8 μm junctions. Junctions in both layers and at both widths showed similar linear I_C - T dependence. The critical currents of the Y2 junctions are a factor of 4–6 lower than those of the Y1 junctions directly below them even though the width and thickness of each junction in a stacked pair are the same. A similar reduction in I_C was observed in bicrystal grain boundary junctions grown on buffer layers.¹⁹ The reduction in I_C is accompanied by a corresponding increase in R_N , so the resulting $I_C R_N$ products are much more similar than either I_C or R_N alone. At this point, it is not clear whether the lower I_C in the Y2 layer is caused by differences in the grain boundaries in the two layers or by a difference observed in the Y2 film quality. We measured a multilayer film grown on a STO substrate (without a bicrystal boundary) under the same conditions as our junction samples and patterned it with same process. The critical current density J_C of the second YBCO layer was several times lower than that of the first YBCO layer. We have since determined that by changing the deposition conditions we can reduce the difference in J_C to less than a factor of 2.

We have also observed interactions between junctions in a stack. In this experiment, the junction in Y1 is biased at a fixed current above I_C , and the Y2 junction is swept; Shapiro steps are evident in the I - V characteristic of the swept junction at the voltage of the Y1 junction. This is presumably due to capacitive coupling of the Josephson oscillations through the STO. Steps were seen up to 2.8 mV at 20 K and

to 0.5 mV at 77 K. This observation implies that the physical proximity of the two junctions in each stack can lead to complex and potentially useful device behavior. A more detailed study of this effect is underway and will be reported elsewhere. This type of sample has allowed us to fabricate compact, very low inductance dc SQUID interferometers.

In conclusion, we report what we believe is the first successful fabrication and testing of bicrystal grain boundary junctions stacked one above the other. Junctions in both layers behave similarly to those reported for grain boundary junctions in a more conventional geometry. The two layers have different I_C and R_N values (comparing pairs of junctions in stack), but the $I_C R_N$ product is approximately the same. The difference between Y1 and Y2 junctions therefore may be due to an effectively different cross-sectional area. This junction geometry and the fabrication process can be used to make novel and as-yet untested HTS device structures.

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