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We report electrical characterization of memory elements consisting of a p-type silicon field-effect transistor incorporating a ferroelectric polymer Langmuir–Blodgett film into the gate insulator to produce bistability through polarization hysteresis. The thin gate insulator, consisting of a 10 nm thick silicon oxide layer and a 35 nm thick ferroelectric polymer film, enabled bistable operation at 4 V. Device hysteresis as a function of gate voltage was evident both in the device capacitance, which was measured between the gate and drain, and in the source-drain conductance. The ferroelectric film polarization was not saturated, even up to operating voltages of 10 V. This is likely the reason for the short state retention of less than 10 s at room temperature. The hysteresis vanished as the sample was heated toward the ferroelectric-paraelectric phase transition temperature, showing that the bistability was due to ferroelectric polarization reversal. © *2010 American Institute of Physics*. [doi:10.1063/1.3437638]

If the gate dielectric of a conventional metal-oxide-semiconductor field effect transistor (MOSFET) is replaced by a ferroelectric material, a so-called ferroelectric FET (FeFET) is obtained. The reversal of polarization in the ferroelectric layer is used to alter the resistance of the semiconductor source-drain channel, which defines the computational "0" and "1." The ferroelectric film state is stable even without power, making the FeFET a versatile nonvolatile memory element.[1] Currently, available ferroelectric memories use a switchable capacitor design. The state of a bit is set with a voltage pulse and read out by applying another voltage pulse and measuring the switching current. This scheme has several drawbacks. In particular, it requires four to six elements per bit, taking up much space on the chip, and readout is destructive, so that it is slow and requires excess energy to operate. The advantages of the FeFET include a small footprint (only 1 transistor per bit), fast read, write and erase cycles of a nanosecond or less, low power consumption, and long device lifetime. Surprisingly, although the development of the first FeFET goes back to 1963,[2] there is still no commercial product available up to now. So far, most studies of FeFETs have focused on inorganic complex oxide and fluoride ferroelectrics, e.g., $PbZr_xTi_{1-x}O_3$, $SrBa_2Ta_2O_9$, or $BiMgF_4$, on a silicon complementary MOS platform.[1] One of the technical difficulties with these materials is due to interdiffusion and chemical reaction between the stack interfaces at the high deposition temperatures and high oxygen pressures used for deposition of the ferroelectric film. These processes produce poorly defined interfaces and uncompensated trap charges, thus, reducing the performance, reliability, and longevity of devices. The incorporation of an additional high-k oxide buffer layer to make the metal-ferroelectric-insulator-semiconductor (MFIS) stack structure has partially mitigated these problems, at the cost of increased fabrication complexity.[3] Moreover, the insufficient compensation of the ferroelectric bound charge on the semiconductor side leads to a high depolarization field that destabilizes the film polarization[4] and leads to electron injection. Both mechanisms tend to make the device states indistinguishable and are likely responsible for the limited FeFET state retention times of a few days or less.[5–7]

Ferroelectricity is found in various material classes besides complex oxides. One promising material class is ferroelectric polymers, such as polyvinylidene fluoride (PVDF) and its copolymers with, e.g., trifluoroethylene, P(VDF-TrFE).[8] Ferroelectric polymers are chemically benign and do not require high temperature deposition and processing methods. They are also inexpensive, easily handled, and thin films are readily fabricated with common solvent methods. Further, the low dielectric constant of order 10 and low saturated polarization of approximately 0.1 C/m^2 make the material appropriate for incorporation within FeFET devices on a silicon platform. Despite an encouraging early demonstration of capacitor and FeFET memory elements based on P(VDF-TrFE),[9] there has been little work on this technology until a few years ago.[10,11] More recent work takes the promising step of integrating the ferroelectric polymer

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with organic semiconductors.[12–19] The low processing temperatures for the polymer films, deposition at 25 °C and annealing at 130 °C, should have no deleterious effects on the semiconductor and metal components of the device. This is an important advantage compared to oxide ferroelectrics, which require high temperature processing in oxygen to optimize the composition and structure of the ferroelectric layers. Copolymers of PVDF are thermally sensitive, however, with melting points in the range 145 to 220 °C,[20] so standard MOS procedures need to be modified for compatibility reasons during device fabrication.

One of the drawbacks of PVDF and its copolymers is the high coercive field, the minimum electric field required to reverse the polarization state. With coercive fields of 50 MV/m and higher,[21] films must be quite thin, less than 100 nm, to allow for operation voltages below 5 V. The early devices,[9] for example, required up to 200 V to operate, while the more recent examples still require 30 V or more.[11–14,16–18,22] A proven means of making ultrathin films of P(VDF-TrFE) is Langmuir–Blodgett (LB) deposition on silicon wafers, which has produced ferroelectric films as thin as one nanometer[23] and nonvolatile memory devices operating at less than 10 V.[18,24–26] This report describes the successful low-voltage operation of a silicon-based FeFET nonvolatile memory device with a gate insulator consisting of a 35 nm thick P(VDF-TrFE) LB film and a 10 nm thick SiO_2 layer, operating in the low-voltage range between ± 5 V.

The FeFET devices were fabricated on Silicon (100) oriented, p-type (boron, concentration $\approx 4\times 10^{15}$ cm^{-3}), 6 in. wafers. First, the drain and source regions 300 by 300 μm were defined by photolithography. Then, As^+ dopants were implanted into the source and drain regions using an Axcelis Ion Implanter with an accelerator energy of 30 keV. The simulated ion concentration depth profile for the applied parameters predicted a donor concentration of 2×10^{20} cm^{-3} and a maximum ion penetration of 80 nm within the source and drain regions. After implantation, the wafer was cleaned by using the RCA cleaning procedure for organics.[27] An annealing step at 1000 °C in a nitrogen atmosphere was used for 1 min to activate the ions. After an additional cleaning procedure, an SiO_2 gate oxide was grown at 700 °C for 1 h in O_2 using a wet oxidation process followed by a forming gas (N_2H_2) annealing step at 450 °C for 15 min to passivate dangling bonds, which otherwise can act as charge traps. The thickness of the SiO_2 layer was determined by ellipsometry to be approximately 10 nm. The source and drain contacts were fabricated by first defining the contact area with photolithography, etching with buffered HF solution to remove the SiO_2 layer, and depositing the platinum contacts by sputtering. The remaining photoresist and excess platinum were then washed off. By these means, FETs with different channel areas were fabricated lacking only the ferroelectric film and gate contact. The 6 in. wafer was then cut into 1 cm^2 pieces.

The photolithography, implantation, and high temperature MOS processing steps were completed before deposition of the temperature-sensitive ferroelectric copolymer. The ferroelectric film consisted of a random copolymer of 70% VDF and 30% TrFE with a weight-averaged average molecular weight of 100 000. It was deposited directly on the prepared silicon wafer by horizontal LB deposition from an ultrapure water (18 MΩ cm) subphase at a surface pressure of 5 mN/m, as describe in greater detail elsewhere.[28] The films were formed from 25 LB transfers, which under these conditions produces films with thickness 44 ± 2 nm.[29] The samples were subsequently annealed at 130 °C for 1 h to improve the crystallinity of the copolymer. Au gate electrodes with various dimensions were deposited by vacuum evaporation through a shadow mask to complete the Au/PVDF/SiO_2/p-Si stack. The inset diagram in Fig. 1 shows the cross-section of the device.

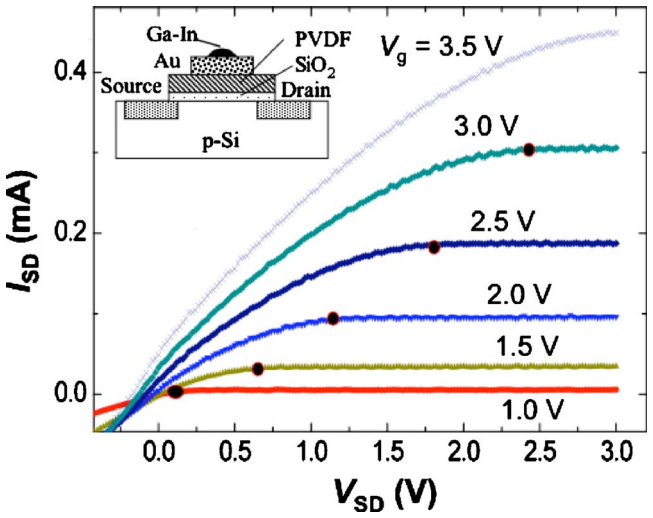

FIG. 1. (Color online) Source-drain current I_{SD} curves for an Au/PVDF/SiO_2/p-Si FeFET are shown with their dependency on the gate voltage values as shown. Inset: FeFET device diagram.

For electrical characterization, a low-resistance side contact was made to the silicon. Both top and side electrodes were connected via gold probe tips. The Au top electrode was first covered with a liquid metal GaIn eutectic, which was contacted with a needle. This method allows minimizing mechanical stress on the polymer film during electrical characterization. The FeFET measurements were performed with a semiconductor parameter analyzer at room temperature in a dark environment (a shielded metal box).

The FETs exhibited excellent current-voltage characteristics for gate voltage V_g ranging from 0 to +3.5 V, as shown in Fig. 1, for a channel area of 25×25 μm^2. The source-drain current I_{SD} increased linearly with the source-drain voltage V_{SD} at first and then tended toward saturation. The flat saturation currents are an indication of low leakage current between gate electrode and substrate and means that the PVDF/SiO_2 gate double layer is highly resistive.

The state bistability of the FeFET is best probed by measuring the source-drain current I_{SD} as the gate voltage V_g is cycled, while the source-drain voltage is kept low, in the linear I_{SD} versus V_{SD} region. Figure 2 shows the growth of hysteresis in the source-drain conductance with increasing amplitude of the gate voltage V_g. The hysteresis is due to the cycling between two opposing polarization states of the ferroelectric film. Although a symmetric gate voltage V_g cycle of up to ± 6 V was applied, for simplicity only the

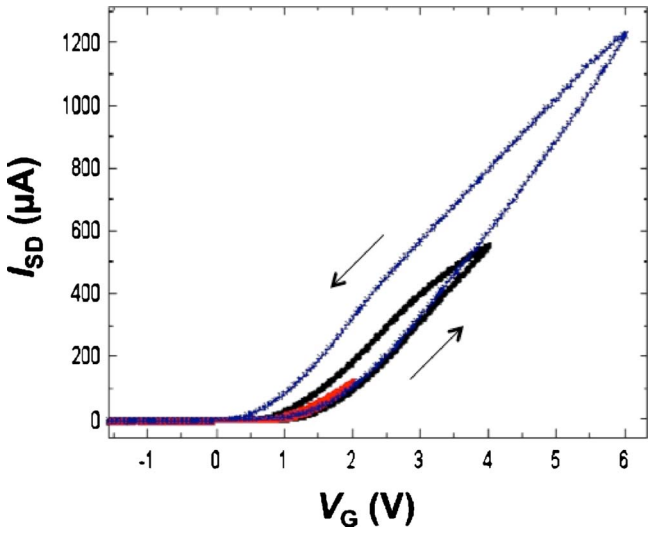

FIG. 2. (Color online) Source-drain current I_{SD} vs applied gate voltage V_g for an Au/PVDF/SiO_2/p-Si FeFET for different maximal gate voltages. The gate voltage was cycled between ±2, ±4, and ±8 V. The source-drain voltage was V_{SD}=0.1 V.

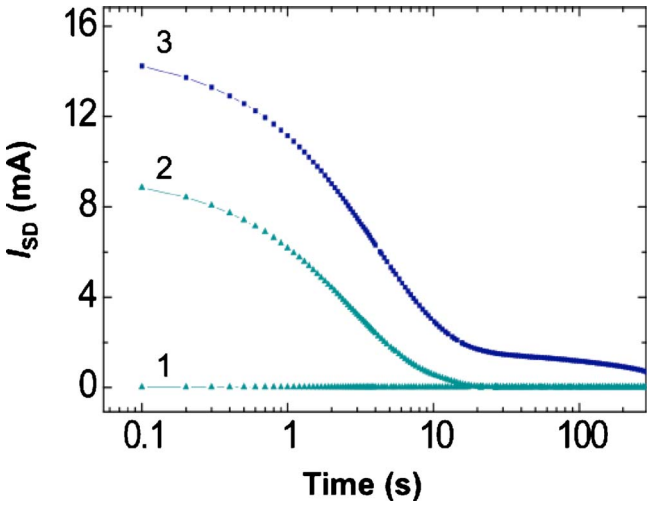

FIG. 4. (Color online) Source-drain current I_{SD} measured at zero gate bias and V_{SD}=0.1 V after setting the device state with a gate bias of ±5 V. Curve 1 was measured after applying a gate bias of −5 V for 2 min. Curves 2 and 3 were measured after applying a gate bias of +5 V for 2 min and 20 min, respectively.

interval between −1.5 V and +6 V is shown because there was negligible conductance with negative gate bias. A small V_g sweep of ±2 V produces a very small hysteresis loop (the small center loop in Fig. 2) with width < 100 mV whereas a large V_g sweep ±14 V results in a width of 3 V (the largest loop in Fig. 2). The width of the hysteresis loop is called the memory window and is one of the most important characteristics of an FeFET memory element. The memory window is also evident in measurements of device capacitance C versus gate voltage V_g as in an MFIS,[24] as shown in Fig. 3. Accumulation is attained at negative gate bias, resulting in a high device capacitance, while depletion is achieve at positive gate bias, resulting in low capacitance. The cross-over between accumulation and depletion is shifted from zero gate bias by the polarization state of the ferroelectric film. The MFIS memory window increases linearly from 0.15 to 1.3 V as the gate voltage cycle amplitude increased from ±1 V to ±6 V, as shown in Fig. 3. A larger memory window indicates higher remanent polarization in the ferroelectric film.

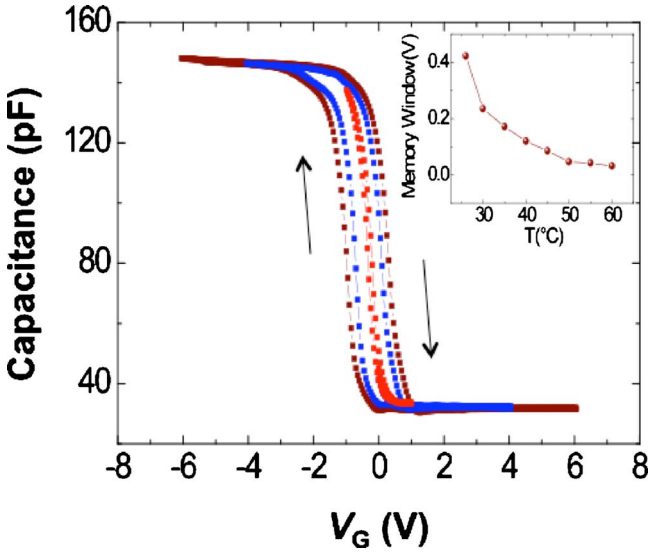

FIG. 3. (Color online) Capacitance-voltage hysteresis loops of a Pt/PVDF/SiO_2/p-Si gate MFIS stack diode measured with gate voltage sweeps over ±1, ±4 and ±6 V at a rate of 0.05 V/s. The measurement frequency was 100 kHz. The inset shows the width of the memory window as a function of temperature for gate voltage sweeps over ±5 V.

A large memory window, however, is not sufficient for practical FeFET operation. The state retention, i.e., the capability to maintain either the "on" or "off" state for a sufficiently long time, is another important issue. State retention in FeFETs can be limited by instability in the ferroelectric film polarization or by charge leakage and trapping in the insulating layers, or both. The state retention in the polymer FeFET was measured by monitoring the source-drain current I_{SD} (for V_{SD}=0.1 V) at zero gate bias after setting either the on or off states with ±5 V pulses of duration 2 or 20 min. The on state showed retention times of only a few minutes after state-setting bias voltage pulses of +5 V for 2 or 5 min, as shown in Fig. 4. Relaxation of the remanent polarization would reduce the source-drain conductance but so would leakage and charge trapping in the insulator or ferroelectric layers, and therefore, retention measurements alone are not sufficient to identify which of these mechanisms is dominant. An appreciable source-drain current will only be measured when the condition of strong inversion at the silicon surface is met. Once the ferroelectric polarization in the off state falls so that this condition is no longer met, the on and off states of the FeFET are indistinguishable even if the on state is completely stable. Therefore, the capacitance state retention study that was previously reported[24] is better suited for a discussion of the dominant mechanisms for state relaxation. Since the capacitance hysteresis (Fig. 3) is highly symmetric we can conclude that charge trapping is not significant and that state retention is primarily limited by polarization stability.[24,30] (Charge injection is a much bigger problem with oxide ferroelectrics, which are in effect semiconductors.[31]) Nevertheless, this hypothesis needs further study to clarify the mechanisms for retention in FeFETs,

and properly prescribe a remedy. Polarization stability is best improved by providing better charge compensation at the surfaces of the ferroelectric film. This can be accomplished by further reducing the thickness of the oxide layer so that its capacitance is at least ten times that of the ferroelectric film.

In summary, we fabricated ferroelectric FETs with the copolymer P(VDF-TrFE) integrated in the gate-stack of a p-type silicon FET. The copolymer film was deposited by the LB technique to produce a thin high-quality ferroelectric film. Functional bistable FeFETs were operated with low gate bias voltage ranges from ± 2 to ± 6 V. A hysteresis in the I_{SD} versus V_g characteristics was observed which represented the remanent polarization of the ferroelectric polymer. We observed retention times of less than 10 s, which likely is limited by incomplete polarization saturation.

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