June 1997

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An Improved Multi-layer Fabrication Process for $YBa_2Cu_3O_{7-x}$-based Circuits*

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***Abstract*—Improved via connections in structures of $YBa_2Cu_3O_{7-x}/SrTiO_3/YBa_2Cu_3O_{7-x}$ (YBCO /STO/ YBCO) multilayers have been made using a combined HF wet-etching and ion-milling process. The critical current density J_C of the via is as high as 2 x 10^6 A/cm^2 at 76 K, and is dominated by edge contacts in the *ab*-plane. YBCO and Sr_2AlNbO_6 (SAN) multilayer test circuits were also made with this process. The 4° crossovers in a SAN test chip had a critical temperature T_C of 88 K and J_C of 1.5 x 10^6 A/cm^2 at 81 K, very close to those of the planar film, showing no evidence of weak links in the YBCO crossing low angle SAN steps.**

I. Introduction

We describe improvements to a multi-layer circuit process using $YBa_2Cu_3O_{7-x}$ (YBCO) and epitaxial insulators $SrTiO_3$ (STO) and Sr_2AlNbO_6 (SAN). We reported earlier on a reproducible fabrication process which combines HF wet-etching and Ar^+ ion-milling for making HTS multilayer circuits [1]. The HF solution, which is highly selective for etching STO over YBCO, was used to form an STO pattern with controllable shallow slopes. The patterned STO layer, with photoresist removed, was used as a conformal ion-milling mask for etching the layers beneath it; as a result shallow slopes were also formed in the bottom layer. The YBCO/STO/YBCO multilayer test chips we made this way had crossovers with critical current density J_C above 1x10^6 A/cm^2 at 86 K, close to those of planar bottom and top YBCO layers. However, overall critical currents of the circuits were limited by the interlayer vias. In this paper, we present our recent results from a systematic study of via connections between the top and bottom YBCO layers and present data on two multilayer test chips with SAN insulation layers.

Multilayer circuits are required in many high temperature superconducting (HTS) devices such as the flux transformer of a dc SQUID and ramp-type Josephson junction circuits [2]-[6]. Such a circuit usually consists of paths in both bottom and top superconducting layers separated by an epitaxial insulator, crossovers, via connections, and other devices. It is important to form shallow slope edges in the base layer pattern of crossovers and via connections, so the films subsequently grown on the patterned base layer would maintain their epitaxy even over the edges [7], [8]. This is necessary to avoid degradation in superconducting properties and to limit flux noise [9]. Various methods have been reported to make shallow slope patterns in YBCO/STO/YBCO multilayer circuits [10]-[12]. Via connections usually limit the critical current (I_C) of a multilayer circuit, both because the growth of YBCO on exposed YBCO might not be ideal and because the critical current density (J_C) of YBCO is anisotropic, more than 10 times lower along the *c*-axis than in the *ab*-plane [13]. Another limitation to circuit design and fabrication is imposed by the use of STO as the insulator due to its very high dielectric constant and large dielectric loss at low temperatures, limiting it to low frequency uses. For high frequency HTS applications, one needs to find insulators with low dielectric constants and well-matched lattice parameters; a potentially good choice is SAN because it is lattice matched to YBCO [14] and has a relative dielectric constant of 10 [5].

II. Experimental

A. *Fabrication Overview*

The details of our YBCO/STO/YBCO multilayer circuit process are described elsewhere [1]. In brief, we deposited *in situ* a bilayer of YBCO and STO on $LaAlO_3$ (LAO) by pulsed KrF laser ablation. The STO layer was patterned with positive photoresist and etched in a 3% aqueous HF solution at 23-25 °C. By controlling the soft-bake and hard-bake of the photoresist, the temperature and time of HF wet-etching, and the deposition conditions, we can reproducibly make slopes in the STO layer with 2-30° angles (relative to the film surface). After stripping the photoresist in acetone and an oxygen plasma etcher the film was ion-milled at 0° incident angle. Since the ion-milling rate of YBCO and STO in our process were similar to each other, the shallow slope profile in the STO was reproduced in the YBCO layer. The STO and YBCO thicknesses were chosen so that a thin seed layer of STO remains on the YBCO after milling [4]. Another layer of STO was then deposited on the ion-milled film as the insulator. The same HF wet-etching and ion-milling process was repeated to form the via connections. Because no photoresist was on the sample during ion-milling there was no problems with insoluble residues after patterning by ion-milling. Finally, a layer of YBCO and a layer of Au were deposited and patterned by ion-milling using a conventional photoresist mask.

Manuscript received August 27, 1996
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B. *Via Connections*

To investigate the most effective way for enhancing the current carrying capacity of via connections in HTS multilayer circuits, we designed a set of masks with three sets of via connections on a 12 mm x 12 mm LAO substrate. An optical micrograph of 3 sets of vias is shown in Fig. 1. The bottom YBCO/STO bilayer, consisting of 200 nm YBCO and 200 nm STO, was patterned by HF wet-etching and Ar^+ ion-milling as described above. The subsequent insulating STO layer was 240 nm thick. We opened the vias in the insulating STO layer by 3% HF wet-etching and then stripped the photoresist. The HF wet-etching was controlled to form a shallow slope, about 5° as measured by atomic force microscopy (AFM), in the STO layer. This insures that the YBCO film grown on the STO slope had a high enough I_C and presented no limit to the I_C of the via connections. We ion-milled the first set of vias for 1 minute just to expose and clean the bottom YBCO layer. The second set of vias was milled for 6.5 minutes to etch halfway into the bottom YBCO layer, and the third set of vias for 13 minutes to completely etch through the bottom YBCO layer and leave only the sloped YBCO edge along the perimeter of the vias exposed. A sketch of this process is shown in the inset to Fig. 2. The upper contact layer consisted of 200 nm of YBCO covered by 200 nm of Au.

The critical currents of these via connections were obtained using a 1 μV criterion. I_C was related to the ion-milling depth into the bottom YBCO layer. Figure 2 shows the I_C (T) curves of three 8 μm x 8 μm vias each from one of the three sets of vias mentioned above. Via (c), with the bottom YBCO layer completely ion-milled, had the highest I_C. Via (b), with the bottom YBCO layer milled halfway, had an I_C half of the I_C of via (c). Via (a), with the bottom YBCO layer exposed but not deeply etched, had a value of I_C one order of magnitude lower than that of via (c). This is clear evidence that I_C is dominated by the edge connection in the ab-plane.

The critical current of via (c) is 32 mA at 83 K,

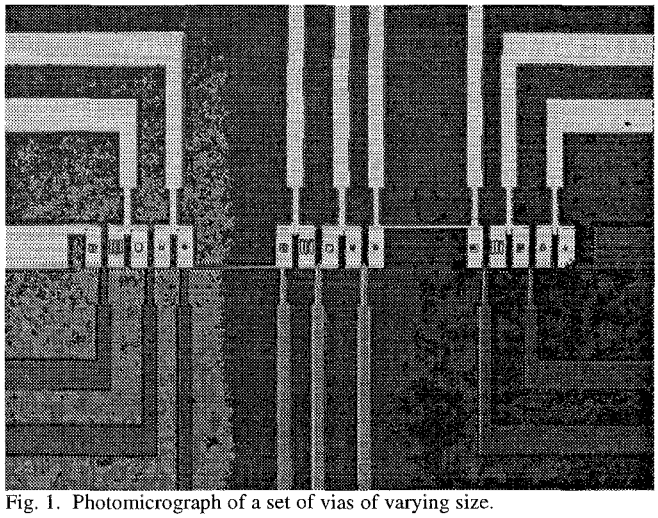

Fig. 1. Photomicrograph of a set of vias of varying size.

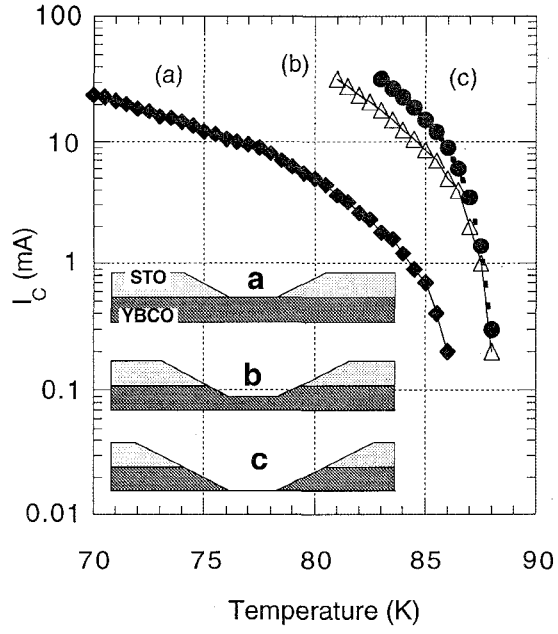

Fig. 2. The critical currents of vias: (a) milled only through insulator layer, leaving top surface of YBCO exposed; (b) milled halfway down through the lower YBCO layer; and (c) milled all the way to the substrate. The inset shows this progression schematically.

which corresponds roughly to a J_C of $7x10^5$ A/cm^2. J_C was calculated by dividing the I_C by the cross section formed by the thickness of the bottom YBCO layer and the perimeter of the via. There was some uncertainty in the via perimeter because of the corner rounding and undercutting from the HF wet-etching. We made another chip which includes a 10 μm wide wire in the top YBCO layer, 200 nm thick, connecting

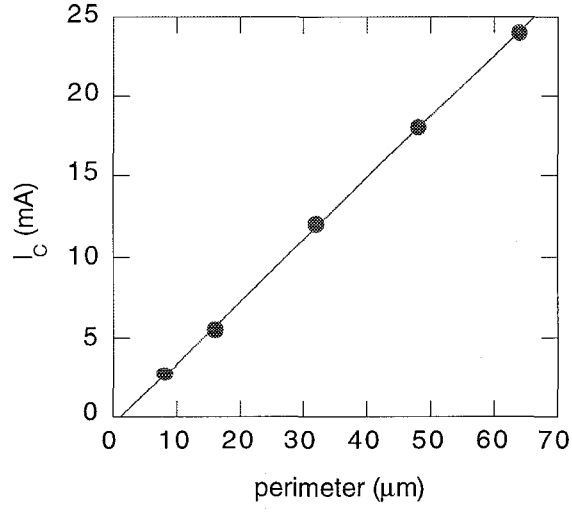

Fig. 3. Critical current vs. perimeter length of the via. J_C can be computed by dividing the critical current by the product of the perimeter length and the lower YBCO thickness; the linear fit gives $J_C = 1.9x10^5$ A/cm^2.

with the bottom YBCO layer, 100 nm thick, across one side of a 30x30 μm via ion-milled to the substrate The cross section of this edge connection was exactly 10 μm by 100 nm. At 76 K, I_C was 20 mA, corresponding to a J_C of $2x10^6$ A/cm^2 which is high enough for most practical applications although still somewhat smaller than the J_C of either layer (typically greater than $4x10^6$ A/cm^2).

To test the uniformity of the via connections made with our process, we made a test chip using a mask which includes ten 2 μm x 2 μm vias and one via each of 4 μm x 4 μm, 8 μm x 8 μm, 12 μm x 12 μm, 16 μm x16 μm, and 20 μm x 20 μm. The bottom and top YBCO layers are 200 nm and 250 nm thick respectively. After HF wet etching the 2 μm vias and the 4 μm via turned out to be circular due to the corner rounding and undercutting. The vias were milled to the substrate (as in via (c) above). The average I_C of the ten 2 μm vias was about 22 mA at 76 K, with a standard deviation less than 5%. Figure 3 shows I_C of the vias as a function of perimeter length at 86 K. As expected we see that I_C changes linearly with via perimeter.

C. *Multilayer Circuit with SAN Insulator*

We applied our improved process to the fabrication of an HTS multilayer circuit with SAN as the insulator. We first tested the HF wet etching and Ar^+ ion-milling conditions for SAN. The SAN etched very slowly in the HF but ion milled at a rate equal to that of STO. We can therefore treat a base YBCO/SAN bilayer in the same way as the bottom YBCO layer in a YBCO/STO/YBCO multilayer circuit, i.e. constructing a conformal STO pattern with shallow slope on top of the YBCO/SAN bilayer by HF wet-etching, and then ion-milling the chip to copy the shallow slope profile into the YBCO/SAN bilayer. The thickness of the STO is chosen so that no STO would remain after ion-milling.

We made a YBCO/SAN/YBCO multilayer test chip which had J_C lines in the top and bottom YBCO layers, crossovers, and via connections. All the YBCO, STO and SAN films were deposited by KrF laser ablation. First a YBCO/STO bilayer (100 nm YBCO, 120 nm STO) was patterned by our HF wet-etching and Ar^+ ion-milling process. A thin layer of STO, roughly 10-30 nm, was left on the YBCO layer as a seed for subsequent layers. The slope angle, as measured by AFM, is about 4°. Then a 200 nm insulating SAN layer was deposited at 750°C and 12 Pa oxygen pressure. In order to open vias through the SAN layer, another STO layer, 240 nm thick, was deposited and etched in a 3% HF solution at 25°C for about 2.5 minutes. After the photoresist was removed, the chip was ion-milled for 26 minutes to etch all the way to the substrate in the vias and into the SAN layer everywhere else. In the last step, the top YBCO (250 nm) and Au (200 nm) were deposited and patterned by conventional ion-milling.

We measured T_C and J_C of the components in this test chip. A 10 μm line in the top YBCO layer with one crossover had a T_C of 88 K, the same as that of a planar 10 μm line in the top YBCO layer. A 10 μm wide, 3 mm long zigzag line with 80 crossovers had a T_C of 87 K. Their J_C vs.

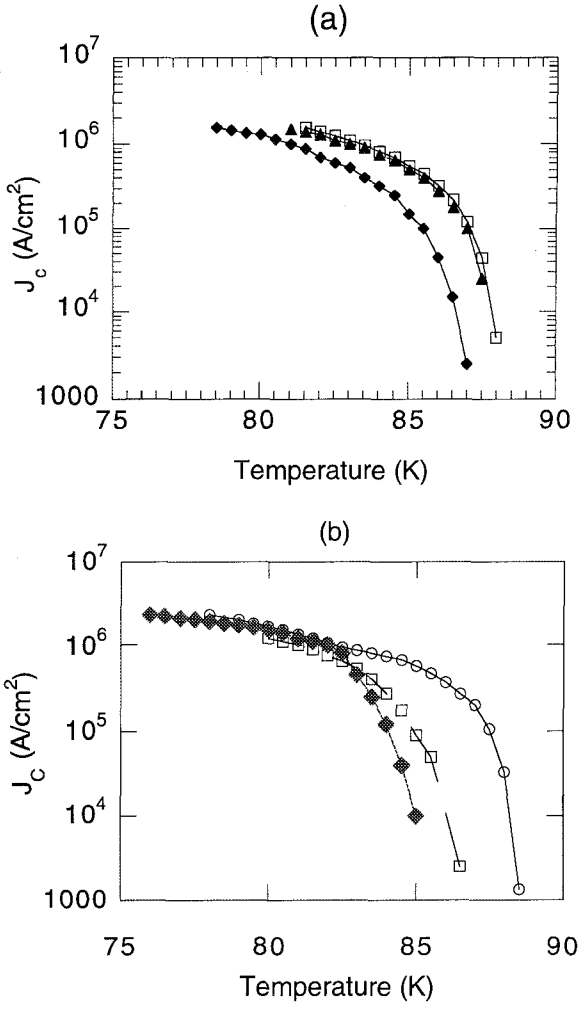

Fig. 4. (a) J_C of various structures on the first SAN test chip: (squares) no crossings, planar 10 μm strip, (triangles) a single crossover, and (diamonds) zigzag path with 80 crossovers. (b) J_C from second SAN test chip with long O2 anneal: (circles) lower YBCO layer, (squares) upper YBCO layer, and (diamonds) single 2 μm via.

temperature curves are shown in Fig. 4a. The J_C of one crossover is very close to that of the top YBCO layer, indicating that there is no weak link in the top YBCO layer across a 4° SAN step. The J_C of the zigzag line is a little lower, probably due to a low T_C or narrower region in its 3 mm path. The T_C of the bottom YBCO layer and the via connections for this chip were low, about 55 K. This is probably caused by the loss of oxygen during SAN deposition. A second chip was fabricated with a long O_2 anneal (10 h at 400 °C) after the SAN deposition; conditions, layer thicknesses, and slope angles were otherwise identical. The T_C of the lower YBCO was 89 K and the via I_C could now be measured at 76 K. The results are shown in Fig. 4b. The resistivity of the insulating SAN is about $2x10^{10}$ Ω-cm.

III. Discussion and Conclusions

The main contribution to the I_C of via connections in YBCO/STO/YBCO multilayer circuits comes from the edge

connection to the ab-planes. High via critical currents, 48 mA at 76 K in a 4 μm x 4 μm via for example, were achieved by ion-milling the bottom YBCO to the substrate, leaving only the edge along the perimeter of the vias for connection. The highest J_c for this kind of via connection was 2.1×10^6 A/cm^2 at 76 K, calculated from the cross section formed by the thickness of the bottom YBCO layer and the perimeter of the via. Since the dominant factor for the I_c of vias is edge connection to the ab-planes, it should be more effective to increase the via's perimeter than to enlarge the via's area in order to maximize its critical current.

Our process can also be used for the patterning of a variety of materials where controllable low angle steps are required, provided that their ion-mill rates are close to that of STO. A YBCO/SAN/YBCO multi-layer test circuit was made with the process. By forming a conformal shallow slope STO pattern on the SAN layer, we were able to etch low angle steps in SAN by ion-milling. The low angle YBCO crossover on SAN had a T_c of 88K and J_c of 1.5 $\times 10^6$ A/cm^2 at 81 K, very close to that of the top YBCO layer on the same chip. Vias on the second SAN chip had J_c approximately equal to the J_c of vias on the STO samples. This makes SAN, with its lower dielectric constant, a viable insulator candidate for YBCO multilayer circuits.

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