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Interactions Between Bicrystal Josephson Junctions in a Multilayer Structure

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***Abstract*-We have fabricated and studied a variety of devices based on stacked $YBa_2Cu_3O_x$ bicrystal Josephson junctions in a multilayer structure. The proximity of the junctions in the two layers produces a large number of effects based on interactions between the junctions. Voltage locking and current locking were observed in the stacked junctions. The voltage locking is due to the ac path provided by a $SrTiO_3$ layer between the stacked junctions. The current locking is likely the result of a Josephson vortex interaction.**

I. INTRODUCTION

We have studied multilayer high-T_C bicrystal Josephson junctions [1,2] and observed junction interactions in the form of voltage locking and current locking. In this paper we will show experimental evidence for these interactions and discuss possible mechanisms causing such effects.

Coupled Josephson junctions interact with each other, displaying voltage locking [3-5] and current locking [6-10]. In the case of two junctions in a circuit where the coupling is capacitive and/or inductive, the voltages of each junction are *pulled together* and can lock over a finite range of current bias. This is the result of the interaction of the high frequency currents arising from the ac Josephson effect in each junction. The study of voltage-locked junctions can help us understand the internal dynamics of the junctions (through modeling of circuit and junction parameters) and the layered structure of high-T_C materials. The coupling of junctions is the basis for applications such as voltage standards [11] and high frequency oscillators [12].

When two junctions are closely spaced, under the appropriate bias conditions the critical currents of the junctions are pulled together. This effect is called current locking and was first observed by Jillie *et al.* [6] in a system of two closely connected microbridges. Current locking was also observed in stacked Nb tunnel junctions, in which the junctions are parallel and connected by a thin superconducting Nb layer [8-10]. Current locking of this type can occur only when the distance between the junctions is comparable to the coherence length of the superconductor. Mutually reinforced depression of the order parameter is thought to be the basis for such current locking [7]. Other explanations such as inductive interactions between two junctions [10] and modulation of I_C of one junction by the radiation from the other junction [8] have been given for current locking.

II. EXPERIMENTAL

We first deposited a 4-layer stack of $YBa_2Cu_3O_x$ (YBCO) and $SrTiO_3$ (STO) films on a bicrystal STO substrate with 24° misorientation angle by KrF pulsed-laser ablation. The thickness of each of the YBCO films is about 0.19 μm, and the thickness of the STO layer between the YBCO layers is about 0.18 μm. After patterning the stack using a defocused exposure of photoresist (to produce sloped edges) and ion-milling, we deposited another layer of STO which covers the exposed YBCO edges. Then the sample was patterned again to expose the YBCO layers separately. Finally, another layer of YBCO was deposited and patterned, forming leads to the two YBCO layers at the exposed vias. The critical temperatures were measured to be 86.5 K for the bottom YBCO layer and 88.7 K for the top YBCO layer. This process allows us to study the junctions in each layer independently and to construct various devices. Details of the fabrication are reported elsewhere [1, 2].

The experimental vertical structures are shown in Fig. 1. Starting with a 4-layer stack, Fig. 1a, we can form the voltage-locking structure, Fig. 1b, in which the two junctions are biased independently, and the current-locking structure, Fig. 1c, in which the junctions are connected at one end by another YBCO layer and biased in series.

III. RESULTS AND DISCUSSION

A. Voltage Locking

With a sample such as shown in Fig. 1b, we observed

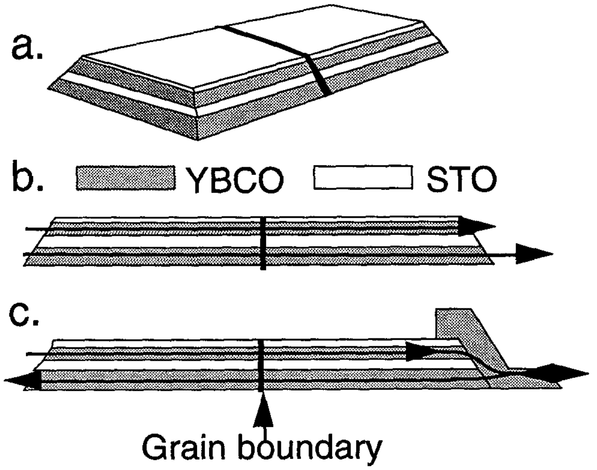

Figure 1. Vertical structures of samples used for voltage and current locking experiments.

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voltage locking between a pair of stacked Josephson junctions. In our experiment the bottom junction was biased at a fixed current above its critical current I_C (and therefore at a fixed voltage), and the bias current through the top junction was swept. When the current in the top junction is in same direction as the current in the bottom junction, the I-V characteristic of the top junction shows steps at the voltage of the bottom junction. Figure 2 shows a series of I-V characteristics of a top junction at 60 K. Both junctions are 4 μm wide and the I_C of the bottom junction is about 4-5 times higher than that of the top junction. Each of the curves is offset in the voltage axis for clarity. The step positions are precisely at the fixed voltage of the bottom junction, within the uncertainty of the measurements of approximately 1 μV. In Fig. 2 the step height decreases with increasing bottom junction voltage but does not monotonically decrease over a larger voltage range. We have seen a step disappear and reappear with increasing voltage at higher voltage ranges. The biggest step, measured when the bottom junction is biased at 0.1 mV, is about 0.11 mA. It is about 20 % of the I_C (0.54 mA) when $V_b = 0$. The highest voltage at which steps can be observed increases with decreasing temperature. Steps at 2.8 mV were observed at 20 K.

The voltage locking is presumably due to coupling of the Josephson oscillations between the junctions. The simplest coupling mechanism is through the capacitance between the YBCO layers separated by STO. When one junction is in the normal state, it produces an oscillating supercurrent which in turn affects the other junction through the STO layer, causing steps in its I-V curves. The STO has a dielectric constant greater than 500, so very large capacitances can result even with small overlap areas. Resonances in the junction stack and the wiring can also influence the range of voltages over which locking can be seen; geometric resonances can result in non-monotonic step height-vs.-voltage relations such as we observe. The capacitive coupling can be modeled using a circuit simulation including the interlayer capacitance. We are carrying out preliminary calculations using a commercial simulation package which includes Josephson junctions.

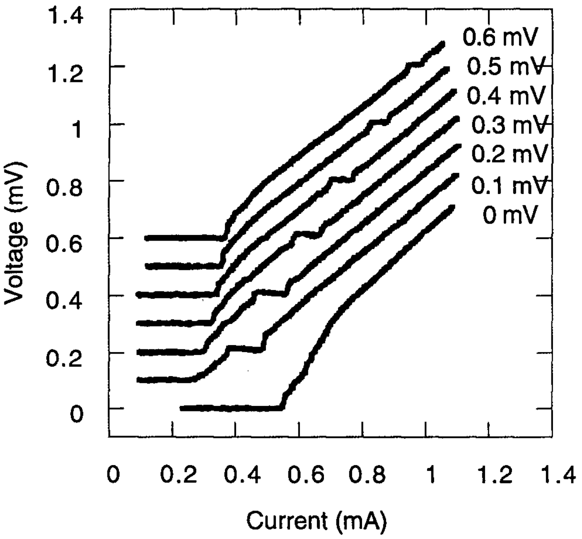

Figure 2. Voltage interactions. We show the I-V characteristics of a 4 μm wide top layer junction at 60 K with the bottom junction biased at 0, 0.1, 0.2, 0.3, 0.4, 0.5, and 0.6 mV. The curves are displaced upwards at 0.1 mV for clarity.

B. Current Locking

Critical current locking was observed in a stacked junction pair connected at one end, as shown in Fig. 1c. Swept bias current was passed through the two junctions in series, and the voltages across each junctions were recorded at the same time. The I-V characteristics at 77 K, 50 K, and 30 K of a pair of stacked junctions 40 μm wide are shown in Figures 3a, 3b, and 3c respectively. The voltages for the top junction are reversed, so that they can be seen more easily when plotted with the bottom junction. At 77 K the critical currents of the top and bottom junctions are different, 3.6 mA for the top junction and 3.9 mA for the bottom junction, as seen in Fig. 3a. As the temperature is lowered, the critical currents of the junctions get closer, and at about 53 K they became identical. The critical currents are locked at 16.5 mA at 50 K and 25.8 mA at 30 K. Note that while the critical currents are identical, the normal resistances are

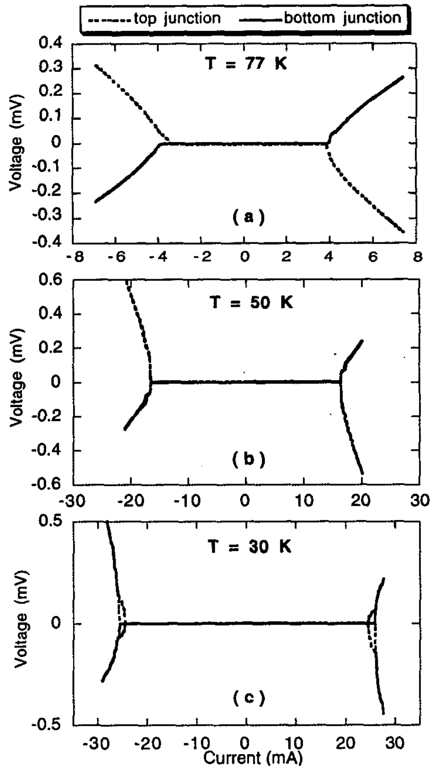

Figure 3. I-V characteristics of the top and bottom junctions in a 40 μm wide stack at (a) 77 K, (b) 50 K, (c) 30 K. The junctions are biased in series and the curves for the bottom junction have been reversed for visual clarity. Critical current locking is present at 50 K and 30 K. Hysteresis is evident at 30 K and the return currents are also locked.

different. Also, due to the high dielectric constant of STO and the large critical current at low temperature, the I-V characteristics of both junctions are hysteretic. As shown in Fig. 3c, when hysteresis appears in the locked junctions, both the critical currents and the return currents of the two junctions are identical.

When biased individually, each junction has a lower I_C than the locked I_C obtained when a bias current flows in series through both junction. The I-V characteristics of the top and bottom junctions were measured by passing the bias current through only the junction being measured while leaving the other junction idle. The locked critical current is higher at least partly because the self-fields of the junctions cancel each other when they are biased in series.

The strong current locking effects were not seen in narrower junctions (8 µm or less). To further study the current locking, we made a chip which includes junction patterns with different widths. An optical micrograph is shown in Fig. 4. The junctions stacks are 5 µm, 10 µm, 20 µm, and 40 µm wide. Critical current locking was observed in the 10 µm, 20 µm, and 40 µm stacks. The 5 µm junction stack showed no current locking even when the temperature was lowered to 4.2 K. The temperature dependence of I_C measured with series biasing in the 10 µm, 20 µm, and 40 µm stacks are shown in Fig. 5. At high temperature the two junctions in a stack have different I_C values. Below an onset temperature, which increases with the width of the stack, the I_C of each junction become identical and remain locked down to 4 K. The starting temperature of current locking is 76 K for the 40 µm stack, 72 K for the 20 µm stack, and 64 K for the 10 µm stack.

Our multilayer junction system is significantly different from the other systems displaying current locking discussed in the introduction. The two bicrystal junctions as shown in Fig. 1 are connected by a 160 µm long YBCO film, which is much longer than the YBCO coherence length. The long superconducting connection easily rules out any order parameter interaction. However the junctions are very closely spaced vertically, with a STO layer 0.18 µm thick between them. Since the junctions are formed through the upward propagation of the single grain boundary in the bicrystal substrate, the junction planes reside in the same plane as the substrate grain boundary. Thus, some form of inductive or capacitive interaction is possible. However, the locked critical currents are larger than the critical currents of the individually measured junctions, counter to the expected result from a high frequency interaction.

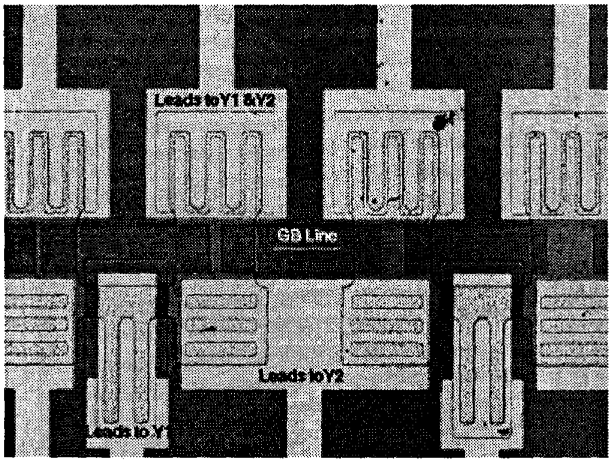

Figure 4. An optical micrograph of the microbridge junction stacks for current locking measurement. The width of the junction stacks are 5, 10, 20, and 40 µm from left to right and their length are all 40 µm. The grain boundary crosses the middle of the microbridges. The top and the bottom YBCO layers are connected at the upper end of the stacks by a YBCO/Au bilayer film ("Leads to Y1&Y2"). Separate leads to the top and to the bottom YBCO layer can be seen at lower end of the stacks ("Leads to Y1(Y2)").

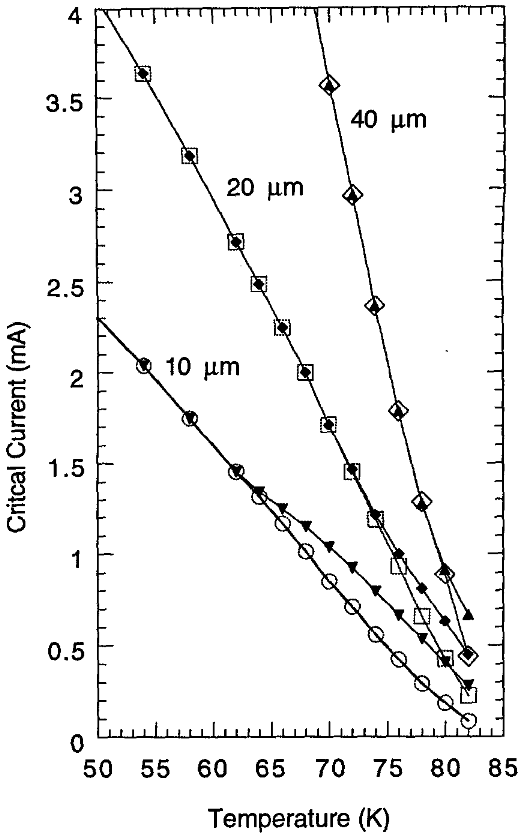

Figure 5. Critical current as a function of temperature for the stacked junctions in series. The open circles is for the 10 µm, the open squares for the 20 µm, and the open diamonds for the 40 µm wide top junctions. The filled inverted triangles is for the 10 µm, the diamonds for the 20 µm, and triangles for the 40 µm wide bottom junctions.

Magnetic field penetrates a wide junction in the form of Josephson vortices whose sizes are defined by the Josephson penetration depth λ_J. In our system the Josephson vortices in the two junctions would align due to the unique geometry. The qualitative observation that the onset temperature for current locking increases with junction width supports this idea because λ_J increases with temperature. More detailed investigations such as field dependence of the current locking and the accurate determinations of λ_J of the junctions in each layer are under way to confirm this explanation. Our measurements of λ_J will appear elsewhere; there is at present agreement between the temperature dependence of the current locking and that of λ_J.

IV. CONCLUSIONS

The voltage locking is due to capacitive coupling between the junctions through the STO layer which has a high dielectric constant. Preliminary circuit modeling supports this hypothesis. We are presently exploring the hypothesis that the current locking arises from Josephson vortex interactions between the stacked junctions. The appearance of a Josephson vortex depends on the ratio of the junction width to the Josephson penetration depth, width divided by injection current, and the magnetic field (both self field and external field combined). The temperature at which these vortices can exist is consistent with the observed onset temperature of current locking.

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