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Electrical properties of ZnO–$BaTiO_3$–ZnO heterostructures with asymmetric interface charge distribution

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We report on capacitance-voltage, current-voltage, Sawyer–Tower, and transient current switching measurements for a ZnO–$BaTiO_3$–ZnO heterostructure deposited on (001) silicon by using pulsed laser deposition. The triple-layer structure reveals asymmetric capacitance- and current-voltage hysteresis and cycling-voltage dependent Sawyer–Tower polarization drift. We explain our findings by coupling of the ferroelectric ($BaTiO_3$) and piezoelectric (ZnO) interface charges and parallel polarization orientation of the ZnO layers causing asymmetric space charge region formation under positive and negative bias. The transient current characteristics suggest use of this structure as nonvolatile memory device. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3211914]

Heterostructures composed of perovskite-structure $BaTiO_3$ (BTO) and wurtzite-structure ZnO are interesting because of the anticipated interface charge coupling effects between the electrically switchable[1–5] and the nonswitchable spontaneous polarization[6] of BTO and ZnO, respectively.[7] The nonswitchable spontaneous polarization of ZnO causes a permanent electric field and biases the switching behavior of the ferroelectric polarization charge in the adjacent BTO layer.[8–11] The permanent electric field also influences the space charge region (SCR) toward BTO in *n*-type ZnO.[11] Two polar [0001] ZnO surfaces give rise to two possible spontaneous polarization vector orientations (P_{sz}).[12–15] In triple or multiple layer heterostructures, polarization coupling can occur at multiple interfaces, and will become interdependent.[16–22] The charge distribution at the interfaces will affect the electrical properties of the overall heterostructure. For a triple layer structure, two scenarios can be envisioned, where either the ferroelectric layer is embedded by two piezoelectric layers, or vice versa. In this paper we study a ZnO–$BaTiO_3$–ZnO heterostructure. We observe an asymmetric interface charge distribution, and discuss relevant device applications for such heterostructures.

We reported previously on electrical Sawyer–Tower (ST) polarization measurements on ZnO-BTO double layer structures which exhibited a strong asymmetric and rectifying behavior.[9] ST measurements detect the charging and discharging ability (the history of electric polarization versus applied voltage) of a capacitive sample compared to a standard ideal capacitor. We developed a dielectric continuum model that described the asymmetric polarization hysteresis behavior and thereby identified that both, the SCR and the spontaneous polarization in ZnO influence the ferroelectric properties of the BTO layer.[10] We also pointed out that the ferroelectric response of the double layer structure is different for positive and negative orientations of P_{sz}. Here we report on capacitance-voltage (*C-V*), current-voltage (*I-V*), ST, and transient current switching (*I-t*) measurements of a ZnO-BTO-ZnO heterostructure. The observed characteristics are explained by the spontaneous polarization orientation of the ZnO at the top and bottom ZnO-BTO interfaces.

Figure 1(a) depicts a model calculated *C-V* hysteresis curve for a semiconductor-insulator-semiconductor (SIS) heterostructure without interface charge coupling and without hysteresis (ferroelectric) properties. For semiconductor layers with equal donor concentrations and interface properties, the *C-V* curve is symmetric with respect to zero volt [Fig. 1(a)], and decreases monotonically for increasing voltages due to formation of identical SCRs in either of the semiconductor layers depending on the sign of the applied voltage. The SCR infers a series capacitance which decreases with increasing voltage, leading to an overall reduction of the total capacitance. For semiconductor layers with equal donor concentrations and ideal interface properties, the *C-V* curve is symmetric with respect to zero volt. Figure 1(b) shows the *C-V* response if the insulator between the two semiconductor layers is ferroelectric. In that case the *C-V* response is shifted along the voltage axis, depending on the

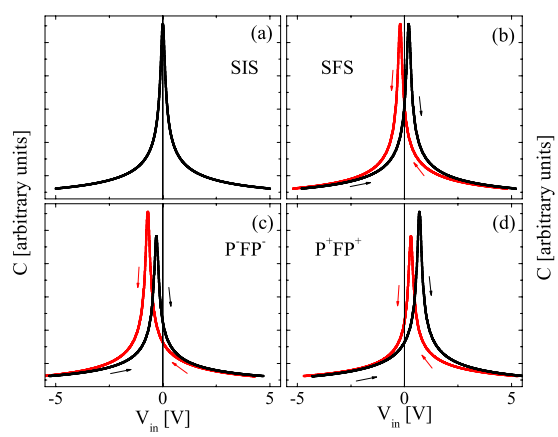

FIG. 1. (Color online) *C-V* characteristic for a SIS (a), semiconductor-ferroelectric insulator-semiconductor (SFS) (b), and piezoelectric semiconductor-ferroelectric insulator-piezoelectric semiconductor layer structure with both piezoelectric spontaneous polarization vectors oriented downward (P^-FP^-) (c) or upward (P^+FP^+) (d) when the bottom layer is grounded.

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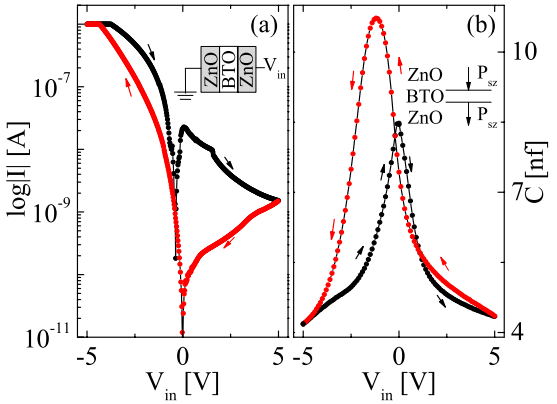

FIG. 2. (Color online) Experimental current-voltage response (a) and capacitance-voltage response (b) of the ZnO-BTO-ZnO heterostructure.

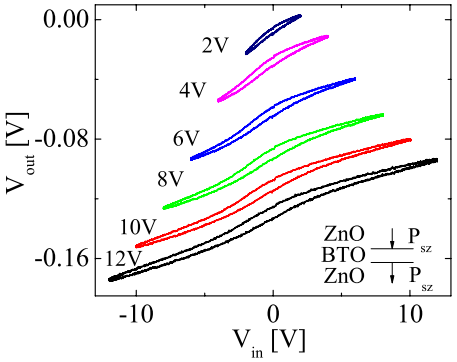

FIG. 3. (Color online) Experimental ST response of the ZnO-BTO-ZnO heterostructure as a function of input voltage amplitudes.

actual polarization in the ferroelectric constituent. The ferroelectric polarization produces additional interface charge, which offsets the SCR formation depending on the sign of the charge. At certain external voltages, the electric field within the ferroelectric layer is sufficient to switch the polarization charge, identified by the maxima in the *C-V* response. A typical symmetric butterfly-type hysteresis is observed centered at zero voltage. Figures 1(c) and 1(d) depict scenarios when the two semiconductor layers carry spontaneous polarizations with their associated polarization vectors parallel to each other (perpendicular to interfaces) oriented downward and upward to the grounded bottom layer, respectively. The associated interface charges affect the SCR formation within the piezoelectric semiconductor layers, and shift (bias) the ferroelectric hysteresis. For both parallel orientations of the spontaneous piezoelectric polarizations, denoted here P^{++} and P^{--}, opposite space-fixed charges are located at the top and bottom semiconductor-ferroelectric interfaces, causing asymmetric SCR formation with asymmetric series capacitance within the semiconductor layers. This asymmetry is rendered by an asymmetric *C-V* response, as shown in Fig. 1(c) and 1(d), respectively. For antiparallel orientations, P^{+-} and P^{-+}, identical charges are located at the top and bottom semiconductor-ferroelectric interfaces. While the piezoelectric interface charges still affect the SCR formation at both interfaces, the changes are symmetric with respect to the applied external voltage, and the *C-V* response is qualitatively equivalent to the case depicted in Fig. 1(b).

The ZnO-BTO-ZnO heterostructure investigated here, was deposited by pulsed laser deposition as reported previously.[10,11] The thickness of the preferential (111) oriented BTO and (0001) oriented (*c*-plane) ZnO layers are 1 and 0.5 μm, respectively. Top and bottom Ohmic Pt contacts were deposited by Magnetron sputtering. The BTO layer was confirmed with ferroelectric perovskite structure at room temperature by x-ray diffraction and temperature-dependent Raman measurements.[7,8,11] *C-V*, *I-V*, and ST investigations on the ZnO-BTO-ZnO heterostructures were performed. The *C-V* characteristics were measured by using an model 4192A LF impedance analyzer (HP Co., Inc.) applying a small AC signal of 10 mV amplitude at 1 kHz while the DC electric voltage was cycled from negative to positive and back to negative bias. ST and *I-V* measurement conditions were performed as reported previously.[10,11]

Figures 2(a) and 2(b) present the results of the *I-V* (log|*I*|-*V*) and *C-V* investigations of our ZnO-BTO-ZnO heterostructure. The *I-V* response reveals strong nonlinear and asymmetric behavior. At negative bias the current reaches two orders of magnitude larger value at equal positive and negative bias voltage, where the current compliance limit was set to 1 μA. The hysteresis renders the structure with lower resistance for negative and with higher resistance for positive external voltage swings. The voltage-asymmetric resistance can be understood by the asymmetric SCR formation, which present series resistances within the heterostructure. For positive voltages, the overall resistance is larger, indicative for the situation P^{--} discussed above. For positive bias voltage, the SCR forming within the top ZnO layer increases due to the positive interface charge provided by the ZnO spontaneous polarization, whereas the SCR forming within the bottom ZnO layer at negative voltage decreases by the same polarization charge. The asymmetry observed in the *C-V* response [Fig. 2(b)] can be understood by the same asymmetric SCR formation mechanism. The capacitance maximum is reduced in the positive voltage region in comparison with the maximum in the negative voltage region and both maxima are shifted toward negative voltages. The reduction of the capacitance maximum at positive voltages is due to the larger SCR formation. The shift is produced by the ZnO interface charges, and both observations corroborate the above suggested P^{--} situation.

Figure 3 depicts ST data from our ZnO-BTO-ZnO heterostructure for various maximum cycling voltages from 2 to 12 V. The response reveals subtle asymmetric properties with respect to zero volt. In addition, a negative drift occurs for increasing cycling voltages. The differential increase of the ST response at a given voltage is proportional to the heterostructure capacitance. The difference in capacitance for positive and negative sweeping directions causes the slightly asymmetric ST loop. A similar observation was made in our previous model calculations for a ZnO-BTO-ZnO heterostructure for P^{--} and P^{++} situations, which reflect the same asymmetry, but different drift with increasing cycling voltage.[23] Because the series resistance of the heterostructure investigated here is smaller at negative bias voltages, the heterostructure continues to charge negatively with increasing cycling voltage thus reflecting the drift of the ST hysteresis loops. A similar behavior was observed previously in ferroelectric samples.[24–26] Bouregba *et al.*[26] recently suggested asymmetric resistance changes as the cause of hysteresis offsets. The authors used a single-layer dielectric continuum model for calculation of the ferroelectric response and augmented parallel circuit models including diode-

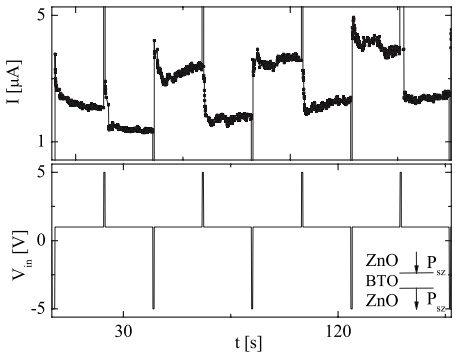

FIG. 4. *I-t* measurements at 1 V (reading) bias and short 5 and −5 V (set bias) pulses.

resistance pairs with different resistance values. The two pairs of antiparallel oriented diodes mimicked the effect of different leakage currents within the ferroelectric layer over interface barriers into the metal contacts.[26] The situation studied here is different in that opposite ZnO-BTO interfaces form two asymmetric diodes with voltage asymmetric series capacitance and resistance properties. Quantitative analysis of our *C-V*, ST, and *I-V* data allows for determination of the spontaneous polarizations parameters. We previously developed a model approach for calculation of the electrical properties of ZnO-BTO-ZnO heterostructures.[10] Details of the present model analysis will be discussed elsewhere. We obtain here that the spontaneous polarization parameter of both ZnO layers amounts to 0.1 μC cm^{-2}, and which is smaller by one order of magnitude than in a previously studied ZnO-BTO heterostructure.[11] We suspect microscopic domain formation with alternating surface orientations within the ZnO layers compensate partially their spontaneous polarizations, and which requires further investigations.

Figure 4 presents pulsed-mode *I-t* measurements at steady reading voltage. The bottom panel depicts the applied bias voltage, which was held constant at 1 V (reading bias), and ramped every 20 s to +5 and −5 V (set bias) for short periods of time (0.5 s). Positive (negative) set bias pulses switch the structure into its high (low) resistance state, in accordance with Fig. 4(a). Note that a different contact pad was used for this measurement, which provided an overall slightly larger current. The measurements reveal fast switching between the different hysteresis states, with good time stability. A background drift requires further investigations, and might be caused by imperfect setup conditions. The *I-t* measurements suggest ZnO-BTO-ZnO heterostructures as candidate for stable, low-power consumptive, nonvolatile memory devices.

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