October 2005

Roadmap for High Efficiency Solid-State Neutron Detectors

R. J. Nikolic
Center for Micro and Nano Technology, Lawrence Livermore National Lab

Chin Li Cheung
University of Nebraska at Lincoln, ccheung2@unl.edu

C. E. Reinhardt
Center for Micro and Nano Technology, Lawrence Livermore National Lab

T. F. Wang
Chemistry and Material Science Directorate, Lawrence Livermore National Lab

Abstract

Proceedings of SPIE -- Volume 6013
Optoelectronic Devices: Physics, Fabrication, and Application II,
Joachim Piprek, Editor, 601305 (Oct. 25, 2005)

(published online Oct. 25, 2005)

http://spiedl.aip.org/dbt/dbt.jsp?KEY=PSISDG&Volume=6013&Issue=1#P601305000001

---

doi:10.1117/12.633256

Roadmap for High Efficiency Solid-State Neutron Detectors

R.J. Nikolić[a*], C.L. Cheung[b], C.E. Reinhardt[a], T.F. Wang[c]
[a]Center for Micro and Nano Technology, Lawrence Livermore National Lab
[b]Department of Chemistry and Center for Materials Research Analysis, University of Nebraska
[c]Chemistry and Material Science Directorate, Lawrence Livermore National Lab

ABSTRACT

Solid-state thermal neutron detectors are generally fabricated in a planar configuration by coating a layer of neutron-to-alpha converter material onto a semiconductor. The as-created alpha particles in the material are expected to impinge the semiconductor and create electron-hole pairs which provide the electrical signal. These devices are limited in efficiency to a range near (2-5%)/cm^2 due to the conflicting thickness requirements of the converter layer. In this case, the layer is required to be thick enough to capture the incoming neutron flux while at the same time adequately thin to allow the alpha particles to reach the semiconductor. A three dimensional matrix structure has great potential to satisfy these two requirements in one device. Such structures can be realized by using PIN diode pillar elements to extend in the third dimension with the converter material filling the rest of the matrix. Our strategy to fabricate this structure is based on both "top-down" and "bottom-up" approaches. The "top down" approach employs high-density plasma etching techniques, while the "bottom up" approach draws on the growth of nanowires by chemical vapor deposition. From our simulations for structures with pillar diameters from 2 μm down to 100 nm, the detector efficiency is expected to increase with a decrease in pillar size. Moreover, in the optimized configuration, the detector efficiency could be higher than 75%/cm^2. Finally, the road map for the relationship between detector diameter and efficiency will be outlined.

Keywords: neutron detection, pillars, pixel array, nanowires, high density plasma etching, boron, alpha.

1. INTRODUCTION

Neutron detectors fall into two categories: those suitable for detecting thermal (low-energy) neutrons, and those that directly detect and measure the energy of fast (high energy) neutrons. The Helium-3 tube based system has long been used for thermal neutron detection and the efficiency (depending on size) can be high and with recent advances can be 70 % [1]. There are several significant drawbacks to many Helium-3 tube configurations in terms of portability as well as field deployment. For example, the high pressure gas in the tubes makes transport via air shipment difficult; the high-bias voltage required can be a hazard if underwater; the stability of the system is in general poor; and the system is sensitive to microphonics. They are also normally bulky and difficult to configure. Current solid-state detectors suffer from poor resolution, moderate to poor fieldability, inconvenient geometries, low absolute efficiency, and a lack of directional information. The need for improved neutron detection is evident since neutrons are a highly specific indicator of fissile material. Recognizing this need, we propose to exploit recent advances in micro and nanofabrication and advanced materials, to build the next generation of neutron detectors for national security requirements. Room temperature high resolution, high efficiency and scalable radiation detection can be realized by manipulating materials at the nano and microscale. Using recoil charged particle tracking, the direction and the energy of the incident neutron can be reconstructed.

This paper is organized as follows. Section 2 outlines the roadmap for high efficiency thermal neutron detectors. The detector device physics and use of converter materials are explained. Also, the device geometric impacts are shown to directly affect the detector efficiency with the possibility to reach over 75%/cm^2. Section 3 shows the mapping of the device geometry to techniques for producing such devices from sub 100 nm to micron dimensioned features. Section 4 discusses two technology hurdles that must be overcome in order to fabricate devices with geometries that will be able to reach over 75%/cm^2 efficiency. These include the ability to etch high aspect ratio features with diameter of 2 μm and aspect ratio of 25 and boron deposition or growth with a high fill factor to fill the etched region. Section 5 covers the device currently being fabricated as our proof-of-principle device. Section 6 is the conclusion.

2. SOLID STATE PILLAR NEUTRON DETECTOR ROADMAP

Our proposed pillar semiconductor neutron detector is designed for detecting neutrons with a revolutionary improvement in efficiency. The pillar semiconductor platform is designed to eliminate the geometrical constraints that limit the amount of active neutron converter material in planar semiconductor neutron detectors. For planar semiconductor detectors, usually a layer of neutron converter material is coated on the device surface (Figure 1a). As an example, boron 10 is frequently used as a thermal neutron converter material. The thermal neutron ^{10}B reaction produces charged particles: alpha particles (1.47 MeV) and ^{7}Li (0.84 MeV) [2]. These charged particles subsequently enter the semiconductor detector material to create electrons and holes for generation of electrical signals. However, these charged particles can travel inside the converter materials only for a short distance. The alpha particle travel distances in different materials are calculated by finding the mean range of travel distance in which the intensity of alpha particles drops by a half. The range of (1.47 Mev) α in boron 10 is ~ 3.3 μm, as shown in Figure 2 [3]. Thus, if the boron layer is too thick, the charged particles will be absorbed before they reach the semiconductor material. This is a design conundrum because the converter material needs to be sufficiently thick to capture most of the incoming thermal neutrons. Furthermore, the as-generated charged particles that travel away from or even parallel to the planar semiconductor surface may not be detected.

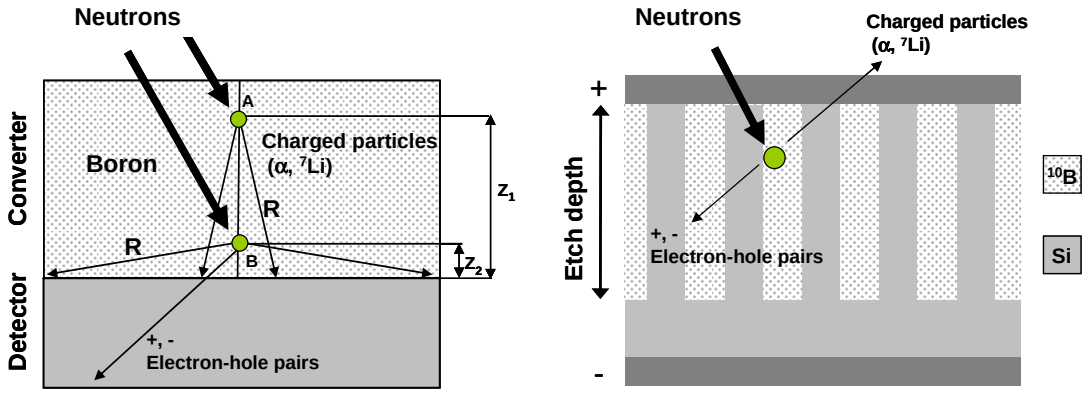

Figure 1 (a) Schematic of planar solid state neutron detector [4] (b) proposed pillar semiconductor platform with ^{10}B in a semiconductor detector matrix.

A schematic of the planar detector is shown in Figure 1a to explain the limitation of active converter material thickness. The charged particles from the thermal neutron ^{10}B reaction emitted from point **A** at distance $\mathbf{Z_1}$ from the detector have a low probability to reach the semiconductor detector. Only forward directed particles emitted can reach the detector and produce signals. The rest of the particles are stopped in the converter. Clearly, the probability of signal generation for particles emitted from point **B**, at $\mathbf{Z_2 < Z_1 < R}$, is much higher than for the ones from point **A**. Thus, only a limited converter thickness is effective for the detection.

The above discussion explains the reasoning for having the boron layer thick enough to capture the neutron flux but at the same time thin enough to allow the alpha particle to travel through the boron layer and reach the detector. The upper limit of the detector thickness can also be evaluated by the mean travel range of alpha particles for different materials (Figure 2). For α (1.47 Mev) in silicon, the range is ~ 5.3 μm. For a denser material like GaAs, the range will be reduced (Figure 2).

Our proposed design is a dramatic technology advance that can increase the neutron detection efficiency from the current 2-5%/cm^2 [5], towards greater than 75%/cm^2. The platform consists of pillars of PIN diodes grown on planar semiconductor substrates (Figure 1b). The converter material (boron) and the detector material are inter-digitated such that charged particles from the thermal neutron ^{10}B reaction have a significantly higher probability of impinging the detector material due to the close proximity. Moreover, the thickness of active converter materials is not limited, because most charged particles generated at different depths of the converter materials can be detected by the adjacent detector pillar.

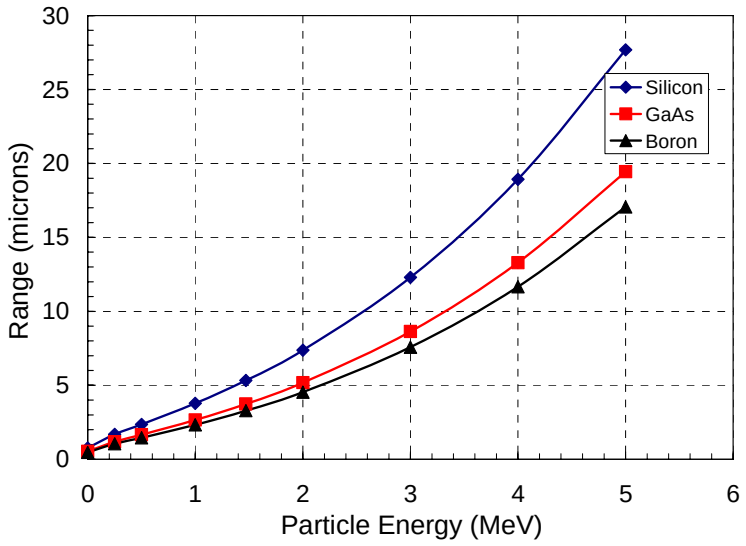

Figure 2 Range of alpha particles in Boron, Silicon and GaAs.

The device geometry for our experiments is evaluated by simulating the efficiency based on a combination of Monte Carlo and TRIM codes for statistically determination of the effective neutron cross section and the travel range of the charged particles, respectively. The etch depth, pillar width and converter material and ratio with respect to the pillar width, are modeled with these codes. Preliminary data from the simulation, shown in Figure 2**,** indicate that the detector efficiency could reach 65%/cm^2 for a pillar width (and converter width) of 2µm with an etch depth of 50µm. This is over a 10 fold increase over the current state-of-the-art planar structure. There is an additional increase of 31% by shrinking the device diameter from 2µm down to 100nm, for an equivalent etch depth of 50µm. The relatively large etch depth of 50 µm is needed to capture the full thermal neutron flux, while the small device pitch is required to insure the alpha particles to strike the detector instead of being absorbed in the boron region.

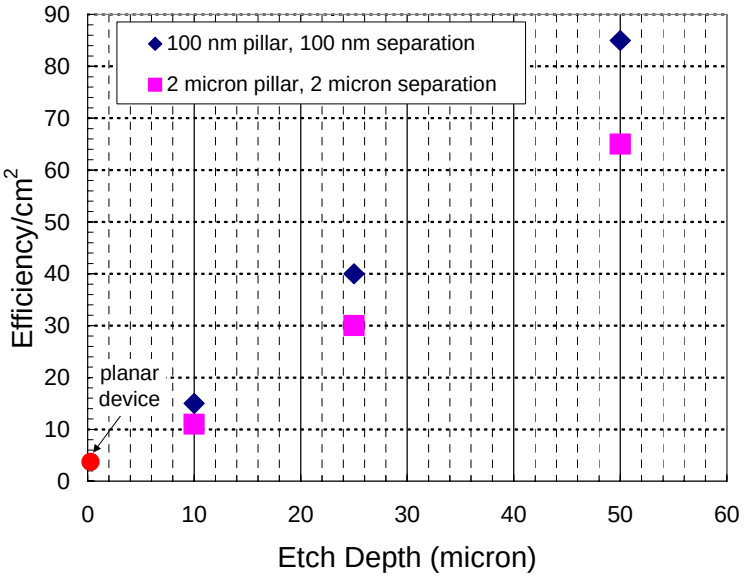

Figure 3 Neutron detection efficiency versus etch depth of pillar structures for various silicon detector pillars of micron and sub-micron sized diameters and gaps filled with ^{10}B.

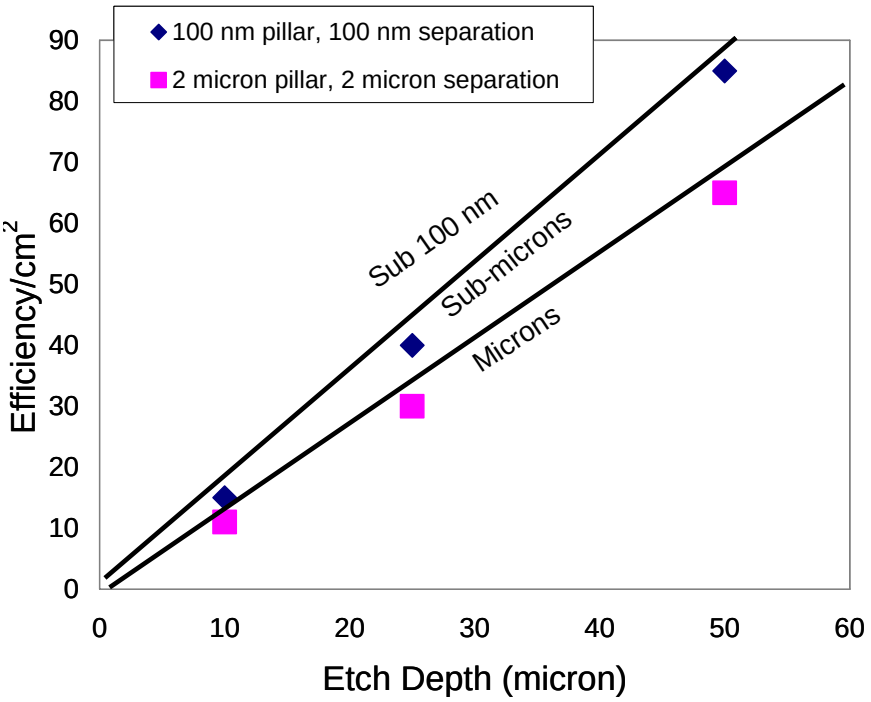

Figure 4 Efficiency versus etch depth for technology size ranges.

3. TECHNOLOGY MAPPING FOR DEVICE FEATURE SIZE

The efficiency of the detector scales with the pillar size, where a smaller pillar diameter with a closer spacing give rise to a higher efficiency, as discussed in Section 2 and shown graphically in Figure 3. Figure 4 shows the pillar diameter ranges to realize these devices: micron, sub-micron and sub 100 nm. There are many technologies that can be applied to realize devices with these dimensions. In this section, we highlight the methods we are using to fabricate devices which cover the entire spectrum in question from micron to sub 100 nm devices. In order to cover this range, we use both a "bottom-up" and "top-down" approaches which are discussed below.

3.1 Bottom-up approach

The bottom-up detector fabrication scheme is used to grow nanowires with sub 100nm diameter. The detector fabrication scheme is shown in Figure 5. First, metal catalyst particles, such as gold and copper are patterned on the top of a semiconductor such as silicon by evaporation of metals or deposition of metal colloids of well-defined size. The substrate is then put in a chemical vapor deposition chamber in which appropriate pre-cursors of semiconductor gases are supplied to the catalyst to synthesize semiconductor nanowires by the vapor-liquid-solid mechanism [6]. The space between the nanopillar structures are then filled with neutron converter material. Lastly, the contact metals and electrodes are deposited on the top and bottom sides of the substrates for electrical connection to the detection electronics.

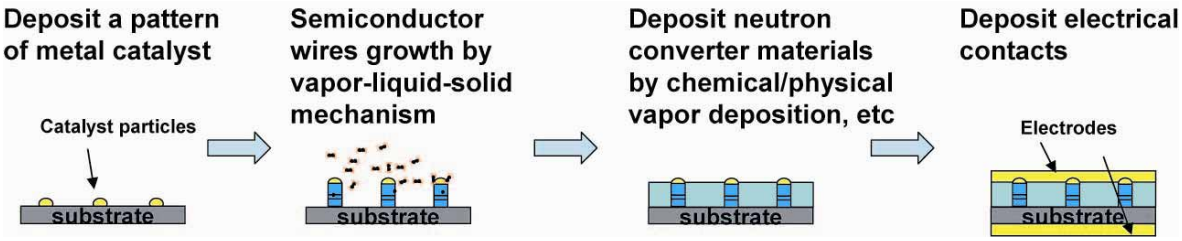

Figure 5 Bottom-up approach for the fabrication of proposed neutron semiconductor detector.

3.2 Top-down approach

The "top-down" approach uses wafer scale patterning to define the pillars and subsequent plasma etching to etch the feature. For the micron sized pillars we are using standard contact lithography. In order to reach sub-micron geometries we have developed a process which uses polystyrene beads which are spin coated to define the pillars. The technique can be used to define geometries from 500 nm to 100 nm. This can be done by O_2 plasma processing to tailor the geometry of the beads. This is shown in Figure 6 and discussed in more detail in [7].

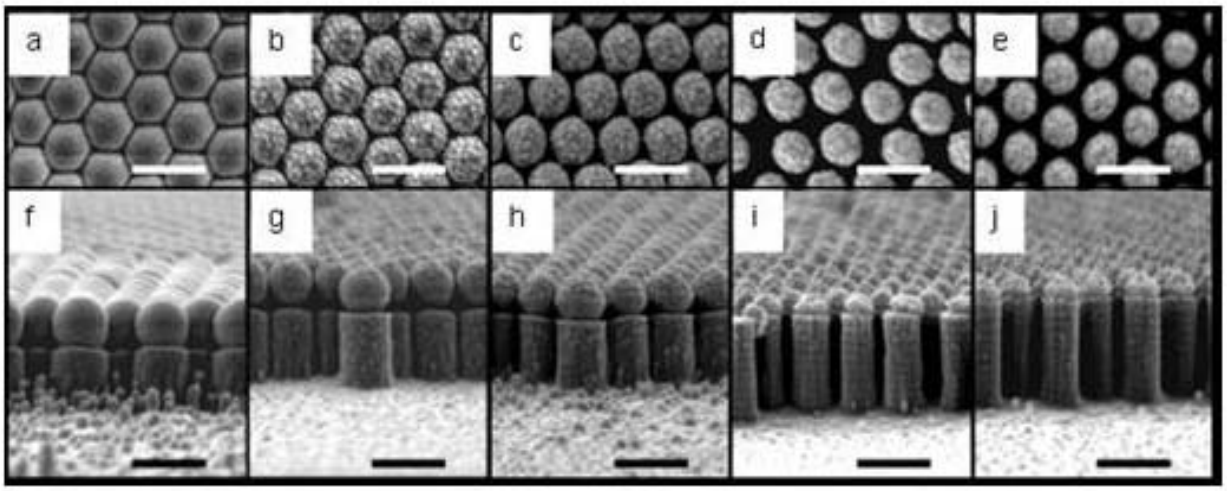

Figure 6 Top row shows top-view of polystryrene masked etched pillars, where the diameter of the bead is tailored by RIE etching in O_2. The bottom row shows the cross section view after STS plasma processing (see Table 2) to etch the silicon pillars. The scale bar is 750 nm.

4. TECHNOLOGY REQUIREMENTS

The advanced solid-state neutron detector requires state-of-the plasma etching and boron processing. The plasma processing is required for the top-down methodology, which is our first device.

Plasma processing

Plasma processing continues to be one of bottle necks for semiconductor device processing. Devices requiring high-aspect ratio etching include photonic crystals [8] and MEMS gyroscopes [9], among others. Our requirements for plasma etching are based on the relationship between detection efficiency and etch depth, as shown in Figure 2. With the increased etch depth and backfill with boron, a near complete thermal neutron capture is theoretically possible. This requires anisotropic features with an etch depth of 50 μm with an aspect ratio of 1:25 for the 2 μm diameter pillar detector geometry. Adequate masking materials and vertical etched features with smooth sidewalls are also required. These requirements can be met with high density plasma systems which employ high density plasma to provide a large ion flux with small ion energy that yields low-damage etching. For instance, electron cyclotron resonance system (ECR) and inductively coupled plasma (ICP) systems fall into this category. Unlike reactive ion etching (RIE) systems which

have the ion density coupled to the bias voltage, high density plasma etchers have these two parameters uncoupled to enable highly anisotropic etching with smooth features.

Our initial devices employ a silicon based detector with etching by a deep RIE system [10] with an ICP plasma source and the time-multiplexed "Bosch Process", which uses SF_6 to etch silicon and C_4F_8 for the passivation step. The time-multiplexed process is carried out by etching with SF_6 for 12 seconds and then a 9 second passivation step with C_4F_8. The etch rate is determined by the full cycle: etch and passivation. The plasma processing recipe is summarized in Table 1.

Table 1 Silicon plasma processing recipe for pillar fabrication.

Deposition gas, C_4F_8	85 sccm, 11 mTorr
Etch gas, SF_6	15 sccm, 5.5 mTorr
RF	600 W
Platen power	14 W
Silicon etch rate	~ 0.4 μm/min

The deep RIE process is applied to samples with mask features with both micron and submicron diameter devices. This is done to study the effect of radiation and charged carrier transport for various device sizes. This will be used to experimentally validate our simulations shown in Figure 3. Figure 7a shows SEM images of the 2 micron diameter pillar with a separation of 4 μm and an etch depth of 3.9 μm. Figure 7b shows the silicon nano-pillars of ~ 200 nm (with near equivalent separation) and an etch depth of 2.3 μm. For these relatively shallow etching (compared with our long term goal of 50 μm), the etch selectivity of the photoresist mask (S < 10) is not an issue. However, thicker and more robust mask layers such as thermal oxide or metals will be needed to achieve our long term goal for the high aspect ratio pillars with an etch depth of 50 μm.

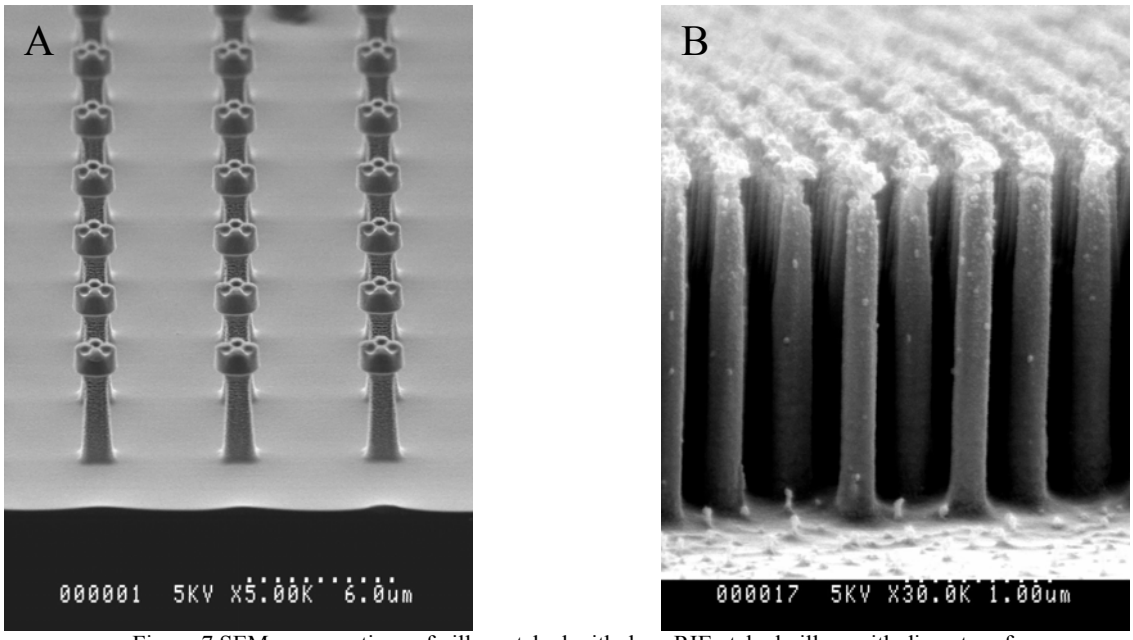

Figure 7 SEM cross sections of pillars etched with deep RIE etched pillars with diameter of (A) micron and (B) submicron.

4.2 Boron deposition

The ability to deposit conformal and uniform coating of boron 10 is one of the key steps to the success of the proposed neutron semiconductor detector. Since alpha particles are generated in the ^{10}B (n, α) reaction, any air gap between the semiconductor and the boron layer will decrease the detector sensitivity. Our proposed semiconductor pillar platform requires completely filling of the high-aspect-ratio space between the pillars with boron. The common methods for boron deposition are electron beam (e-beam) evaporation, sputtering, and chemical vapor deposition:

E-beam evaporation

E-beam evaporation of boron is the most common method to deposit boron because of its simplicity in the requirement of the boron source. Extensive investigations were performed to optimize the evaporation of boron [11]. Since boron has a high melting point (2076ºC) and sublimation point (2550ºC), electron beam, rather than resistive heating, is required to supply enough energy for vaporization. Boron source targets with low purity (90% or less) or uneven heating of the boron target will cause non-uniform evaporation rates and "spiting" of materials from the evaporation target.

Presently, we are investigating parameters to optimize conformal coverage of boron between our micron-sized pillar structures by e-beam evaporation. As the e-beam evaporation is a line-of-sight method of deposition, the photoresist pattern can easily create shadowing effects and therefore create small gaps between the vertical walls of pillars and the as-deposited boron layer.

Sputtering

Sputtering is another method to deposit boron onto high-aspect-ratio structures. Since the sputtering action of the boron targets would generate boron clusters in randomized directions, the as-deposited boron layer is expected to be more conformal to the geometry of the substrates. However, as boron is a poor conductor charging of the target during sputtering will occur. Therefore, a pure boron sputtering target will usually yield low deposition rates unless the boron is coated as a thin layer on a conductor [11]. Thus, semi-conducting boron carbide (B_4C) or doped boron is often used as the sputtering target to deposit materials with boron 10 isotopes.

Chemical vapor deposition

Chemical vapor deposition (CVD) is a well-known technique to produce conformal coverage of materials on high-aspect-ratio structures. Two of the common precursors for CVD of boron are diborane (B_2H_6) and decaborane ($B_{10}H_{14}$). Diborane exists as a gas at room temperature. Thermal CVD with diborane has been successfully applied to grow boron films at 600-1000ºC [12]. Though the gaseous form of this chemical allows the ease of transport to the reactor, its high toxicity often imposes expensive safety precautions, such as the installation of gas cabinets and relatively expensive production of boron 10 isotopes of this chemical.

Decaborane has become one of the preferred precursors for boron deposition due to its advantageous physical properties. First, high purity decaborane can be easily obtained with sublimation purification processes (Sublimation temperature ~ 70ºC). Second, even though decaborane is toxic, since the decaborane is in solid form at room temperature, the materials can be easily contained and handled. Furthermore, decaborane has a lower thermal decomposition temperature (~ 200-400ºC) for thin film deposition [13]. Since decaborane is in solid form at room temperature, it needs to be sublimed at 70+ºC into its gas form for delivery to the reactor. Similar to other non-gaseous precursors, precise control of non-gaseous form materials would require special heated mass flow controllers and manometer set up to control the dynamics of materials deposition. Based on the as-discussed consideration, we are currently developing CVD boron deposition using decaborane.

5. FIRST PROOF-OF-PRINCIPLE DEVICE

Our first proof-of-principle device is illustrated in Figure 8b, a planar device is being processed at the same time for efficiency comparison (Figure 8a). The epitaxial layer structure is shown in Table 2. Here we are using a silicon based structure where the epitaxial growth is done by CVD. Various semiconductors materials can be used with the approach we have outlined; tradeoff's among semiconductors is discussed in [14]. The top layer is doped p+ to form an ohmic contact, while an n+ wafer is used to form the backside ohmic contact. The backside contact is TiPtAu while the top

planar contact is Al. The contacts used do not require annealing. The pillars are etched by the "top-down" approach using a 2 µm dual layer of PECVD SiO_2 and photoresist. The etch recipe is shown in Table 1. For the planar device the thickness of boron 10 t_C = 3 µm, for the pillar device the etch depth d_e will define the thickness of the boron 10, for this structure we will step the thickness d_e=3,4,5,6 µm. This will clearly show the increased efficiency of the pillar structure when d_e > 3 µm. The planar structure is limited to the boron 10 thickness of 3 µm as discussed in Section 2. Our next wafer design has an i-region of 25 µm, which will show a more dramatic efficiency increase.

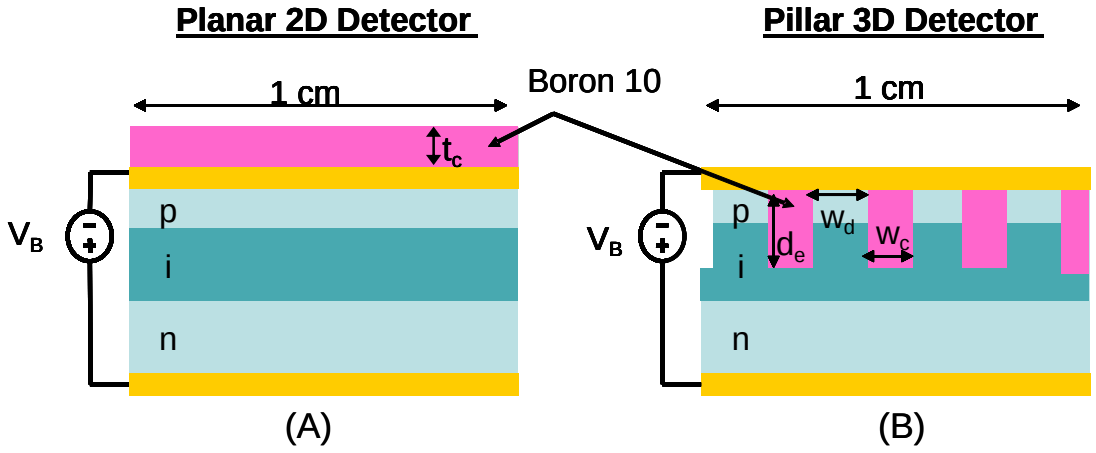

Figure 8 (A) Schematic of planar and (B) pillar detector.

Table 2 Epitaxial layer structure of silicon PIN detector.

P+	2200 Å	$1.3x10^{18}$ cm^{-3}	Boron
i (n)	5.33 µm	$N \leq 3x10^{13}$ cm^{-3}	Arsenic
N+	Si substrate	$1x10^{18}$ cm^{-3}	Arsenic

6. CONCLUSION

We have outlined a new approach to the detection of thermal neutrons by moving from a planar device structure to a 3-dimentional matrix of PIN detector pillars, with converter material filling this matrix. With this structure we have shown *via* simulations that the detector efficiency can have a revolutionary increase from roughly 2-5%/cm^2 towards over 75%/cm^2. This efficiency can be realized by micron sized features, however further improvements can be achieved by shrinking the device geometry to the nanoscale. Furthermore, by covering a wide range of device sizes, the transport of both radiation and charged carriers can be exploited. This will make possible important advances in neutron detection as well as nanoscale device technology which has a multitude of applications as well as scientific discovery.

REFERENCES

1. J.F.C.A. Veloso, F. Amaro, J.M.F. dos Santos, J.A. Mir, G.E. Derbyshire, R. Stephenson, N.J. Rhodes and E.M. Schooneveld, "Application of the microhole and strip plate detector for neutron detection," *IEEE Transactions on Nuclear Science*, **51**, pp. 2104-2109, 2004.
2. G.F. Knoll, *Radiation detection and measurement*, p. 507, John Wiley & Sons, Hoboken, 2000.
3. N. Tsoulfanidis, *Measurement and detection of radiation*, pp. 131-137, Taylor & Francis, Washington, 1995.
4. M. Wielunski, R. Schütz, E. Fantuzzi, A. Pagnamenta, W. Wahl, J. Palfálvi, P. Zombori, A. Andrasi, H. Stadtmann and Ch. Schmitzer, "Study of the sensitivity of neutron sensors consisting of a converter plus Si charged-particle detector," *Nuclear Instruments and Methods in Physics Research A*, **517**, pp. 240-253, 2004.
5. H. K. Gersch, D.S. McGregor, and P.A. Simpson, "The effect of incremental gamma-ray doses and incremental neutron fluences upon the performance of self-biased 10B-coated high-purity epitaxial GaAs thermal neutron detectors," *Nuclear Instruments and Methods in Physics Research A*, **489**, pp. 85-98, 2002.
6. R. A. Wagner, and W.C. Ellis, "Vapor-Liquid-Solid Mechanism of Single Crystal Growth," *Appl. Phys. Lett.* **4**, pp. 89-90, 1964.
7. C.L. Cheung, R.J. Nikolić, C.E. Reinhardt, and T.F. Wang, "Fabrication of nanopillars by nanosphere lithography," in preparation.
8. S. Anand, M. Qiu, M. Mulot, M. Swillo, B. Jaskorzynska, and A**.** Karlsson, "High-aspect-ratio etching and characterization of 2D photonic crystals in InP/InGaAsP/InP heterostructures," SPIE-Int. Soc. Opt. Eng. Proceedings of Spie - the International Society for Optical Engineering, **5277**, no.1, pp.78-89, 2004.
9. F. Ayazi and K. Najafi, "High aspect-ratio polysilicon micromachining technology," *Sensors and Actuators A*, **87**, pp. 46-51, 2000.
10. Rangelow, I.W., Critical tasks in high aspect ratio silicon dry etching for microelectromechanical systems, *Journal of Vacuum Science Technology A*, **21**, 1550-1562, 2003.
11. G.E. Thomas, "New technique for producing thin boron films," *Nuclear Inst. Methods in Physics Research A*, **282**, pp. 124-127, 1989.
12. Y. Kumashiro, K. Sata, S. Chiba, D. Yamada, K. Tanaka, T. Huodo, K. Yokoyama, and K. Hirata, "Preparation of boron and boron phosphide films by photo- and thermal chemical vapor deposition process," *J. Solid State Chem.*, **154**, pp. 39-44, 2000.
13. Y. Kumashiro, K. Nakamura, Y. Doi, K. Hirata, T. Yokoyama, and K. Sato, "The preparation of B-Sb thin films by molecular flow region PVD process," *J. Crystal Growth*, **237-239**, pp. 1531-1535, 2002.
14. G. Lutz, *Semiconductor radiation detectors*, pp. 80-81, Springer-Verlag, Berlin, 1999.

* Email address of corresponding author, Rebecca Nikolić, nikolic1@llnl.gov.

This work was performed under the auspices of the U.S. Department of Energy by University of California, Lawrence Livermore National Laboratory under Contract W-7405-Eng-48, UCRL-PROC-213583.