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Abstract—**A technique is described for evaluating the effectiveness of production tests for large scale integrated (LSI) circuit chips. It is based on a model for the distribution of faults on a chip. The model requires two parameters, the average number (n_0) of faults on a faulty chip and the yield (y) of good chips. It is assumed that the yield either is known or can be calculated from the available formulas. The other parameter, n_0, is determined from an experimental procedure. Once the model is fully characterized, it allows calculation of the field reject rate as a function of the fault coverage. The technique implicitly takes into account such variables as fault simulator characteristics, the feature size, and the manufacturing environment. An actual LSI circuit is used as an example.**

I. Introduction

THE reasons for the practical impossibility of obtaining a complete functional test for a large scale integrated (LSI) circuit may be found among the following attributes: 1) imperfect fault modeling: an actual fault may not correspond to a modeled fault or vice versa [1]; 2) data dependency of faults: it may not be enough to exercise all the functions on a chip since execution of certain functions may be sensitive to data or, worse, to data sequences [2, p. 46]; 3) testability limitations: some LSI circuits may be harder to test because of the pin limitation resulting in the lack of direct access to subcircuits. Thus, if the circuit passes the test, one still cannot guarantee that it is free from faults.

Test designers consider *fault coverage* as a measure of a test's capability to isolate a faulty circuit. Most present-day simulators that are used to determine the fault coverage can simulate single logical (line-stuck type) faults but cannot evaluate the coverage of actual physical faults (shorts or breaks in metallization or diffusion runs, shorting of substrate with metallization or diffusion [1], [2]-[4]). Multiple logical faults are also frequent in the production environment, but the exact relationship between single- and multiple-fault coverage is not well understood [5, p. 21]. Also, different simulators may employ different criteria to detect fault-induced races and oscillations.

Detection of some faults may never be possible, or may be quite irrelevant because of redundancies. If a test could be generated for the complete design verification of a circuit, then the faults that are not detected by the test could be ignored as redundant. Even when only single stuck type faults are targeted, the cost of test development and test application increases very rapidly with an increasing fault coverage requirement.

Since stuck type faults represent only a sample of all possible faults, the coverage of such faults can be regarded as a *figure of merit* for a test. In this paper we try to answer the question: how is this figure of merit related to the quality of the tested product? It is assumed that the desired value of the stuck-type fault coverage would depend upon the circuit implementation, technology, manufacturing environment, and, of course, the required quality level of the tested product. The method developed is based upon a model of fault distribution on the chip. The parameters of this distribution are determined experimentally by examining an actual production lot of chips. The analysis then gives the value of fault coverage required for a given quality (field reject rate [6]) of the tested chips. A previous attempt in this direction [6] was based upon a more restrictive model for the distribution of faults. It produced satisfactory results for chips with high yield (typically, SSI and MSI), but predicted too pessimistic fault coverage values for larger chips with lower yield. Our analysis is not restricted to any particular type or size of chips and can be applied to all scales of integration.

II. Definition of Symbols

A	chip area
D_0	defect density
f	fault coverage
m	number of faults covered by tests
n	number of faults present on a chip
n_0	average number of faults on a defective chip
n_{av}	average number of faults on a chip
N	total number of possible faults on a chip
$p(n)$	probability of exactly n faults being present on a chip
$P(f)$	probability of a chip being found faulty when tested to a fault coverage f
$q_k(n)$	probability of detecting exactly k faults when the chip has n faults present
$r(f)$	field reject rate for fault coverage f
y	yield of chips (probability of a manufactured chip being good)
$Y_{bg}(f)$	probability of a faulty chip being tested as good when the fault coverage of tests is f
λ	a parameter depending upon the variance of D_0.

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III. The Model

Assume that an integrated circuit chip has n faults. Although there can be several types of faults on the chip, we assume that the faults on the chip are equivalent to n single stuck type of faults. In other words, the faults present on our chip are such that they can be detected by tests that detect n stuck type of faults. We further assume that the yield of good chips is y and that the number of faults n on a faulty chip has a Poisson distribution [7, p. 156]:

prob {number of faults = n}

$$= p(n) = (1 - y)\frac{(n_0 - 1)^{n-1}}{(n-1)!} e^{-(n_0 - 1)}, \quad n = 1, 2, 3, \cdots$$

$$p(0) = y, \tag{1}$$

where n_0 is the average number [1] of faults on a faulty chip. In the above expression, the Poisson's density function has been shifted to the right by one unit since it is used for the probability of the number of faults on a defective chip, i.e., $n \neq 0$, $n = 1, 2, 3, \cdots$. From (1), the average number of faults is obtained as

$$n_{av} = \sum_{n=0}^{\infty} n\, p(n) = (1 - y)n_0. \tag{2}$$

Indeed, the number of terms in the above summation should be equal to the maximum number of faults N. In practice, however, the value of n_0 is much smaller than the maximum number of faults and the use of the infinite sum, which allows a simple result, is numerically quite accurate. The distribution of faults, as given by (1), is characterized by the two parameters y and n_0.

Furthermore, we assume that the yield y of the chip is known, at least approximately. In fact, the yield of integrated circuits has been widely studied in the past [8]-[14]. The following formula is often used for calculating chip yield [12], [13]:

$$y = (1 + \lambda D_0 A)^{-(1/\lambda)} \tag{3}$$

where [13]

A = chip area

D_0 = average number of defects per unit area

and

$D_0^2\,\lambda$ = variance of D_0.

The parameters D_0 and λ can be determined either experimentally as described in [11] or from the results on previously manufactured chips that came off the same processing system.

The estimation of the remaining parameter n_0 will be discussed later.

[1] Notice that the parameter n_0 is different from the average number of physical defects (D_0A), which is used for calculating the chip yield. In a highly dense circuit, a physical defect can produce several logical faults.

IV. Field Reject Rate

Let us assume that the total number of possible faults on a chip is N, where $N >> n_0$. We test these chips by the tests that detect m faults. The fault coverage is then $f = m/N$. Let $q_k(n)$ be the probability of detecting exactly k faults when a chip has n faults present on it. The, $q_k(n)$ is given by the hypergeometric density function [7, pp. 43-44]

$$q_k(n) = \frac{\binom{n}{k}\binom{N-n}{m-k}}{\binom{N}{m}}. \tag{4}$$

The probability of passing the chip, having n faults, as good is

$$q_0(n) = \frac{\binom{N-n}{m}}{\binom{N}{m}} \simeq (1 - f)^n \tag{5}$$

where $f = m/N$ is the fault coverage of tests. The above approximation is quite accurate for $n << \sqrt{N(1-f)/f}$ and it will be used in the following analysis. For larger values of n, a better closed form expression is derived in [15] where the accuracy of (5) is also discussed.

Now, since the number of faults n on a bad chip is a random number, the probability (or yield) of a bad chip being tested as good is given by

$$Y_{bg}(f) = \sum_{n=1}^{N} q_0(n)\, p(n). \tag{6}$$

On substituting from (1) and (5), and simplifying, we get

$$Y_{bg}(f) \simeq (1 - f)(1 - y)e^{-(n_0 - 1)f}. \tag{7}$$

The field reject rate $r(f)$ is defined as the ratio of the number of bad chips tested as good and the number of all chips that are tested as good [6]. Therefore,

$$r(f) = Y_{bg}(f)/[y + Y_{bg}(f)]$$

and, upon substituting from (7), we obtain

$$r(f) = \frac{(1 - f)(1 - y)e^{-(n_0 - 1)f}}{y + (1 - f)(1 - y)e^{-(n_0 - 1)f}}. \tag{8}$$

Fig. 1 shows a plot of (8) for two different yields, $y = 0.80$ and 0.20. In each case, two curves corresponding to $n_0 = 2$ and 10, respectively, are drawn. This graph illustrates the dependence of test result on the parameter n_0. Consider the yield of 80 percent (say, for an MSI chip). If we wish to test the chip for a field reject rate below 0.5 percent, then the fault coverage should be 95 percent for $n_0 = 2$ or 38 percent for $n_0 = 10$. Similarly, for a yield of 20 percent (which is closer to LSI) one would require a fault coverage of 99 or 63 percent, depending upon whether n_0 is taken as 2 or 10. As pointed out earlier, the parameter n_0 not only depends upon the chip size, but may also be a function of technology, design rules, processing environment, etc. We will, therefore, use an experimental procedure for determining this parameter.

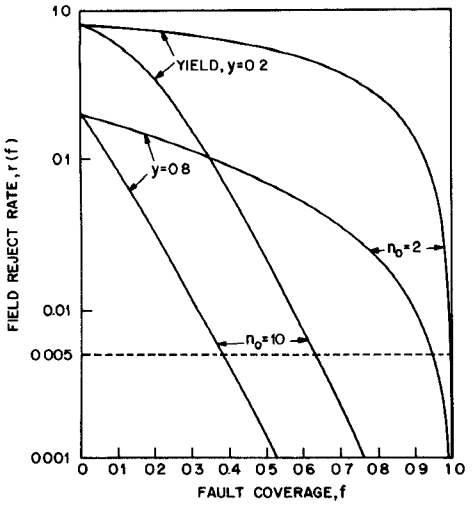

Fig. 1. Field reject rate for two chips with yields of 80 and 20 percent.

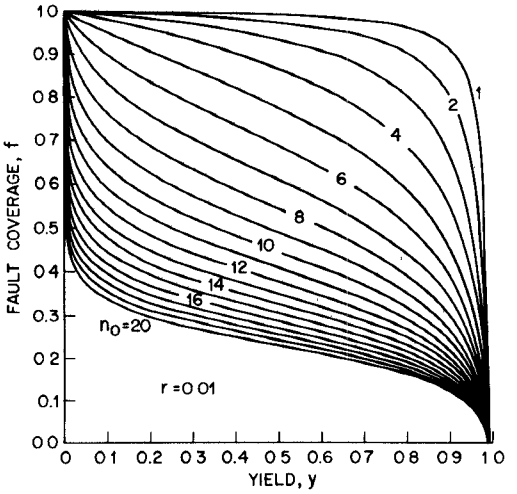

Fig. 2. Fault coverage required for a field reject rate of one in 100.

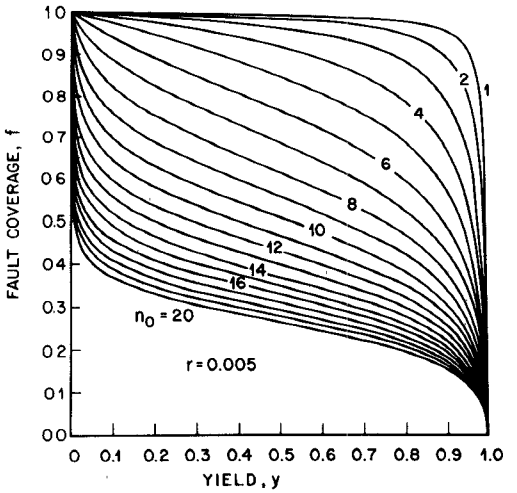

Fig. 3. Fault coverage required for a field reject rate of one in 200.

V. Experimental Characterization of Model

Consider the fraction of chips that have been rejected by tests having a fault coverage f. This fraction is equal to the following probability

$$P(f) = 1 - y - Y_{bg}(f).$$

Upon substitution from (7), we get

$$P(f) = (1 - y)\,[1 - (1 - f)\,e^{-(n_0 - 1)f}]. \tag{9}$$

For a given chip, the yield y can be calculated from (3). In order to determine n_0, we start with a set of test patterns which need not have a high fault coverage. These patterns are evaluated on a fault simulator in the same order as they would be applied to the chip. A cumulative fault coverage as a function of the number of test patterns is thus obtained. Next, the patterns are used for testing the chips that are being produced in the processing line. A chip is rejected at the first pattern that it fails. A sufficiently large number of chips (say 100-200) are tested so that the cumulative fraction of rejected chips can be plotted as a function of the fault coverage. The calculated yield $P(f)$, as computed from (9), is also plotted on the same graph for various values of n_0. The value of n_0 that is closest to the experimental curve is then selected for use in the calculation of the required fault coverage.

Experience has shown that in LSI testing a large proportion of the chips is rejected by the first few test patterns. Thus, the graphs of the fraction of rejected chips and the function $P(f)$ exhibit a steeply rising straight-line behavior near the origin. The experimental value of this slope can also be used for determining n_0 since from (9)

$$P'(f) = \frac{dP(f)}{df} = (1 - y)\,[1 + (1 - f)\,(n_0 - 1)]\,e^{-(n_0 - 1)f}$$

and

$$P'(0) = (1 - y)n_0. \tag{10}$$

Notice that the slope $P'(0)$ is equal to the average number (n_{av}) of faults as given by (2). One can determine an experimental value of $P'(0)$ by applying a relatively small number of test patterns to the chips. Also, when the yield is not known, $n_0 \simeq P'(0)$ can be used as an estimate. Notice that $P'(0)$ will be a close approximation for n_0 for low-yield chips. Since, for a nonzero yield, $P'(0) < n_0$, use of $P'(0)$ in place of n_0 will give a pessimistic (or safe) value of fault coverage; in Fig. 1, a lower value of n_0 means a higher fault coverage for a given field reject rate.

The procedures for determining n_0 as outlined here will be illustrated by an example in a later section.

VI. Fault Coverage Requirement

Once n_0 has been evaluated for a chip, the required fault coverage for any specified field reject rate can be computed from (8). It is, however, not very convenient to solve (8) for f. If the required field reject rate is r, then from (8) we get

$$y = \frac{(1 - r)\,(1 - f)e^{-(n_0 - 1)f}}{r + (1 - r)\,(1 - f)e^{-(n_0 - 1)f}}. \tag{11}$$

This result is plotted in Figs. 2-4 for $r = 0.01$, 0.005, and 0.001, respectively. One can easily obtain the fault coverage from these graphs. For example, if the field reject rate was specified as 1 in 1000, i.e., $r = 0.001$, then from Fig. 4 for

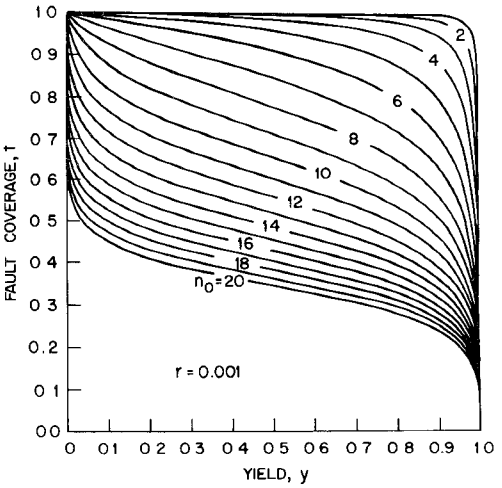

Fig. 4. Fault coverage required for a field reject rate of 1 in 1000.

yield $y = 0.3$ and $n_0 = 8$, the fault coverage should be about 85 percent.

VII. An LSI Example

In this example, we consider an LSI chip containing about 25 000 transistors for which test patterns had been evaluated on the LAMP fault simulator [16]. The results used here were obtained from the testing of wafers on the Fairchild Sentry test system [17]. The yield for this chip was estimated to be about 7 percent. For each chip, the test pattern number on which the chip first failed was recorded. The cumulative number of failing chips as a function of the fault coverage is shown in Table I. The procedure for obtaining the entries in this table can be understood by examining the first line. After the initialization sequence, on the first pattern at which the tester strobed the chip output, 113 of 277 (i.e., 41 percent) chips failed. From fault simulation, the fault coverage on this pattern was obtained as 5 percent. The results of Table I are plotted in Fig. 5, where a family of curves, $P(f)$ versus f for $n_0 = 1$-12, is also plotted. The experimental points closely match the curve corresponding to $n_0 = 8$. Also, if we approximate the slope of $P(f)$ at the origin from the data in the first line in Table I, we get $P'(0) = 0.41/0.05 = 8.2$. Now from (10), $n_0 = 8.2/0.93 = 8.8$.

Taking $n_0 = 8$, we notice from Fig. 2 that for a 1 percent field reject rate, the fault coverage should be about 80 percent. As Fig. 4 indicates, the fault coverage should be improved to 95 percent in order to achieve a field reject rate of 1 in 1000.

The above conclusions differ significantly from those obtained in [6] where the field reject rate was obtained as

$$r = (1 - y)(1 - f).$$

From this formula, for $r = 0.01$, $y = 0.07$, we get $f = 99$ percent and for $r = 0.001$, $f = 99.9$ percent. These fault coverages are significantly higher than those obtained by the analysis presented here and, in fact, represent almost unachievable numbers for LSI circuits. Our analysis would have given similar results for $n_0 = 3$ or 4. But $n_0 = 3$ or 4 produces a $P(f)$ versus f curve which significantly disagrees with the experimental result (see Fig. 5).

TABLE I
Result of Chip Test
Yield ≃ 0.07
Total Number of Chips = 277

Fault Coverage (percent)	Cumulative Number of Chips Failed	Cumulative Fraction of Chips Failed
5	113	0.41
8	134	0.48
10	144	0.52
15	186	0.67
20	209	0.75
30	226	0.82
36	242	0.87
45	251	0.91
50	256	0.92
65	257	0.93

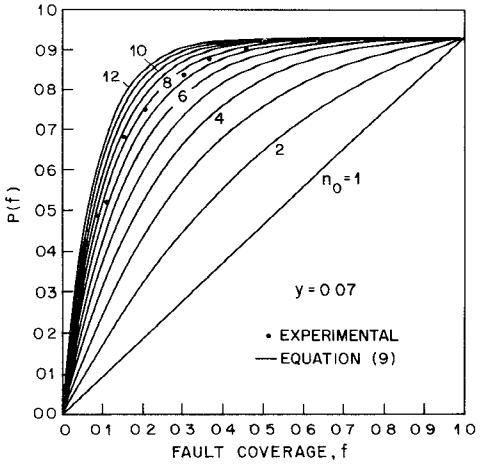

Fig. 5. Determination of n_0 from experimental data.

A large chip can be considered as composed of several smaller chips and thus the average number of faults on a large faulty chip would be higher. Also, for a given chip area, one would expect the average number of logical faults to be higher for greater circuit density (e.g., in the case of fine-line technology). The strength of our model lies in the experimental process by which the model parameter (n_0) is determined for the actual chip being studied. The influence of the fault model used in determining the fault coverage (e.g., stuck type faults) also influences the value of n_0. For instance, let us assume that the tests that detect the stuck type faults detect only very few of the actual fault modes of the chip. As the tests are applied, the chips will be rejected at a slower rate and (see Fig. 5) we will get a smaller value of n_0. This would mean (see Figs. 2-4) that the fault coverage (as measured in terms of stuck type faults) will have to be higher.

VIII. Conclusion

Besides finding the fault coverage requirement for a chip processing line, there are other applications of the technique presented here. One such application is in prediction of the influence of fine-line technology on the testing problem. A given circuit, when implemented with finer design rules, occupies a smaller area. The yield, which largely depends upon the chip area, would be higher. In Figs. 2-4, a higher yield indicates a lower fault coverage requirement if n_0 was kept fixed. However, when the circuit is shrunk into finer features, one should expect many logical faults to be produced by a physical defect. This phenomenon could result in a higher

value of n_0, thereby further reducing the fault coverage requirement.

In our theory, we have introduced a new parameter n_0, the average number of faults on a defective chip. No attempt has been made to relate n_0 to the yield. Yield, which has been extensively studied in the past, is known to depend upon the chip area and the defect density. The average number of faults also depends upon the chip area and defect density. Further work should establish at least an empirical relationship between yield and the average number of faults.

Since the completion of this work, the authors have learned of similar work being pursued elsewhere [18].

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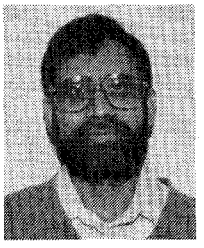

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