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Harmonics Elimination in Three Phase Cascade H-Bridge Multilevel Inverter Using Virtual Stage PWM

Amro Quedan
University of Nebraska-Lincoln, aquedan@huskers.unl.edu

HARMONICS ELIMINATION IN THREE PHASE CASCADE H-BRIDGE MULTILEVEL INVERTER USING VIRTUAL STAGE PWM

By

Amro Quedan

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Amro Quedan, M.S.

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Advisor: Mahmoud Alahmad

The multilevel inverters are one of the great solutions that are proposed to satisfy the demand for high-power application and the significant integration of renewable energy. The conversion process from DC to AC must be done at high efficiency to decrease the energy loss and to ensure the electric grid power quality. The Total Harmonic Distortion (THD) is the most important feature that indicates the efficiency of the conversion process. In this research, due to the advantages of the cascade H-bridge inverter over other topologies, it has been used with the virtual stage PWM technique to investigate two different methods for selective harmonics elimination. The first method is looking from the single-phase perspective, and the second method is looking from the three-phase perspective. A comparison has been done on a wide range of modulation indices using five- and seven- level inverters. The three-phase method provides better results in terms of the THD and the fundamental component. Also, it guarantees the amplitude and shape of output voltage signal in the three-phase application.

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CHAPTER 1

INTRODUCTION

1.1 General

The multilevel inverters are one of the great solutions that are proposed to satisfy the demand for high-power application and the significant integration of renewable energy. In this research, the H-bridge multilevel inverter is used to compare the output voltage quality of two different methods. These methods are used to find the switching angles for the virtual stage PWM modulation technique.

The following chapter contains Section 1.2 that presents the motivation behind this research. Section 1.3 describes the main objective of the thesis. Section 1.4 provides the thesis outline.

1.2 Motivation

In the last few years, there has been a huge development in inverters in either topologies or control. This development has been due to the high demand in power equipment that reaches the megawatts scale. These megawatts applications usually are supplied by medium voltage grids [1]. Also, the recent integration of renewable energy and the large scale of integration that reaches to megawatts is usually connected to medium-voltage distribution networks or sometimes the transmission networks. The power semiconductor devices that typically are used in the industry are insulated gate bipolar transistor (IGBT), integrated gate commutated thyristor (IGCT), and gate turn-off thyristor (GTO) [2]. The maximum rating voltage for a power semiconductor device is around 6.5kV [3], and the ratings for the medium voltage grids range from 2kV to 35kV. Therefore, no power

semiconductor can be directly connected to the grid above 6.5kV. Multilevel inverters have been introduced because of the aforementioned reasons.

In 1975, the concept of the cascade H-bridge (CHB) multilevel inverter was introduced by [4]. Since then, several multilevel inverter (MI) topologies have been proposed, including neutral point clamped (NPC) [5] [6] and flying capacitor (capacitor clamped) [7]. The unique construction of the MI gives it the ability to reach the high-voltage ratings without transformers. Also, it produces an output voltage waveform with low harmonic content. The idea behind the MI is that it accumulates several voltage levels to reach the desirable voltage level. The general shape of the output waveform of the MIs is a staircase. As the steps in the staircase increase, the harmonic contents decrease [1].

The MIs do not just solve the voltage ratings problem; they also provide several advantages over other topologies. The output voltage in the MIs has very low distortion with a reduction of the electromagnetic compatibility problems by reducing the dv/dt stresses. In addition, low distraction in the input current results in a reduction in the total harmonic distortion (THD) and better signal quality. Also, the small production of the common mode (CM) voltage reduces the stress on the motor's bearing. Furthermore, it can be controlled using high and low switching frequency where the latter can provide better efficiency. [8], [9].

1.3 Thesis Objective

The importance of multilevel inverters in the industry is due to the increase in high-power demand and the high integration of renewable energy sources. The MIs structure and control are developed rapidly to improve the power quality and reliability to contribute to this field, this thesis presents an existing modulation, which is the virtual stage PWM

(VSPWM) technique from the three-phase perspective and apply it on a single phase topology the CHB. The three-phase perspective decreases the output voltage THD by 25% in the five-level inverter and by 17% in the seven-level inverter. Also, the three-phase perspective increases the minimum value for the fundamental component by 125% in the five-level inverter and by 38% in the seven-level inverter. This research uses an existing topology, the CHB, due to its advantages over other topologies. Simulations and experiments have been done to validate these improvements, and the Raspberry Pi has been used as the controller for the inverters.

1.4 Thesis Outline

In this chapter, a general idea about multilevel inverter motivation and principle has been presented, as well as advantages of the MIs over other topologies. In addition, the contribution of this thesis has been introduced.

Chapter 2 presents literature review of MIs and their principle function, along with a literature review of the three main topologies of MIs.

Chapter 3 provides the different types of the modulation techniques for MIs and the classification of these techniques.

Chapter 4 introduces the virtual stage PWM for both the five- and seven-level inverters from two perspectives depending on the method used to calculate the unknown angles and, in addition, the derivation of the set of equations that represents it. The chapter also provides the simulation results and analysis.

The purpose of Chapter 5 is to present the experiment methodology and results of the two methods used to calculate the unknown angles to validate the simulation results.

Chapter 6 provides a brief summary of the thesis, and from this summary, the contribution of the thesis is illustrated. Finally, the ongoing work and future suggestions are mentioned.

CHAPTER 2

INVERTER TOPOLOGIES

2.1 General

Increasing demand for electricity and the need for energy independence has led to the fast-growing availability of renewable energy sources, such as solar, wind, bio, and geothermal energy—among others. Due to these growing energy sources, a variety of power converters became common components of the electrical system to achieve their integration into the smart electrical grid. [10]

Generally, the electricity generation is divided into two types: the direct current (DC) generation (i.e., renewable energy systems and batteries) and alternative current (AC) generation (i.e., moving turbine, including steam, fossil fuel, and hydropower). To integrate DC generation with the utility grids, power inverters are needed to convert the DC to AC.

Three main types of inverters have been classified depending on the output waveform: sine wave, square wave, and modified-sine wave. A sine wave inverter converts the DC energy to a near-perfect sine wave—similar to utility grid electricity waveform. This sine wave contains the least amount of THD, which makes it more suitable for sensitive equipment and electronics. This also makes it more expensive than other types. Square wave is the output of typical inverters, where the waveform keeps regularly alternating between positive and negative. The modified square wave looks like a square wave but has an additional step or steps that make it closer to the sine wave shape.

Pure sinusoidal is the ideal inverter output waveform. However, because the sine wave inverter is considered an expensive and complicated solution, the modified sine wave inverter is considered a less expensive and easier solution in most of the applications. Figure 2.1 shows the three different types of the inverter output waveforms [11].

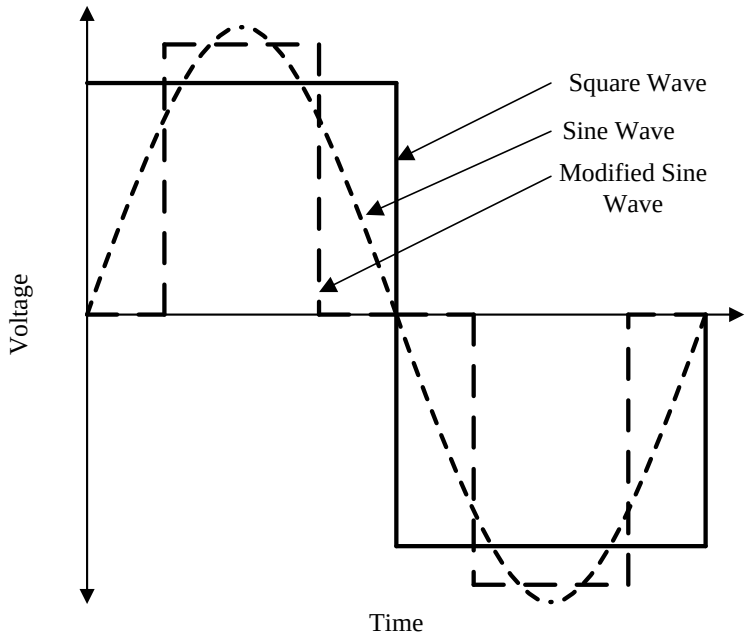

Figure 2.1: Sine, Square, and Modified Sine wave

One of the basic circuits to convert DC to AC is the full-bridge converter. The operation of this circuit depends on the opening and closing sequence of the switches to convert the DC to AC. The output voltage amplitude can be one of the following values: $+V_{dc}$, $-V_{dc}$, and zero depending on each switch position. Table 2.1 shows each switch position and the resultant output voltage. Figure 2.2 shows the coordination of the switches during one full cycle to generate the desirable waveform. Figure 2.3 shows the output voltage waveform generated from the full-bridge converter.

Table 2.1: Full-bridge converter relationships between switches and output voltage

Closed Switches	Open Switches	Output Voltage V_o
S_1 and S_2	S_3 and S_4	$+V_{dc}$
S_3 and S_4	S_1 and S_2	$-V_{dc}$
S_1 and S_3	S_2 and S_4	0
S_2 and S_4	S_1 and S_3	0

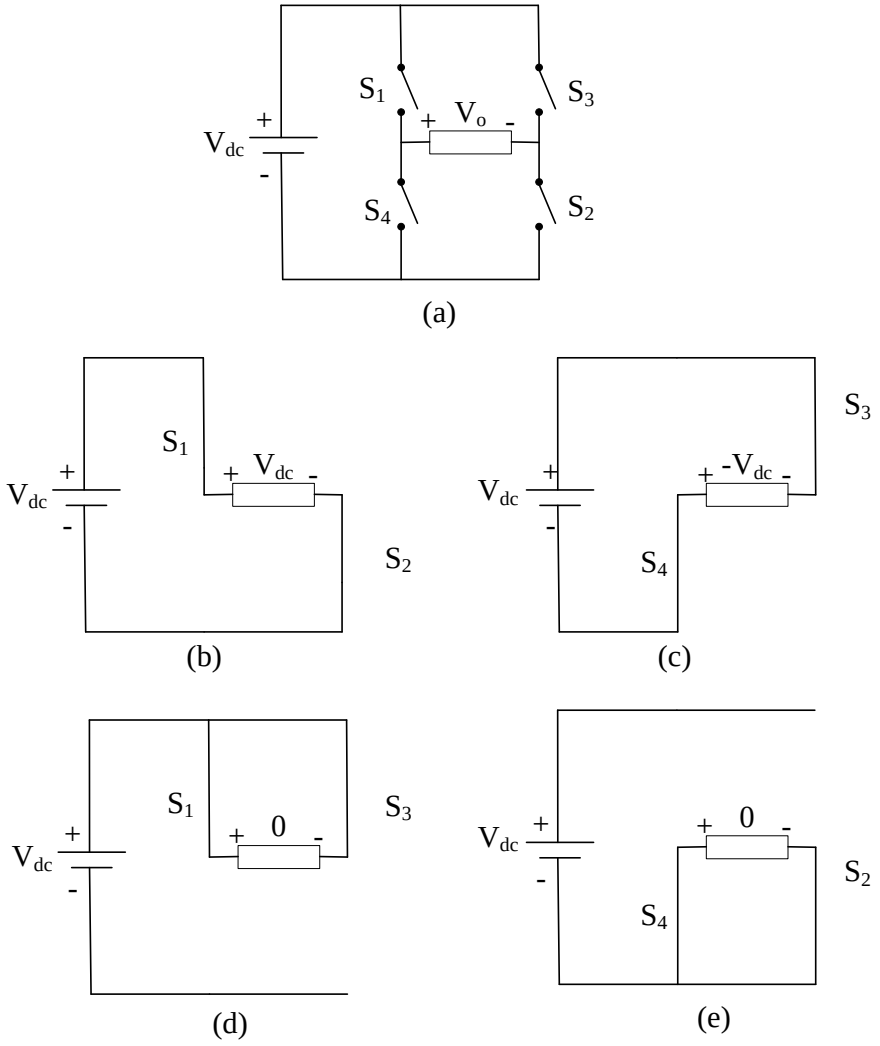

Figure 2.2: (a) Full-bridge converter; (b) S_1 and S_2 closed; (c) S_3 and S_4 closed; (d) S_1 and S_3 closed; (e) S_2 and S_4 closed

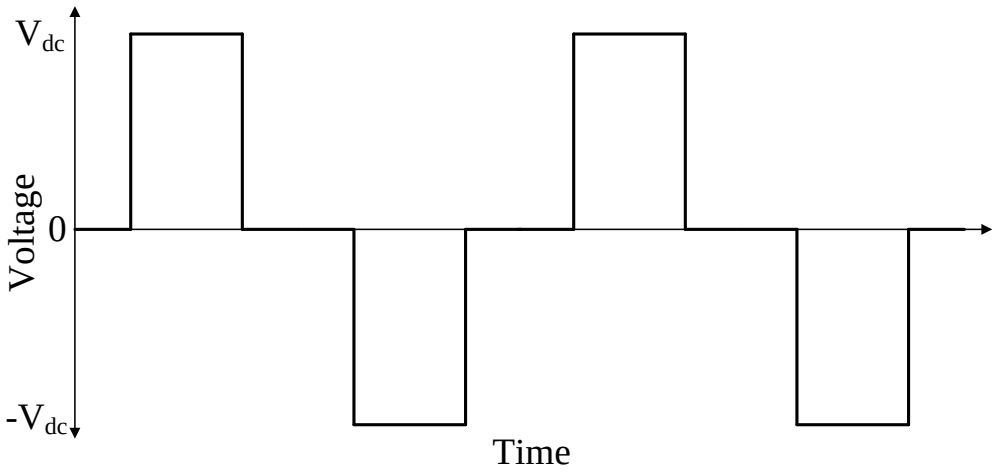

Figure 2.3: Output voltage waveform generated by full-bridge circuit

In all cases, it is prohibited to close S_1 and S_4 and S_2 and S_3 at the same time. If that happens, a short circuit will occur across the DC source. This should be taken into consideration when installing real-time switches in experiments because they will not work instantaneously [12].

In general, there is a contradiction between a “converter” and an “inverter.” A converter refers to the device itself that does the conversion process for the waveform. It operates in two modes depending on the power flow. If it converts the energy from AC to DC, it is called a rectifier. If it converts the energy from the DC to AC, it is called an inverter.

2.2 Multilevel Inverter (MI)

In 1975, the concept of a multilevel inverter (MI) was introduced [4]. It is considered one of the most feasible solutions for medium- and high-power applications.

The semiconductors and the capacitor voltage sources are the main components for MIs and are organized in a way that generates the output voltage in staircase format. The operation of the switches determines the output voltage level depending on its position. Figure 2.4 shows multilevel inverters with one phase leg [13]

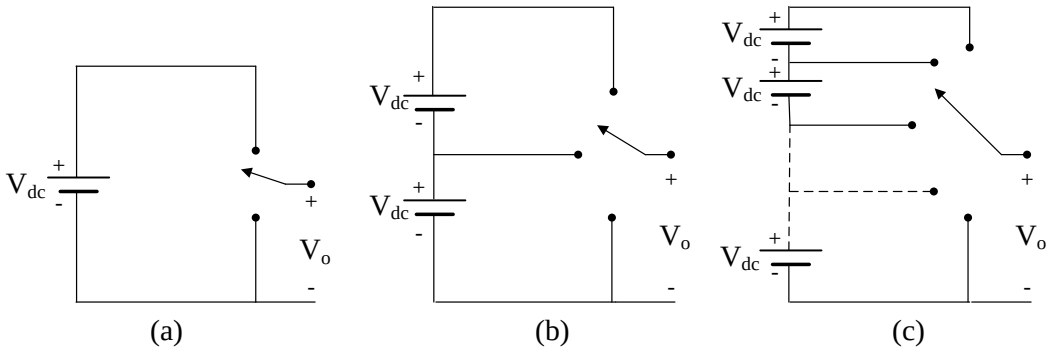

Figure 2.4: a) Two-level inverter; b) three-level inverter; c) n-level inverter [5]

As the number of the levels increases, the output waveform becomes more similar to the desired sine wave. Figure 2.5 shows an 11-level multilevel inverter output voltage.

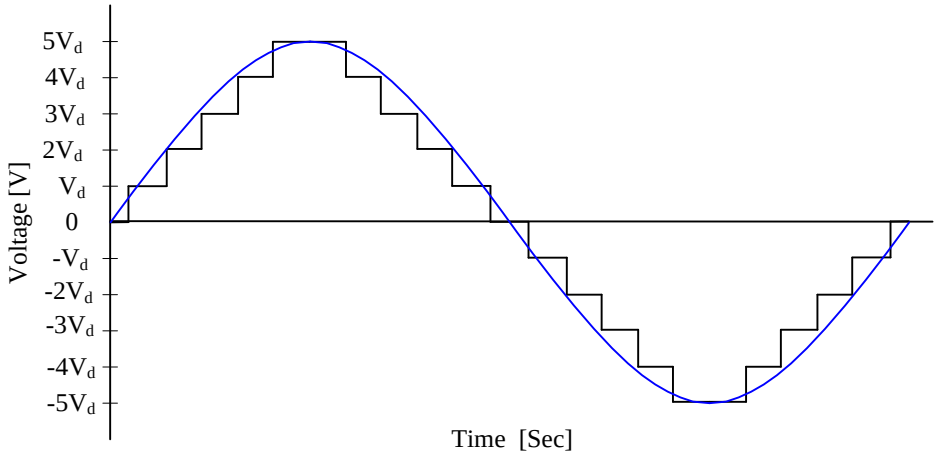

Figure 2.5: Eleven-level multilevel inverter output voltage waveform

The output will not be an exact sine wave despite increasing the number of levels. So, to describe the quality of the output voltage of a nonsinusoidal wave, the term “total harmonic distortion (THD)” has been presented [12].

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty}\left(V_{n,rms}\right)^2}}{V_{1,rms}} = \frac{\sqrt{V_{rms}^2 - V_{1,rms}^2}}{V_{1,rms}} \quad (2.1)$$

Where $V_{n,rms}$ is the voltage rms value at harmonic n, $V_{1,rms}$ is the voltage rms value for the fundamental component and V_{rms} is the output voltage rms value.

The THD for the current depends on the connected load. To find the value of the THD for the current, substitute the voltage by the current using the above equation [12].

The presence of MIs took an important place in industrial applications due to their advantages over other conventional two-level inverters. The output voltage in the MIs has very low distortion with a reduction of the electromagnetic compatibility problems by reducing the dv/dt stresses. Also, low distraction in the input current results in a reduction in the THD and better signal quality [8]. Additionally, the small production of the common mode (CM) voltage reduces the stress on the motor’s bearing [9]. It can also be controlled using high and low switching frequency where the latter can provide better efficiency.

Different topologies have been developed for the multilevel inverters [14] [15] [16] [17] [18] [19] [20] [21]. The main inverters’ topologies are: cascade H-bridge (CHB) with separate DC sources [7] [4], neutral point clamped (NPC) [5] [6], and flying capacitor (capacitor clamped) [7].

In this chapter, the working principle of each inverting topology will be discussed, and the advantages and disadvantages will be illustrated. The CHB will be used in this research due to its advantages over other topologies.

2.2.1 Cascade H-Bridge Inverter

The CHB inverter is the first MI based on semiconductors and was described and constructed by [4]. It was a cascaded topology, which is a serial connection of a one-phase inverter. This MI is based on the series connection of single-phase H-bridge inverters with separate DC sources without clamping diodes or voltage capacitors [7]. Each bridge consists of four switches with their diodes—S_1, S_2, S_3, S_4—and one independent voltage source, "V_d." The voltage sources can include batteries, fuel cells, and solar cells. All the voltage sources have an identical voltage. The output voltage of each bridge can obtain values "$-V_d$," "0," or "$+V_d$." Figure 2.6 illustrates the output voltage from a single H-bridge inverter with a single DC source when considering the normal switch operations as shown in Table 2.2.

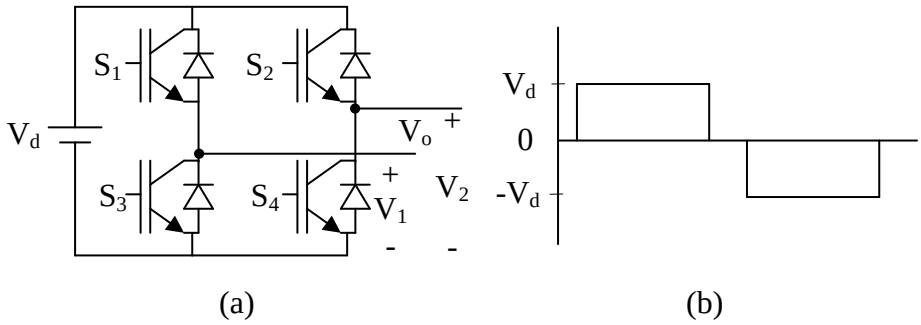

Figure 2.6: CHB circuit (a) single H-bridge inverter with single DC source (b) output voltage from (a)

Table 2.2: Three-level cascaded H-bridge leg relationships between configurations and output voltage

S_1	S_2	S_3	S_4	V_o
1	0	0	1	$-V_d$
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$+V_d$

Increasing the number of levels will smooth the output voltage signal and decrease the total harmonic distortion (THD). In addition, high and low couples of switching can be defined with respect to the voltage output direction. Considering Figure 2.7 with two bridges, the high output of one bridge is a shortcut to the low output of another one, resulting in a cascade connection between two bridges. Each bridge in the cascade adds two more levels to the output waveform. The following equation represents the maximum number of voltage levels that can be generated in the phase voltage from cascaded H-bridge cells, where N is the number of H-bridge cells:

$$V_{ph} = 2 \times N + 1 \qquad (2.2)$$

Figure 2.7 shows the two H-bridge inverter cells cascaded to generate five-level output voltage. Table 2.3 shows the relationship between the transistor on/off situation and the output voltage.

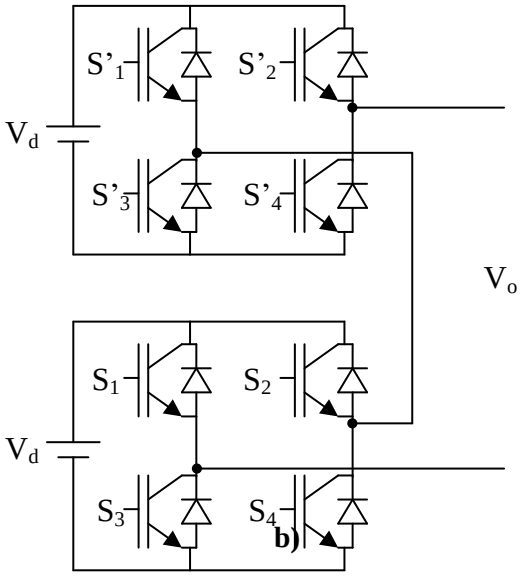

Figure 2.7: Two cascaded H-bridge inverter cells

Figure 2.8 shows the output voltage from the lower cell and the upper cell as well as the resultant output voltage from the whole circuit.

Table 2.3: Five-level cascaded H-bridge leg relationships between configurations and output voltages

The Upper Cell				The Lower Cell				V_{out}
S'_1	S'_2	S'_3	S'_4	S_1	S_2	S_3	S_4	
1	0	0	1	1	0	0	1	$2V_d$
1	1	0	0	1	0	0	1	V_d
1	0	0	1	0	0	1	1	V_d
1	0	0	1	1	1	0	0	V_d
0	0	1	1	1	0	0	1	V_d
1	1	0	0	1	1	0	0	0
1	1	0	0	0	0	1	1	0
1	0	0	1	0	1	1	0	0
0	1	1	0	1	0	0	1	0
0	0	1	1	1	1	0	0	0
0	0	1	1	0	0	1	1	0
0	1	1	0	1	1	0	0	$-V_d$
0	0	1	1	0	1	1	0	$-V_d$
0	1	1	0	0	0	1	1	$-V_d$
1	1	0	0	0	1	1	0	$-V_d$
0	1	1	0	0	1	1	0	$-2V_d$

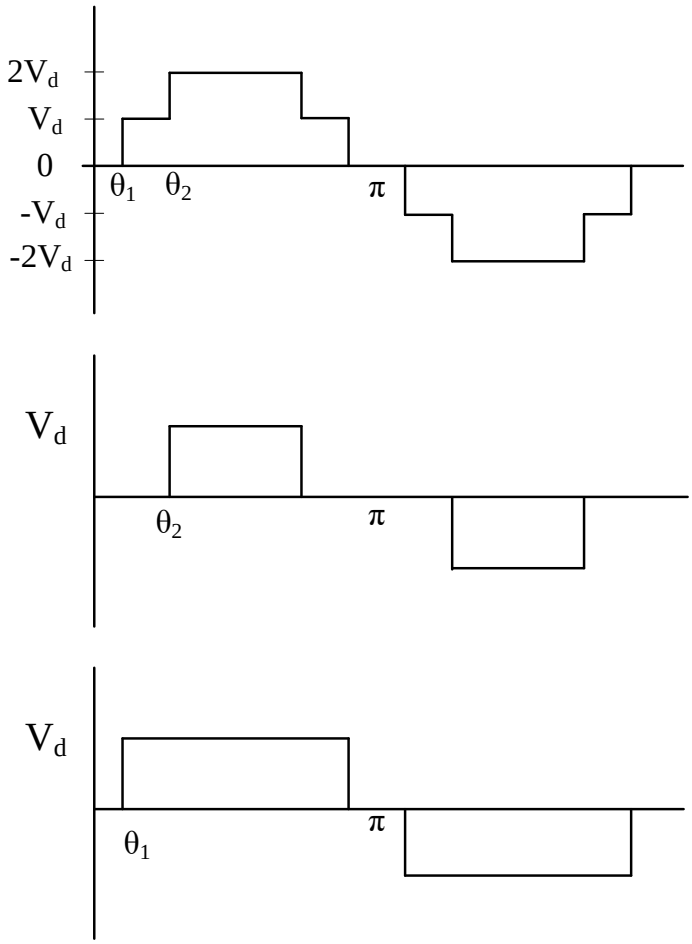

Figure 2.8: Voltage output from the lower cell, upper cell, and total voltage from both cells

The CHB inverter can be connected in a Y or Δ configuration to formulate the three-phase source. Figure 2.9 shows the three-phase Y structure for a five-level CHB inverter [22].

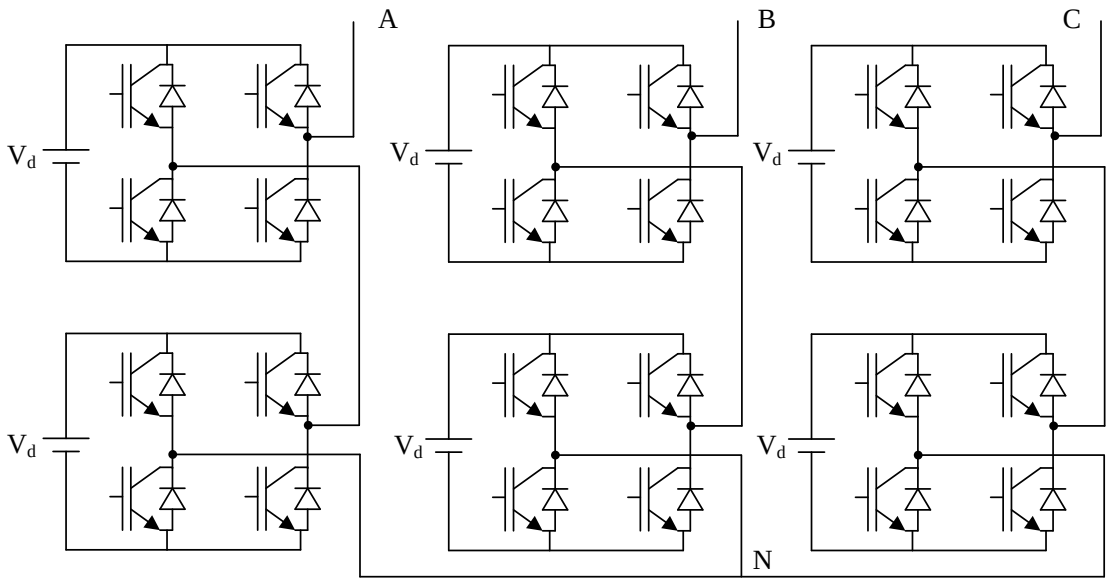

Figure 2.9: Three-phase Y connection structure for five-level cascade H-bridge inverter

The CHB inverter can be considered a suitable solution for many applications due to its advantages over other topologies.

One of the main advantages is the number of the output voltage levels. The number of levels is more than twice the DC source (M = 2*S+1), where S is the number of DC sources. Another advantage from the production point of view is the modularization and packing of the series H-bridge, making it a quicker and less expensive process [7] [23]. Also, it does not require additional clamping diodes or balancing capacitors such as those needed with other topologies [7].

The main disadvantage for the CHB inverter is that it requires separate DC sources. This disadvantage limits the application that it can be used with, mainly the batteries and the photovoltaic panels. However, a new approach has been developed to reduce the number of isolated DC sources by replacing them with capacitors. The proposed approach uses fewer active switches, diodes, capacitors, drivers and DC sources [24]. Also, [25] makes

CHB more suitable for photovoltaic and battery-fed applications. The photovoltaic panels and the batteries can easily be rearranged in several separated sources to feed CHB bridges.

As discussed previously, to increase the output voltage quality, more CHB cells must be used. This increment in the number of CHB cells will increase the number of transistors used. A new topology has been developed to reduce the number of transistors that are used in the CHB inverter. This reduction has been accomplished by replacing some of the transistors with diodes, and it also reduces the total energy loss across the transistors [26].

2.2.2 Diode-Clamped Inverter

In 1980, the diode-clamped multilevel inverter was derived from the cascade inverter [5]. The first proposed diode-clamped inverter was a three-level inverter. The neutral point has been defined to be mid-level voltage; thus, the diode clamp inverter has another name: neutral point clamped (NPC) inverter [13] as shown in Figure 2.10 (a). The first implantation of this topology was done using pulse width modulation (PWM) in 1981 by [6]. Figure 2.10 shows a diode-clamped multilevel inverter with three and five levels.

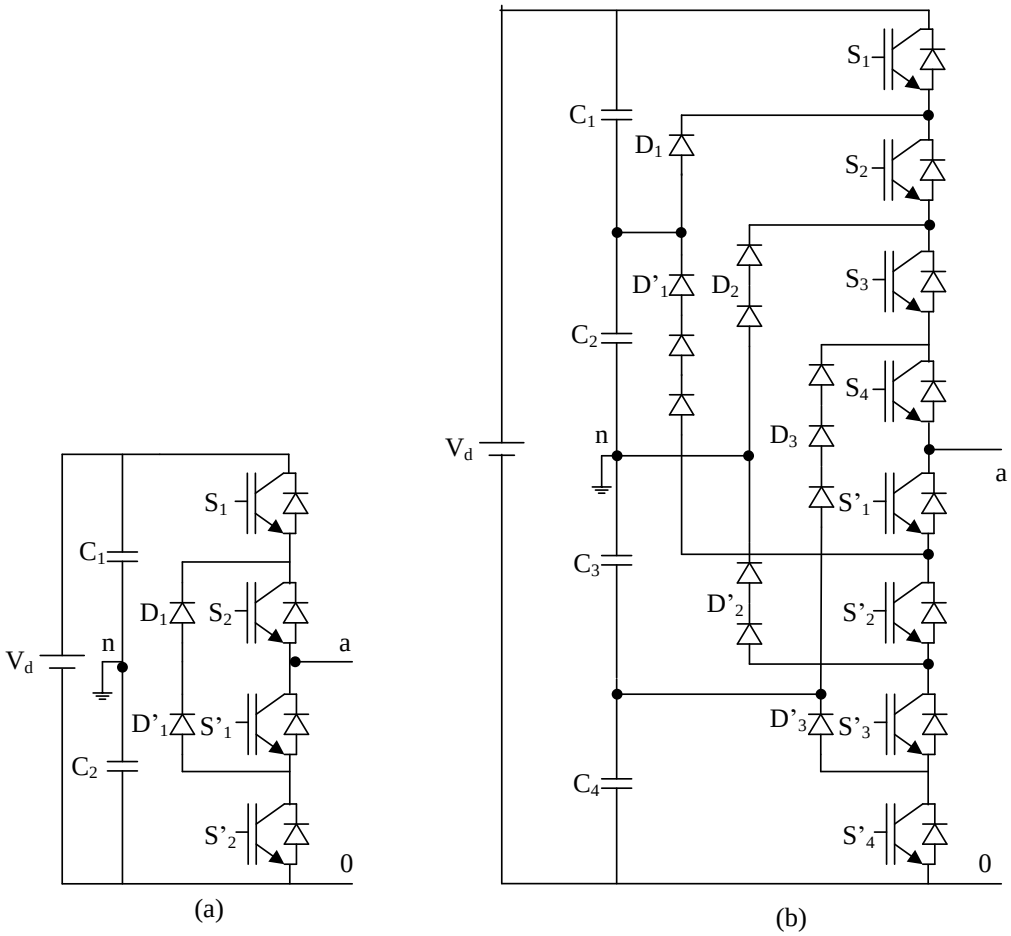

Figure 2.10: Diode-clamped multilevel inverter schematic diagram (a) three-level; (b) five-level [13]

In Figure 2.10 (a), the three-level diode-clamped multilevel inverter contains two bulk series connected capacitors that split the DC bus voltage into three voltage levels. The output voltage V_{an} of this inverter is $V_d/2$, 0, and $-V_d/2$ [13]. Table 2.4 shows the relationship between the output voltage and the on/off status of the switch.

Table 2.4: Diode-clamped three-level inverter voltage levels and corresponding switch states

S_1	S_2	S'_1	S'_2	V_{an}
1	1	0	0	$V_d/2$
0	0	1	1	$-V_d/2$
0	1	1	0	0

What differentiates this topology from others is the implemented diodes that clamp the voltage across switches to half of the DC bus voltage level. In the three-level inverter, as shown in Figure 2.10 (a), if S_1 and S_2 are ON, then V_{a0} will be V_d. In this case, the voltage will be equally distributed between switches S'_1 and S'_2 because of D'_1. Also, the voltage across C_1 will be blocked by switch S'_2, and the voltage across C_2 will be blocked by S'_1. The output AC voltage from the inverter must be taken a V_{an}. Because the output voltage from V_{a0} is DC, it will be a DC/DC converter, not DC/AC inverter. The difference between the two is the voltage across C_2, which is equal to $V_d/2$ [13].

The five-level diode-clamped inverter is shown in Figure 2.10 (b). There are four capacitors parallel with the DC source. The voltage across each capacitor is $V_d/4$ [13]. Table 2.5 shows the relationship between the output voltage and the switch states.

Table 2.5: Diode-clamped five-level inverter voltage levels and corresponding switch states

S1	S2	S3	S4	S'1	S'2	S'3	S'4	V_{an}
1	1	1	1	0	0	0	0	$V_d/2$
0	1	1	1	1	0	0	0	$V_d/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_d/4$
0	0	0	0	1	1	1	1	$-V_d/2$

There are four switch pairs that work in complementary mode in the diode-clamped multilevel inverter: (S_1, S'_1), (S_2, S'_2), (S_3, S'_3), and (S_4, S'_4). If one of them is on, the other is off. In addition, $V_d/(n-1)$ is the required voltage to be blocked by each switch, where n is the number of levels. However, each diode has a different voltage level that needs to be blocked. In the five-level inverter, D'_1 has to block $3V_d/4$, but D_1 needs to block $V_d/4$. D_2 and D'_2 will have the same voltage values, $2V_d/4$. The number of diodes required for each phase in the diode-clamped inverter, taking into consideration that each diode blocks rating voltage the same as the active switch voltage rating, is:

$$N_{diodes} = (n-1) \times (n-2) \quad (2.3)$$

The number of diodes increases quadratically as the number of levels increase, which makes it very difficult to build. Also, with high-voltage, high-power application, the reverse recovery time for the diode will be the major issue in the design, especially when it runs under PWM [13]. Another disadvantage of the diode-clamped inverter is the lack of monitoring and control that makes the real power flow difficult in a certain inverter [7].

An advantage of the diode-clamped multilevel inverter is the presence of the capacitors, which allows a control for the reactive power flow. In addition, fundamental switching

frequency will provide high efficiency because all the devices operate at low frequency [7].

2.2.3 Capacitor-Clamped Inverter

In 1992, the capacitor-clamped multilevel inverter was introduced [27]. The difference between the capacitor-clamped inverter circuit and the diode-clamped circuit is that capacitors have been used instead of diodes. Each capacitor leg has its own voltage that determines the voltage level for each step [8]. Figure 2.11 shows capacitor-clamped multilevel inverter schematic diagrams for three and five levels.

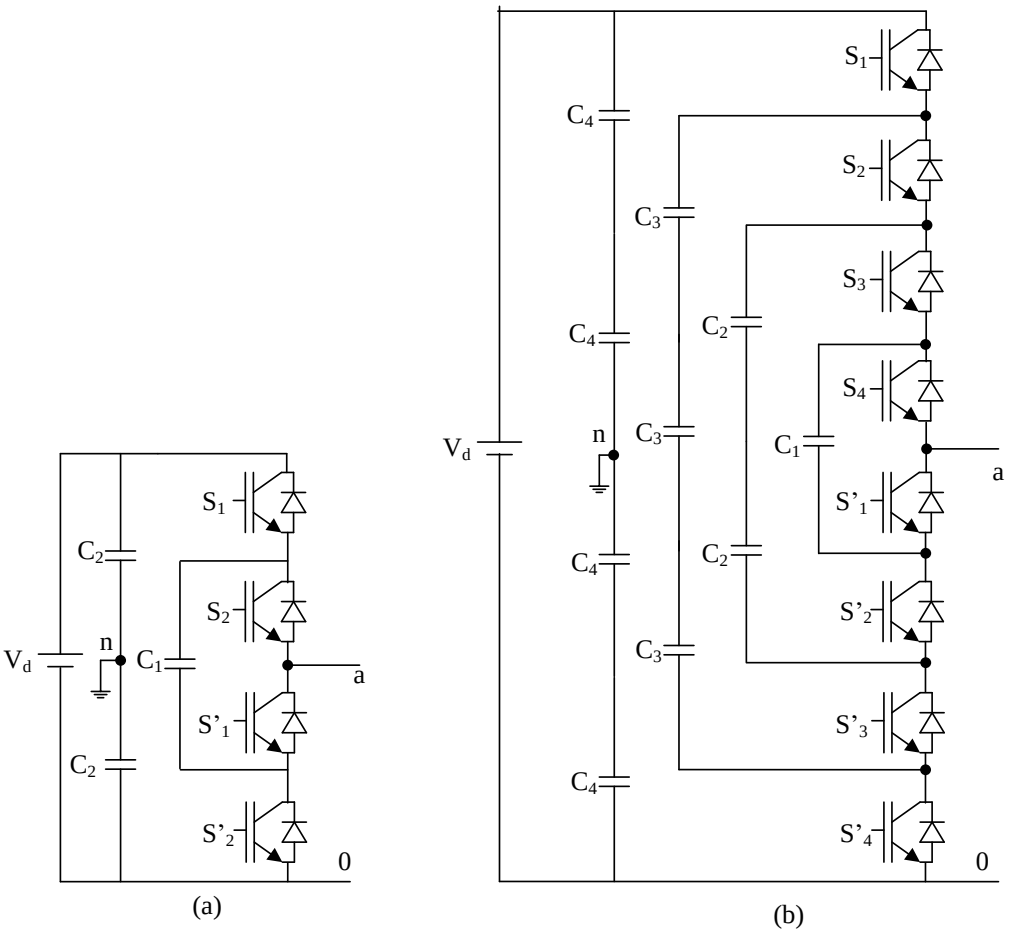

Figure 2.11: Capacitor-clamped multilevel inverter schematic diagram (a) three-level; (b) five-level [13]

The three-level capacitor-clamped inverter will generate three voltage levels across a and n. V_{an} = Vd/2, 0, and -V_d/2. Table 2.6 shows the relationship between the output voltage and switch states for a three-level capacitor-clamped inverter.

Table 2.6: Capacitor-clamped three-level inverter voltage levels and corresponding switch states

S_1	S_2	S'_1	S'_2	V_{an}
1	1	0	0	$V_d/2$
0	0	1	1	$-V_d/2$
1	0	1	0	0
0	1	0	1	0

Turning on S_1 and S'_1 will charge clamping capacitor C_1. Turning on S_2 and S'_2 will discharge clamping capacitor C_1. The zero-level combination will affect the charging balance of C_1, so it should be selected carefully [13].

A more flexible combination can be found for a dedicated voltage level in the capacitor-clamped inverter compared with the diode-clamped inverter. Table 2.7 shows the relationship between the output voltage and switch states for a five-level capacitor-clamped inverter.

Table 2.7: Capacitor-clamped five-level inverter voltage levels and corresponding switch states

S1	S2	S3	S4	S'1	S'2	S'3	S'4	V_{an}
1	1	1	1	0	0	0	0	$V_d/2$
1	1	1	0	1	0	0	0	$V_d/4$
0	1	1	1	0	0	0	1	$V_d/4$
1	0	1	1	0	0	1	0	$V_d/4$
1	1	0	0	1	1	0	0	0
0	0	1	1	0	0	1	1	0
1	0	1	0	1	0	1	0	0
1	0	0	1	0	1	1	0	0
0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	0	1	0
1	0	0	0	1	1	1	0	$-V_d/4$
0	0	0	1	0	1	1	1	$-V_d/4$
0	0	1	0	1	0	1	1	$-V_d/4$
0	0	0	0	1	1	1	1	$-V_d/2$

In the capacitor-clamped multilevel inverter, the number of capacitors needed depends on the number of levels. Equation (2.3) expresses the required number of capacitors needed in the capacitor-clamped inverter per phase [13].

$$N_{capacitors} = (n-1) + \frac{(n-1) \times (n-2)}{2} \tag{2.4}$$

The large amount of capacitors can provide large storage that gives extra time during a power outage and gets over voltage sags. However, the increment in the voltage levels will require a higher number of capacitors, which makes the inverter packaging very difficult and very expensive [7].

The capacitor-clamped multilevel inverter is a good option for the high-voltage DC transmission because the flow for both the real and the reactive power are controllable. On the other hand, in the real power transmission, the inverter requires a high switching frequency that increases the switching losses and control complexity [7].

2.3 Conclusion

The multilevel inverter development has been progressing since 1975 when the first topology was presented in because of its advantages over other types of inverters [4]. Also, the high integration of renewable energy sources to the grid and the electric vehicle existence speeds the development to achieve better performance and reliability of this type of inverter.

The working principle of the cascade H-bridge (CHB), diode-clamped, and capacitor-clamped topologies was discussed in this chapter. Also, the advantages and disadvantages of each of the three main topologies of the multilevel inverters have been presented.

CHAPTER 3

MIs MODULATION TECHNIQUES

3.1 General

In Chapter 2, the construction and the operation principle of the three main multilevel inverter topologies were illustrated. The relationships between switch states and the desired output voltage level were presented in Tables 2.2-2.7. To control the switch state of 1 or 0, several modulation techniques were developed. They have been modified from the conventional inverters to be used in the multilevel inverters and were classified depending on their switching frequency, as shown in Figure 3.1 [8].

This chapter will discuss the modulation techniques used for the MIs.

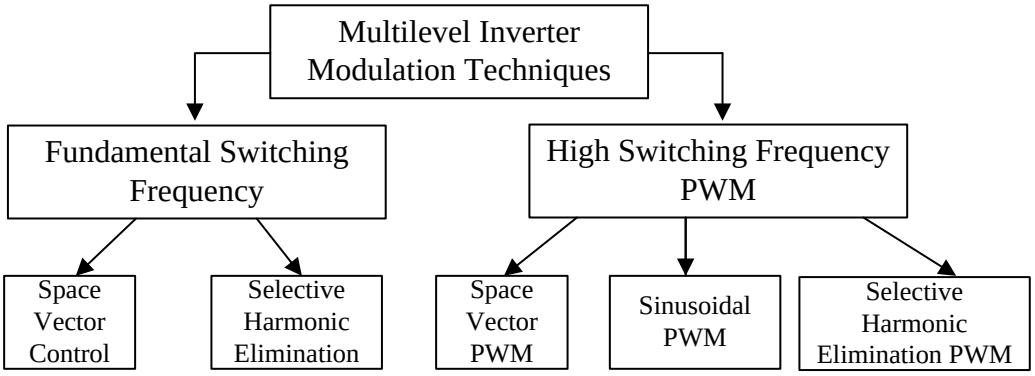

Figure 3.1: Multilevel inverter PWM modulation techniques

3.2 Fundamental Switching Frequency

3.2.1 Space Vector Control (SVC)

The space vector control (SVC) modulation technique works with low switching frequency; it is presented using (d-q) complex plane. This plane is divided into several hexagonal zones [28].

The generated voltage vector by an inverter can be expressed in the following equation:

$$v(t) = \frac{2}{3} \times \left(v_{AN}(t) + a.v_{BN}(t) + a^2 v_{CN}(t)\right) \quad (3.1)$$

Where v_{AN} , v_{BN}, and v_{CN} are the voltages between the terminals A, B, and C with respect to neutral N and *a* is the complex operator [28]:

$$a = -\frac{1}{2} + j\,\frac{\sqrt{3}}{2} \quad (3.2)$$

The voltage vector representation in the complex plane can be expressed by:

$$v(t) = v_d + j\,v_q \quad (3.3)$$

Where:

$$v_d = \frac{1}{3} \times (2 \times v_{AN} - v_{BN} - v_{CN}) \quad (3.4)$$

$$v_q = \frac{1}{\sqrt{3}} \times (v_{BN} - v_{CN}) \quad (3.5)$$

The SVC technique selects a voltage vector (V_c) that is the nearest to the reference voltage vector (V_{ref}) to minimize the space error and reduce the modulation scheme complexity. To make the best selection, the real and the imaginary parts of the reference voltage are

used to locate the reference voltage in a certain hexagon, so the selected voltage vector must be in the area with the best proximity to the reference [28], as shown in Figure 3.2.

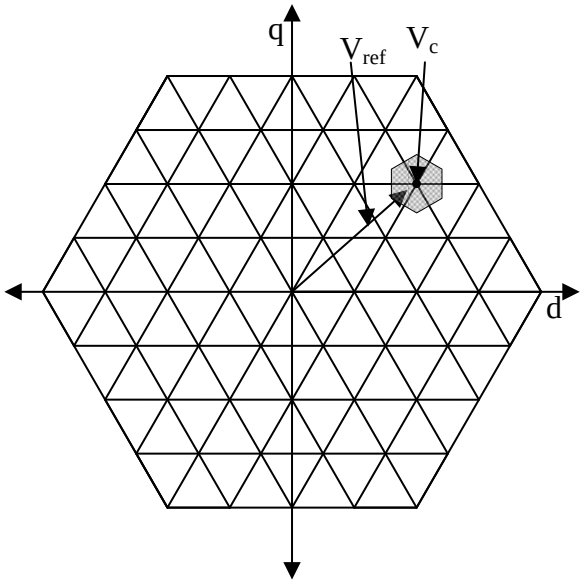

Figure 3.2: Load voltage space vector generated by five-level inverter

This method is more appropriate for inverters with a higher number of voltage levels. The errors will be small in comparison to the reference vector [13].

3.2.2 Selective Harmonic Elimination

In this type of modulation, the fundamental frequency is the same as the switching frequency. The output voltage signal is a staircase, as shown in Figure 3.3 for a five-level inverter. The duration of each step depends on its conducting angle θ_1, θ_2, θ_3, … that is found depending on the eliminated harmonic component. This section presents two methods to find the unknown angles. The first method uses $\pi/2$ interval for a single-phase perspective. The second method uses $\pi/3$ interval for a three-phase perspective.

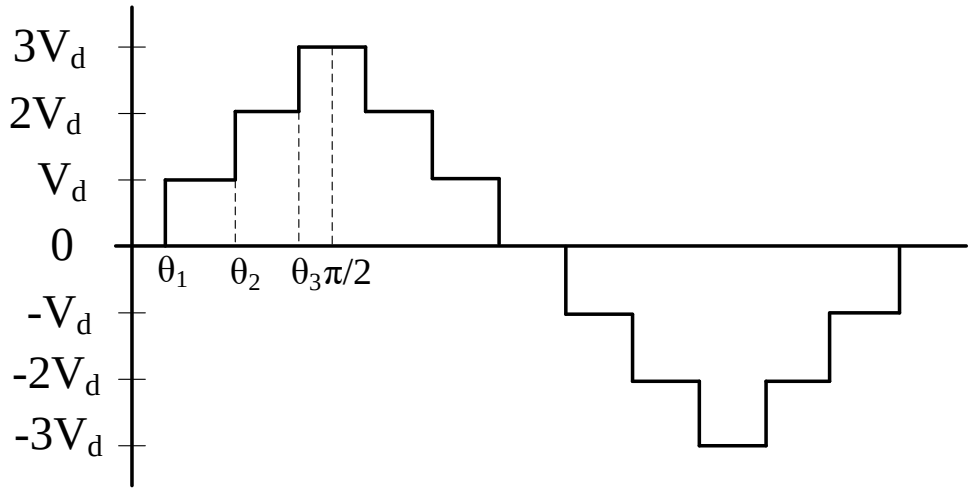

Figure 3.3: Five-level multilevel inverter output voltage signal fundamental frequency modulation

3.2.2.1 Selective Harmonic Elimination Using π/2 Method

Any periodic signal including the output voltage from the multilevel inverter that uses the fundamental switching frequency can be expressed using the Fourier series expansion [29]:

$$v_o(t) = a_v + \sum_{n=1,2,3,4.....}^{\infty} a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t) \tag{3.6}$$

Where $a_v, a_n \; and \; b_n$ are the Fourier coefficients.

$$a_v = \frac{1}{T} \int_{t_0}^{t_0+T} v_o(t)\, dt \tag{3.7}$$

$$a_n = \frac{2}{T} \int_{t_0}^{t_0+T} v_o(t) \cos(n\omega_0 t) dt \tag{3.8}$$

$$b_n = \frac{2}{T}\int_{t_0}^{t_0+T} v_o(t)\, sin(n\omega_0 t)dt \tag{3.9}$$

Where t_o is the time reference, and T is the fundamental period of $v_o(t)$.

To simplify the Fourier series, coefficient multiple symmetries will be taken into consideration for the sine wave odd symmetry, half-wave symmetry, and the odd quarter-wave symmetry.

1- Odd symmetry

If the periodic function has an odd symmetry, the following occurs:

$$f(t) = -f(-t) \tag{3.10}$$

Due to this property, the Fourier series coefficient will be [29]:

$$a_v = 0 \tag{3.11}$$

$$a_n = 0, for\ all\ n \tag{3.12}$$

$$b_n = \frac{4}{T}\int_{0}^{T/2} v_o(t)\, sin(n\omega_0 t)dt \tag{3.13}$$

2- Half-wave symmetry

If the periodic function satisfies equation (3.14), it has a half-wave symmetry:

$$f(t) = -f(t - T/2) \tag{3.14}$$

Due to this property, the Fourier series coefficient will be [29]:

$$a_v = 0 \tag{3.15}$$

$$a_n = 0, for\ all\ n\ even \tag{3.16}$$

$$a_n = \frac{4}{T}\int_0^{T/2} v_o(t)\, cos(n\omega_0 t)dt \;\; for\ all\ n\ odd \tag{3.17}$$

$$b_n = 0, for\ all\ n\ even \tag{3.18}$$

$$b_n = \frac{4}{T}\int_0^{T/2} v_o(t)\, sin(n\omega_0 t)dt \;\; for\ all\ n\ odd \tag{3.19}$$

3- Quarter-wave symmetry

If the periodic function has a half-wave symmetry and symmetry around the midpoint of the positive and negative half-cycle, it has quarter-wave symmetry. So, the Fourier series coefficient becomes [29]:

$$a_v = 0, because\ the\ function\ is\ odd$$

$$a_n = 0, for\ all\ n\ because\ the\ function\ is\ odd$$

$$b_n = 0, for\ all\ n\ even, because\ of\ half\ wave\ symmetry$$

$$b_n = \frac{8}{T}\int_0^{T/4} v_o(t)\, sin(n\omega_0 t)dt \;\; for\ all\ n\ odd \tag{3.20}$$

Due to the above symmetries, the Fourier expression can be conveyed as in equation (3.21) because of the wave symmetry (0, π/2) [29].

$$v_o(t) = \frac{4V_{dc}}{\pi n} \sum_{n=1,3,5,7,\ldots..}^{\infty} [\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cdots] \times \sin(n\omega_0 t) \tag{3.21}$$

The values for θ_1, θ_2, and θ_3 can be chosen to eliminate the lower frequency harmonics or to get the minimum total harmonic distortion (THD) [30].

The number of the eliminated harmonics is equal to:

$$N_{Eliminated\ harm} = N_{conducting\ angles} - 1 \tag{3.22}$$

For example, to eliminate the fifth and seventh harmonic in the five-level MI, the following set of equations are solved using the Newton-Raphson method.

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \tag{3.23}$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \tag{3.24}$$

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = 2 * m_a \tag{3.25}$$

$$m_a = \frac{V_L^*}{V_{Lmax}} \tag{3.26}$$

Where m_a is the modulation index, V_L^* is the amplitude command of the inverter for a sine wave output phase voltage, and V_{Lmax} is the maximum output voltage from the multilevel inverter [8].

All of the above derivations are based on a single-phase perspective due to the single-phase output voltage symmetry properties.

3.2.2.2 Selective Harmonic Elimination Using π/3 Method

From a three-phase perspective, several properties can be found that provide a narrower interval to find a solution to the above set of equations. So, instead of looking (0, π/2), it

will be (0, π/3). The steps are shown as follows. Start by listing the properties and characteristics of the ideal voltage waveform of the three balanced voltages as shown in Figure 3.4 [31]:

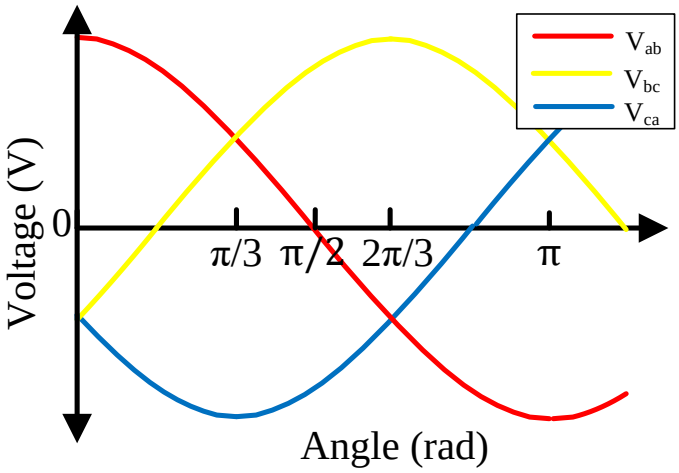

Figure 3.4: Three line to line voltage waveforms in a three-phase system

1. Property (1): v_{ab} is an even function with respect to zero

   For every $\theta \left[0, \frac{\pi}{2}\right], v_{ab}(-\theta) = v_{ab}(\theta)$

2. Property (2): v_{ab} is an odd function with respect to π/2

   For every $\theta \in \left[0, \frac{\pi}{2}\right], v_{ab}\left(\frac{\pi}{2} + \theta\right) = -v_{ab}\left(\frac{\pi}{2} - \theta\right)$

3. Property (3): v_{bc} is symmetrical to $v_{ab}$with respect to π/3

   For every $\theta \in \left[0, \frac{\pi}{3}\right], v_{bc}\left(\frac{\pi}{3} + \theta\right) = -v_{ab}\left(\frac{\pi}{3} - \theta\right)$

4. Property (4): v_{ca} is an inverted and shifted version of v_{ab}

   For every $\theta \in \left[0, \frac{\pi}{3}\right], v_{ca}\left(\frac{\pi}{3} + \theta\right) = -v_{ab}(\theta)$

5. Property (5): v_{ab}, v_{bc}, and v_{ca} are balanced three-phase voltages

   For every $\theta \in [0\,, 2\pi]$, $v_{ab}(\theta) + v_{bc}(\theta) + v_{ca}(\theta) = 0$

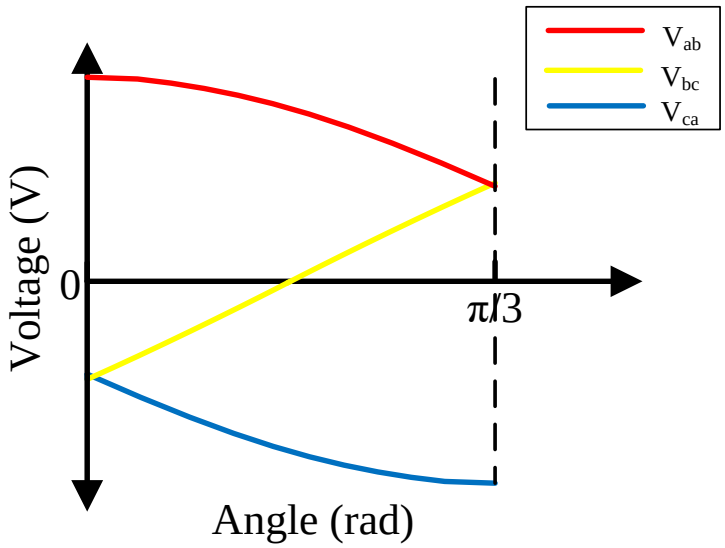

Figure 3.5: Ideal balanced three-phase system in interval (0, π/3)

Assign the above properties of the ideal voltage waveform of the three balanced voltages to the inverter's output voltage by focusing on the (0, π/3) range as shown in Figure 3.5. Also, use the Fourier coefficients of the phase-to-phase output voltage given by (3.27-3.28) because it is well-known that each periodic function of variable can be composed of a set of sine and cosine functions [31]:

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} v_{ab}(\theta).\cos(n\theta)d\theta \tag{3.27}$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} v_{ab}(\theta).\sin(n\theta)d\theta \tag{3.28}$$

Use property (1) and apply it to the Fourier coefficients to become:

$$a_n = \frac{2}{\pi}\int_0^{\pi} v_{ab}(\theta).\cos(n\theta)d\theta \tag{3.29}$$

$$b_n = 0 \tag{3.30}$$

Use property (2) and apply it to the Fourier coefficients to become:

$$a_n = 0 \; for \; n \; is \; even \tag{3.31}$$

$$a_n = \frac{4}{\pi}\int_0^{\pi/2} v_{ab}(\theta).\cos(n\theta)d\theta \;\; for \; n \; is \; odd \tag{3.32}$$

Use property [5] and apply it to the Fourier coefficients to become:

$$a_n = \frac{4}{\pi}\left[\int_0^{\pi/3} v_{ab}(\theta).\cos(n\theta)d\theta - \int_{\pi/3}^{\pi/2}\left(v_{bc}(\theta) + v_{ca}(\theta)\right).\cos(n\theta)d\theta\right] \tag{3.33}$$

Use properties (3) and (4) and apply them to the Fourier coefficients to become:

$$a_n = \frac{4}{\pi}\left[\int_0^{\pi/3} v_{ab}(\theta).\cos(n\theta)d\theta - \int_{\pi/3}^{\pi/2}\left(v_{bc}\left(\frac{2\pi}{3}-\theta\right) + v_{ca}\left(\theta - \frac{\pi}{3}\right)\right).\cos(n\theta)d\theta\right] \tag{3.34}$$

Due to the above three-phase output voltage properties and after some mathematical manipulation, the following occur [31]:

$$a_n = \frac{8}{\pi}\cos\left(n\frac{\pi}{6}\right)\int_0^{\pi/3} v_{\varphi-\varphi}(\theta)\cos\left(n\left(\frac{\pi}{6}+\theta\right)\right)d\theta \tag{3.35}$$

$$b_n = 0 \tag{3.36}$$

Where *n* is the odd and non-triple harmonics and $v_{\varphi-\varphi}$ is line-to-line voltage.

All even harmonics will be zero in both the single-phase and the three-phase output voltage waveform, but all of the triple harmonics will be zero only in the three-phase output voltage because they will be canceled for each phase-to-phase signal.

3.3 High Switching Frequency

3.3.1 Space Vector PWM (SVPWM)

The space vector PWM (SVPWM) method generates the desired mean load voltage value in every switching interval. Figure 3.6 shows a space vector diagram for two- and three-level inverters.

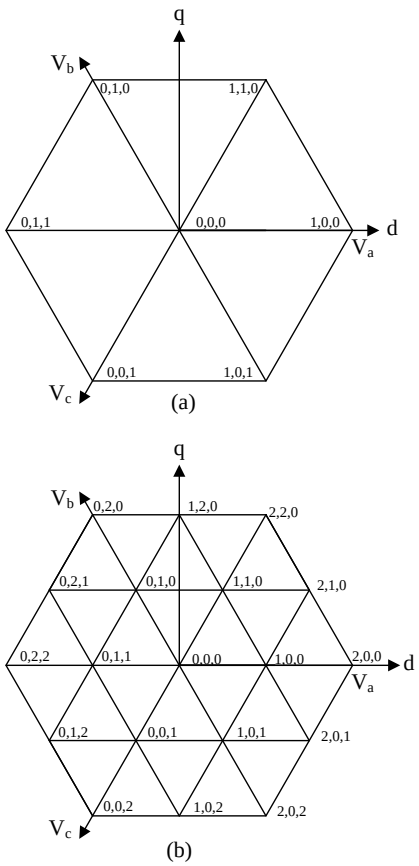

Figure 3.6: Space vector diagram for (a) two-level inverter; (b) three-level inverter

The three-phase output voltages are represented by certain points in the space vector diagram depending on the inverter state. For point (2,1,0) in Figure 3.6 (b), $V_a = 2\ V_{dc}$, $V_b = 1V_{dc}$, and $V_c = 0$ with respect to ground. Figure 3.7 shows the states of the switches on a three-level DC-link referring to this switching combination.

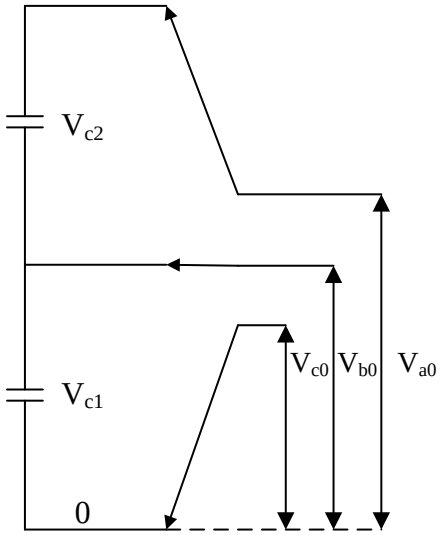

Figure 3.7: Three-level DC-link

The algebraic representation for the output voltages and the switching states are presented in the following equation [32]:

$$V_{abc0} = H_{abc}V_c \tag{3.37}$$

Where:

$$V_c = [V_{c1} \quad V_{c2} \quad V_{c3} \quad \cdots \quad V_{cm}]^T, H_{abc} = \begin{bmatrix} h_{a1} & h_{a2} & h_{a3} & \dots & h_{am} \\ h_{b1} & h_{b2} & h_{b2} & \dots & h_{bm} \\ h_{c1} & h_{c2} & h_{c2} & \dots & h_{cm} \end{bmatrix}, \text{and}$$

$$h_{aj} = \sum_{0}^{m} \delta(h_a - t)$$

ha represents the switch state, and *t* represents an integer from 0 to *m*. If *(ha-t)* ≥ 0, then *δ(ha-t)* = 1; if *(ha-t)* < 0, then *δ(ha-t)* = 0, where m = n-1 and *n* is the number of levels in the inverter.

The available unique switching combination in the n-level multilevel inverter is equal to:

$$N_{unique\ switching\ comb} = n^3 - (n-1)^3 \quad (3.38)$$

Thus, the number of repetitions in the switching combination is equal to $(n-1)^3$. In the three-level inverter, there are 19 unique switching combinations and 27 total combinations.

The repetition in the switching states helps control the charging and discharging of the capacitors and provides the DC-link with good utilization. In addition, a low-ripple output current is generated. These two features make this technique more suitable for the high-voltage application. [8]

From a hardware perspective, the implementation of the SVPWM is considered easy using digital signal processing (DSP) [8]. But, as the number of the inverter levels increases, the implementation becomes harder because the switching states increase, the number of calculations increase, and the sample time becomes shorter. To reduce calculation numbers, a new set of model predictive control (MPC) has been proposed in [33], where only three-voltage vectors are considered depending on the reference voltage.

3.3.2 Sinusoidal PWM (SPWM)

The pulse width modulation technique generates pulse train with pulse widths proportional to a control signal. In the sinusoidal PWM (SPWM), the control signal will be sinusoid, and the average voltage of the generated signal varies sinusoidally. Also, the output

waveform fundamental frequency is equal to the control signal frequency but contains harmonic components [34]. The generated signal is an output of a comparator that is the difference between two signals. The first signal is the control signal, and the second signal is the carrier signal. There are two switching schemes for this type of modulation: bipolar switching and unipolar switching.

In bipolar switching, the output alternates between the $+V_{dc}$ and $-V_{dc}$. If the reference signal is larger than the carrier signal, the output is $+V_{dc}$; when the reference signal is less than the carrier signal, the output is $-V_{dc}$ [12].

In unipolar switching, the output varies from zero to high or from low to zero, but no variation will be between high and low. Figure 3.8 shows the unipolar SPWM applied to the H-bridge shown in Figure 2.6(a), where the output voltage is $V_o = V_1 - V_2$ [12].

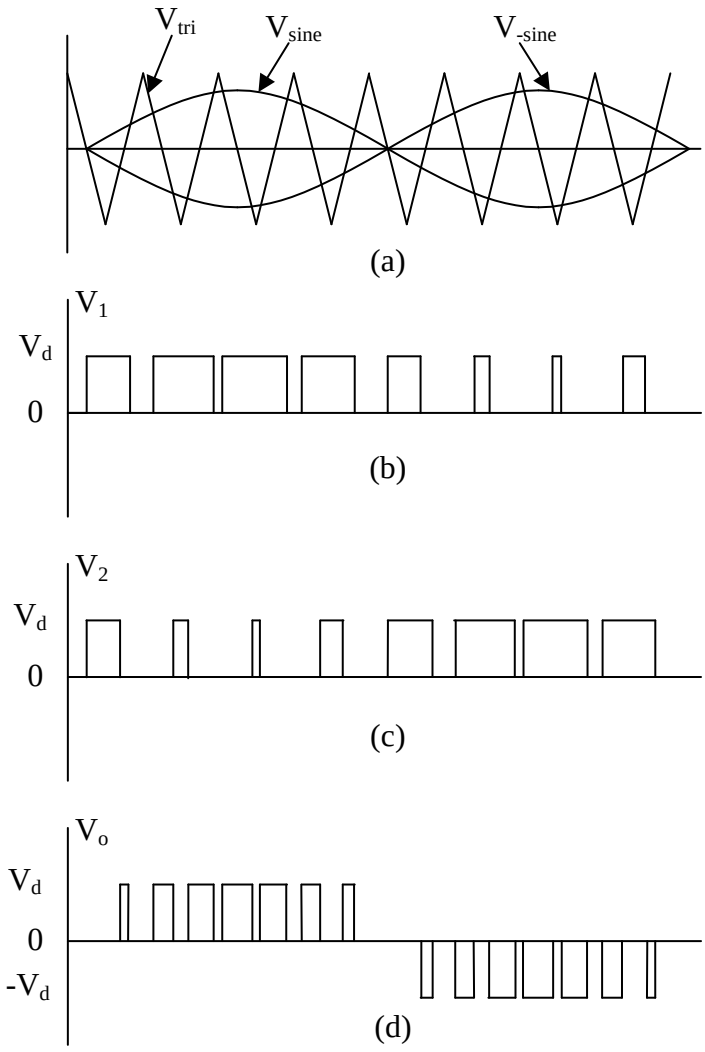

Figure 3.8: (a) Carrier and reference voltage signals; (b) leg 1 output voltage; (c) leg 2 output voltage; (d) H-bridge output voltage

There are harmonic components in the generated signal. These components are multiples of the fundamental frequency. A low pass filter can be used to remove the undesired harmonic components because most of them are in the high frequency regions. The frequency modulation m_f is the ratio between the carrier signal frequency $f_{carrier}$ and the reference signal frequency $f_{reference}$ given in the following equation [12]:

$$m_f = \frac{f_{carrier}}{f_{reference}} = \frac{f_{tri}}{f_{sine}} \tag{3.39}$$

As the frequency modulation ratio increases, the occurrence of harmonic component frequencies increases, which makes it easier to be filtered. To increase the frequency modulation ratio, the carrier frequency must increase, but that increases the loss in the switches [12].

The amplitude modulation ratio m_a is one of the most important factors that must be defined in the PWM. It is the ratio between the reference signal amplitude $V_{m,reference}$ and the carrier signal amplitude $V_{m,carrier}$ [12].

$$m_a = \frac{V_{m,reference}}{V_{m,carrier}} = \frac{V_{m,sine}}{f_{m,tri}} \tag{3.40}$$

The amplitude of the fundamental frequency depends on m_a. If $m_a \leq 1$, the fundamental frequency amplitude is equal to [12]:

$$V_{fund} = m_a \times V_d \tag{3.41}$$

If $m_a > 1$, the relationship between m_a and the fundamental frequency will not be a linear relationship.

3.3.3 Selective Harmonic Elimination PWM

In the fundamental switching frequency, the number of the eliminated harmonics is dependent on the number of DC sources. The multilevel inverter hardware cost affects its usage in comparison with the conventional two-level inverters. Also, the achievement of low THD and the increment in the number of the eliminated low order harmonics in the

two-level conventional inverters needs high switching frequency that causes a high switching losses [35]. A generalized harmonic modulation method called virtual stage PWM [35] has been developed to minimize the THD in the multilevel inverters. The virtual stage PWM decreases the THD and increases the number of the eliminated low order harmonics using the same number of levels. Also, it uses lower switching frequency than is used in the conventional two-level inverters, which significantly decreases the switching losses.

A combination of the unipolar PWM and the fundamental frequency switching is used to formalize the virtual PWM [35]. Figure 3.9 shows a five-level single-phase output waveform of the virtual stage PWM control. One DC source is used when the unipolar PWM is implemented on a multilevel inverter. The output voltage waveform depends on the "on" and "off" number of switching times during one fundamental cycle.

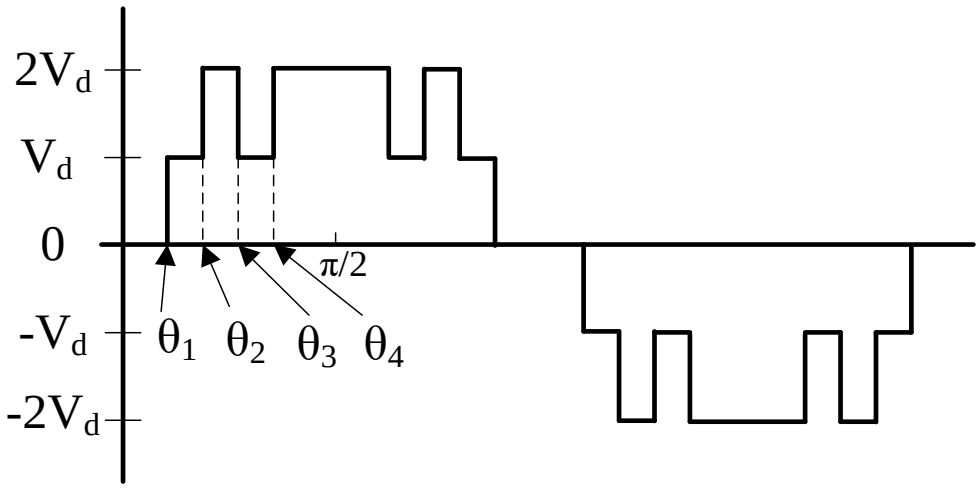

Figure 3.9: Five-level single-phase output voltage waveform of the virtual stage PWM control

In both the fundamental frequency and the PWM selective harmonic elimination methods, a set of equations must be developed to find the unknown angles depending on the eliminated harmonics.

To solve this set of equations, a good initial guess is needed by applying Newton's method, but sometimes it cannot be solved [36]. The resultant method has been presented in [37] [38] [39] to solve this set of equations to find the unknown angles. In this method, the set of equations convert to polynomials equations. The resultant theory has been used to eliminate specific harmonics: fifth, seventh, eleventh, and thirteenth. When the number of conducting angles increase, the polynomial order increases. To solve this problem, the resultant theory has been used to find the initial guess using Newton's method for the fundamental frequency switching.

Another way to solve the same set of equations has been introduced in [40] using the Groebner bases and the symmetric polynomials. At the same time, all possible switching patterns and their possible switching angles can be found, which provides different choices for the multilevel selective harmonic elimination (SHE). Also, it provides a full study for different modulation indices through a different switching patterns.

3.5 Conclusion

In this chapter, the control of the multilevel inverter has been discussed and different control methodologies have been introduced and illustrated. These methodologies have been classified depending on switching frequencies. In this thesis, the selective harmonic elimination PWM has been selected as a modulation technique because of its advantages

over other techniques. Also, the π/3 method has been used to find the switching angles. All of this will be discussed in Chapter 4.

CHAPTER 4

THEORETICAL METHODOLOGY AND SIMULATION RESULTS

4.1 Introduction

Chapter 2 introduced a literature review for multilevel inverter (MI) topologies. The Cascade H-bridge (CHB) topology was selected to conduct this research because of the advantages it has over other topologies. Chapter 3 introduced a literature review for MI modulation techniques, and the virtual stage PWM was selected as a modulation technique for this research.

Chapter 4 will provide the theoretical methodology and the simulation results. In section 4.2, the virtual stage PWM will be discussed in more detail. The generated VSPWM output waveform is line-to-line voltage. Both five- and seven-level inverters will be constructed using the CHB topology. The generated output waveform is five and seven levels from a three-phase perspective and three and five levels from a single-phase perspective. In general, if a selected harmonic content is eliminated from the single-phase waveform, it will be eliminated from the three-phase waveform. In addition, the triplen harmonics will be equal to zero in the three-phase waveform.

The conducting angles for this modulation technique will be found using two different methods. The first method is to calculate the angles from a single-phase perspective, while the second method is to calculate the angles from a three-phase perspective. In Section 4.3, simulation results will be provided for different cases regarding

eliminated harmonics and the number of levels. Section 4.4 will provide the analysis of the results by presenting comparison charts for both methods at different modulation indices.

4.2 Theoretical Methodology

The number of the eliminated harmonics in the MI that uses fundamental frequency switching depends on the number of the switching angles to achieve the lower THD, and the number of the switching angles depends on the number of levels in the MI. In the MI, the number of levels depends on the number of DC sources. As the number of DC sources increases, the manufacturing process becomes more expensive and the applications become limited. On the other hand, a way to decrease the THD can be done using high switching control, but this will increase the switching losses. For the same hardware and without using a very high switching frequency, the virtual stage PWM (VSPWM) has been developed [35].

The VSPWM is a combination between two different modulation techniques: the fundamental frequency switching and the unipolar PWM technique. Figure 4.1 shows this combination.

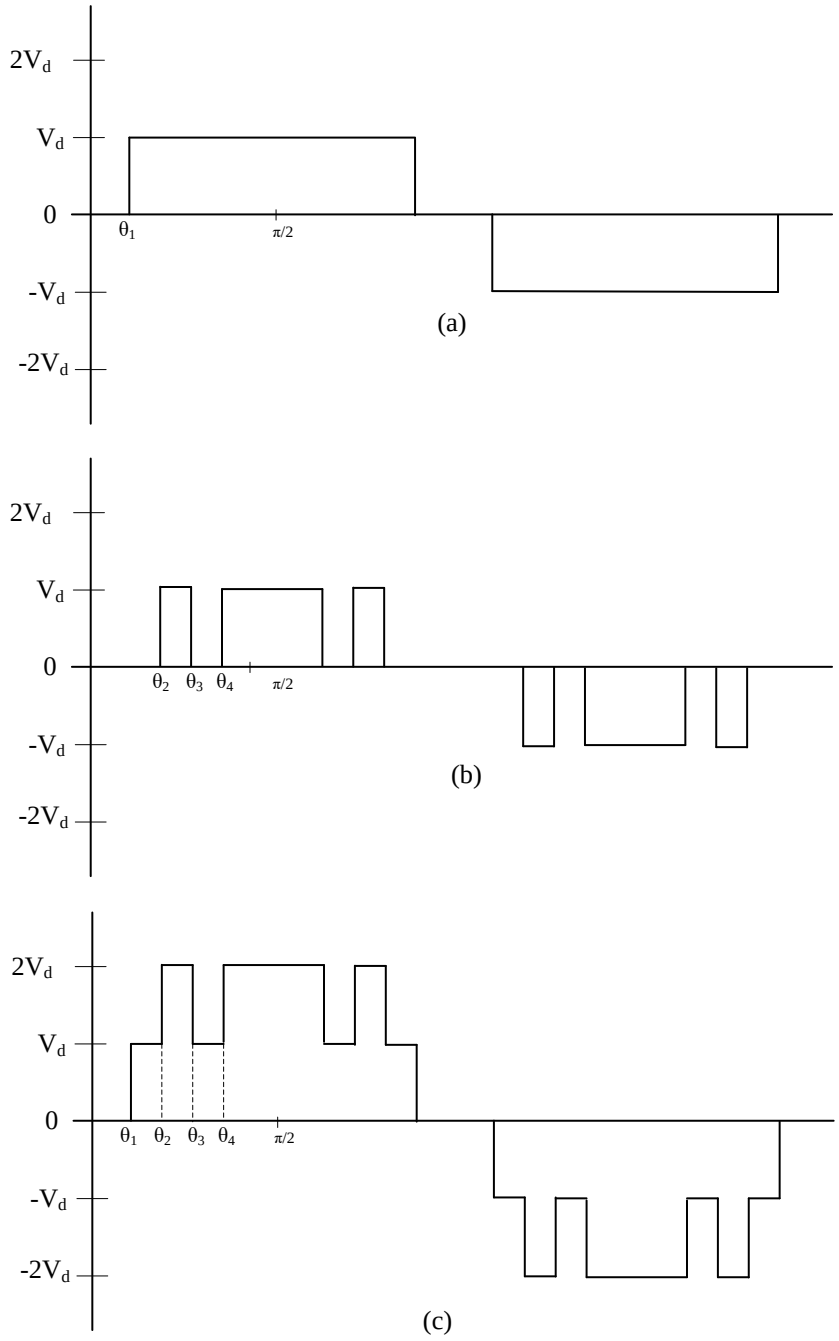

Figure 4.1: (a) Fundamental frequency switching output waveform; (b) unipolar switching output waveform; (c) VSPWM output waveform for a five-level inverter output voltage

4.2.1 Five-Level VSPWM Inverter

4.2.1.1 Using π/2 Method

In the following derivation, the fifth and seventh harmonics are eliminated from the single-phase perspective using equation (4.1). The three-phase output signal will contain the non-triplen harmonic contents greater than only the seventh because the fifth and seventh have been eliminated from the single-phase and will be eliminated from the three-phase waveform. In addition, the even harmonic contents will equal zero, as discussed in Chapter 3. The triplen harmonic contents will equal zero because the proposed system is dealing with a balanced three-phase system in which the line to neutral voltage contains multiple of three times the fundamental frequency and they are equal in magnitude and phase for the triplen harmonics contained in the other two line to neutral voltages. Thus, they will cancel each other and the balanced three-phase system will have zero triplen harmonic contents [41].

The generation of the line-to-line five-level VSPWM waveform has been done using single CHB for each phase, and each phase generates a unipolar switching output waveform with a 120˚ phase shift.

Figure 4.2 shows the unipolar generated single-phase waveform from single CHB. This waveform will be used to construct the set of equations to find the unknown switching angles.

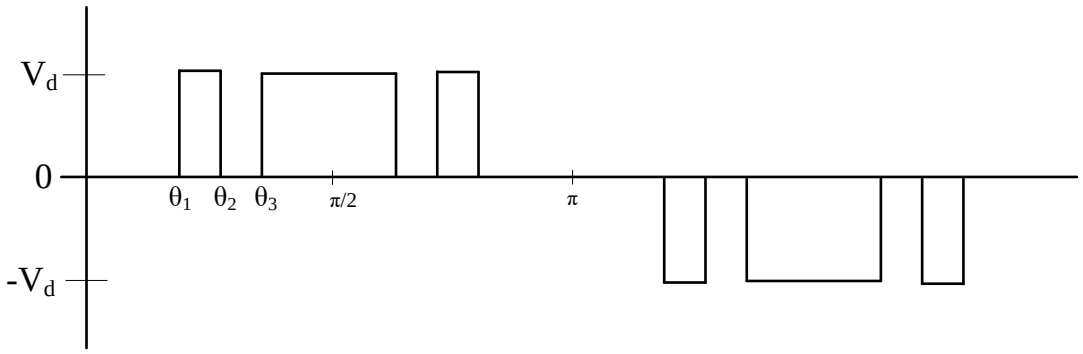

Figure 4.2: Unipolar switching output waveform from single-phase, single source CHB

$$b_n = \frac{4}{\pi}\int_0^{\pi/2} f\left(\frac{\omega t}{2\pi f_0}\right)\sin(n\omega t)d\omega \tag{4.1}$$

$$0 \le \theta_1 \le \theta_2 \le \theta_3 \le \frac{\pi}{2} \tag{4.2}$$

Where *n* is the harmonic order.

$$b_n = \int_0^{\theta_1} 0 \times \sin(n\omega t) + \int_{\theta_1}^{\theta_2} V_d \times \sin(n\omega t) + \int_{\theta_2}^{\theta_3} 0 \times \sin(n\omega t) + \int_{\theta_3}^{\frac{\pi}{2}} V_d \times \sin(n\omega t) \tag{4.3}$$

$$b_n = V_d \times \cos(n\theta_1) - V_d \times \cos(n\theta_2) + V_d \times \cos(n\theta_3) \tag{4.4}$$

To eliminate the fifth harmonic, equation (4.4) equals zero at n = 5:

$$V_d \times \cos(5\theta_1) - V_d \times \cos(5\theta_2) + V_d \times \cos(5\theta_3) = 0 \tag{4.5}$$

To eliminate the seventh harmonic, equation (4.4) equals zero at n = 7:

$$V_d \times \cos(7\theta_1) - V_d \times \cos(7\theta_2) + V_d \times \cos(7\theta_3) = 0 \quad (4.6)$$

If the inverter output sine wave fundamental frequency amplitude command is equal to V_1, equation (4.4) will equal V_1 at n = 1:

$$\frac{4}{\pi} V_d[\cos(\theta_1) - \times \cos(\theta_2) + \cos(\theta_3)] = V_1 \quad (4.7)$$

Then, the modulation index is equal to:

$$m_a = \frac{V_1}{\frac{4V_d}{\pi}} \quad (4.8)$$

For example, if the modulation index is considered equal to 0.8, the set of equations becomes:

$$\cos(5\theta_1) - \cos(5\theta_2) + \cos(5\theta_3) = 0 \quad (4.9)$$

$$\cos(7\theta_1) - \cos(7\theta_2) + \cos(7\theta_3) = 0 \quad (4.10)$$

$$\cos(\theta_1) - \cos(\theta_2) + \cos(\theta_3) = 0.8 \quad (4.11)$$

To solve the above set of equations, the MATLAB program has been used. The function fsolve in MATLAB uses Newton-Raphson's method to solve the non-linear equations. The three unknown angles will be the following:

$$\theta_1 = 23.6303^\circ = 0.41242\, rad$$

$$\theta_2 = 38.0607^\circ = 0.66428\, rad$$

$$\theta_3 = 47.8397^\circ = 0.83496\, rad$$

4.2.1.2 Using π/3 Method

In the following derivation, the fifth and seventh harmonics will be eliminated. In this method, the set of equations will be developed using the three-phase waveform. Figure 4.3 shows the VSPWM for a three-phase signal in the interval (0, π/3).

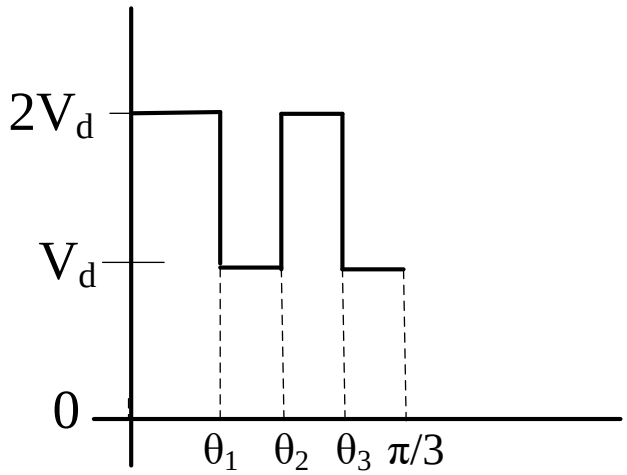

Figure 4.3: Five-level line-to-line output voltage waveform of the VSPWM technique in the interval (0, π/3)

To eliminate the fifth and seventh harmonic in the three-phase output waveform, equation (3.35) from Chapter 3 has been used to develop the set of equations needed to find the unknown switching angles.

$$a_n = \frac{8}{\pi}\cos\left(n\frac{\pi}{6}\right)\int_0^{\pi/3} v_{\varphi-\varphi}(\theta)\cos\left(n\left(\frac{\pi}{6}+\theta\right)\right)d\theta \tag{3.35}$$

$$0 \le \theta_1 \le \theta_2 \le \theta_3 \le \frac{\pi}{3} \tag{4.12}$$

For the fifth harmonic content, equation (3.35) will become the following:

$$a_n = \frac{8}{\pi}\cos\left(5\frac{\pi}{6}\right)\int_0^{\theta_1} 2V_d \cos\left(5\left(\frac{\pi}{6}+\theta\right)\right)d\theta + \frac{8}{\pi}\cos\left(5\frac{\pi}{6}\right)\int_{\theta_1}^{\theta_2} V_d \cos\left(5\left(\frac{\pi}{6}+\theta\right)\right)d\theta + \frac{8}{\pi}\cos\left(5\frac{\pi}{6}\right)\int_{\theta_2}^{\theta_3} 2V_d \cos\left(5\left(\frac{\pi}{6}+\theta\right)\right)d\theta + \frac{8}{\pi}\cos\left(5\frac{\pi}{6}\right)\int_{\theta_3}^{\pi/3} V_d \cos\left(5\left(\frac{\pi}{6}+\theta\right)\right)d\theta \quad (4.13)$$

For the seventh harmonic content, equation (3.35) will become the following:

$$a_n = \frac{8}{\pi}\cos\left(7\frac{\pi}{6}\right)\int_0^{\theta_1} 2V_d \cos\left(7\left(\frac{\pi}{6}+\theta\right)\right)d\theta + \frac{8}{\pi}\cos\left(7\frac{\pi}{6}\right)\int_{\theta_1}^{\theta_2} V_d \cos\left(7\left(\frac{\pi}{6}+\theta\right)\right)d\theta + \frac{8}{\pi}\cos\left(7\frac{\pi}{6}\right)\int_{\theta_2}^{\theta_3} 2V_d \cos\left(7\left(\frac{\pi}{6}+\theta\right)\right)d\theta + \frac{8}{\pi}\cos\left(7\frac{\pi}{6}\right)\int_{\theta_3}^{\pi/3} V_d \cos\left(7\left(\frac{\pi}{6}+\theta\right)\right)d\theta \quad (4.14)$$

For the fundamental frequency, equation (3.35) will become the following:

$$a_n = \frac{8}{\pi}\cos\left(\frac{\pi}{6}\right)\int_0^{\theta_1} 2V_d \cos\left(\left(\frac{\pi}{6}+\theta\right)\right)d\theta$$

$$+\frac{8}{\pi}\cos\left(\frac{\pi}{6}\right)\int_{\theta_1}^{\theta_2} V_d \cos\left(\left(\frac{\pi}{6}+\theta\right)\right)d\theta$$

$$+\frac{8}{\pi}\cos\left(\frac{\pi}{6}\right)\int_{\theta_2}^{\theta_3} 2V_d \cos\left(\left(\frac{\pi}{6}+\theta\right)\right)d\theta$$

$$+\frac{8}{\pi}\cos\left(\frac{\pi}{6}\right)\int_{\theta_3}^{\pi/3} V_d \cos\left(\left(\frac{\pi}{6}+\theta\right)\right)d\theta \qquad (4.15)$$

To eliminate the fifth and seventh harmonics, a_n will be equal to zero. After performing the integration, the set of equations will become as follows:

$$\frac{8}{\pi}\cos\left(\frac{5\pi}{6}\right)\times\left(\frac{\mathrm{V}_d}{5}\cos\left(5\theta_1+\frac{\pi}{3}\right)-\frac{\mathrm{V}_d}{5}\cos\left(5\theta_2+\frac{\pi}{3}\right)+\frac{\mathrm{V}_d}{5}\cos\left(5\theta_3+\frac{\pi}{3}\right)\right)=0 \qquad (4.16)$$

$$\frac{8}{\pi}\cos\left(\frac{\pi}{6}\right)\times\left(-\frac{\mathrm{V}_d}{7}\cos\left(7\theta_1-\frac{\pi}{3}\right)+\frac{\mathrm{V}_d}{7}\cos\left(7\theta_2-\frac{\pi}{3}\right)-\frac{\mathrm{V}_d}{7}\cos\left(7\theta_3-\frac{\pi}{3}\right)\right)=0 \qquad (4.17)$$

$$\frac{8}{\pi}\cos\left(\frac{\pi}{6}\right)\times\left(\mathrm{V}_d\cos\left(\theta_1-\frac{\pi}{3}\right)-\mathrm{V}_d\cos\left(\theta_2-\frac{\pi}{3}\right)+\mathrm{V}_d\cos\left(\theta_3-\frac{\pi}{3}\right)\right)=22 \qquad (4.18)$$

To solve the above set of equations, the MATLAB program has been used. The function fsolve in MATLAB uses Newton-Raphson's method to solve the non-linear equations. The three unknown angles will be the following:

$$\theta_1 = 13.8648^{\circ} = 0.24198\,rad$$

$$\theta_2 = 22.3263^{\circ} = 0.38966\,rad$$

$$\theta_3 = 37.8334^{\circ} = 0.660317\,rad$$

4.2.2 Seven-Level VSPWM Inverter

4.2.2.1 Using π/2 Method

In the following derivation, the fifth, seventh, and eleventh harmonics will be eliminated from a single-phase perspective using equation (4.1). The three-phase output signal will contain the non-triplen harmonic contents greater than only the eleventh because of reasons previously mentioned in this section. The generation of the line-to-line seven-level VSPWM waveform has been done using two CHB for each phase, and each phase generates a five-level VSPWM waveform with a 120˚ phase shift.

Figure 4.4 shows the five-level VSPWM single-phase waveform, which will be used to construct the set of equations to find the unknown switching angles.

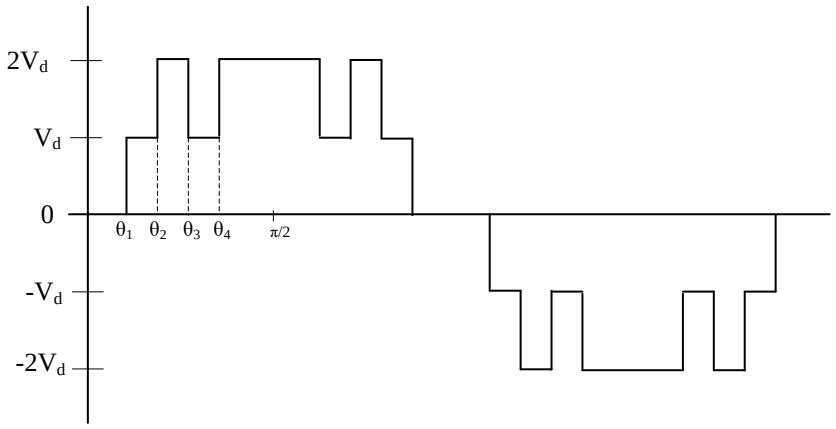

Figure 4.4: Five-level single-phase output voltage waveform of the VSPWM technique

$$b_n = \int_0^{\theta_1} 0 \times \sin(n\omega t) + \int_{\theta_1}^{\theta_2} V_d \times \sin(n\omega t) + \int_{\theta_2}^{\theta_3} 2 \times V_d \times \sin(n\omega t)$$

$$+ \int_{\theta_3}^{\theta_4} V_d \times \sin(n\omega t) + \int_{\theta_4}^{\pi/2} 2 \times V_d \times \sin(n\omega t) \qquad (4.19)$$

In the seven-level inverter, the eliminated harmonic contents will be fifth, seventh, and eleventh. The modulation index, for example, will be 1.34. After some manipulation, the set of equations becomes as follows:

$$\cos(\theta_1) + \cos(\theta_2) - \cos(\theta_3) + \cos(\theta_4) = 1.34 \quad (4.20)$$

$$\cos(5\theta_1) + \cos(5\theta_2) - \cos(5\theta_3) + \cos(5\theta_4) = 0 \quad (4.20)$$

$$\cos(7\theta_1) + \cos(7\theta_2) - \cos(7\theta_3) + \cos(7\theta_4) = 0 \quad (4.22)$$

$$\cos(11\theta_1) + \cos(11\theta_2) - \cos(11\theta_3) + \cos(11\theta_4) = 0 \quad (4.23)$$

To solve the above set of equations, the MATLAB program has been used. The function fsolve in MATLAB uses Newton-Raphson's method to solve the non-linear equations. The four unknown angles will be as follows:

$$\theta_1 = 20.3604^{\circ} = 0.35535\, rad$$

$$\theta_2 = 60.6732^{\circ} = 1.05894\, rad$$

$$\theta_3 = 79.9236^{\circ} = 1.39492\, rad$$

$$\theta_4 = 84.9717^{\circ} = 1.48303\, rad$$

4.2.2.2 Using π/3 Method

In the following derivation, the fifth, seventh, and eleventh harmonics will be eliminated. In this method, the set of equations will be developed using the three-phase waveform. Figure 4.5 shows the seven-level VSPWM for a three-phase signal in the interval (0, π/3).

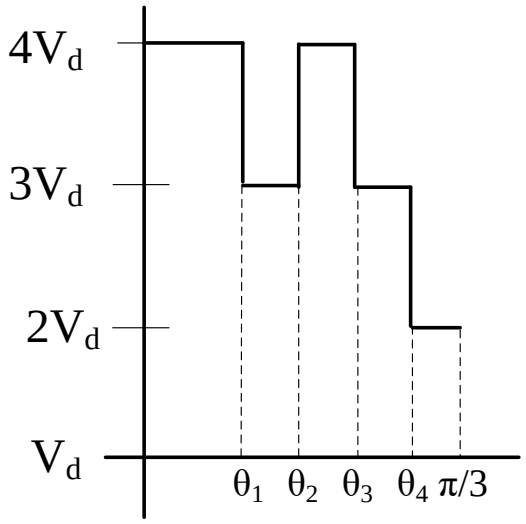

Figure 4.5: Three-phase output voltage waveform of the VSPWM technique for the interval [0, π/3]

To eliminate the fifth, seventh, and eleventh harmonic contents in the three-phase output waveform, equation (3.35) from Chapter 3 has been used to develop the set of equations needed to find the unknown switching angles. After some manipulation, the set of equations becomes as follows:

$$\frac{8}{\pi}\cos\left(\frac{5\pi}{6}\right)\times\left(\frac{\mathrm{V}_d}{5}\cos\left(5\theta_1+\frac{\pi}{3}\right)-\frac{\mathrm{V}_d}{5}\cos\left(5\theta_2+\frac{\pi}{3}\right)+\frac{\mathrm{V}_d}{5}\cos\left(5\theta_3+\frac{\pi}{3}\right)+\frac{\mathrm{V}_d}{5}\cos\left(5\theta_4+\frac{\pi}{3}\right)\right)=0 \quad (4.24)$$

$$\frac{8}{\pi}\cos\left(\frac{7\pi}{6}\right)\times\left(-\frac{\mathrm{V}_d}{7}\cos\left(7\theta_1-\frac{\pi}{3}\right)+\frac{\mathrm{V}_d}{7}\cos\left(7\theta_2-\frac{\pi}{3}\right)-\frac{\mathrm{V}_d}{7}\cos\left(7\theta_3-\frac{\pi}{3}\right)-\frac{\mathrm{V}_d}{7}\cos\left(7\theta_4-\frac{\pi}{3}\right)\right)=0 \quad (4.25)$$

$$\frac{8}{\pi}\cos\left(\frac{11\pi}{6}\right)\times\left(-\frac{\mathrm{V}_d}{11}\cos\left(11\theta_1+\frac{\pi}{3}\right)+\frac{\mathrm{V}_d}{11}\cos\left(11\theta_2+\frac{\pi}{3}\right)-\frac{\mathrm{V}_d}{11}\cos\left(11\theta_3+\frac{\pi}{3}\right)\right.$$

$$\left.-\frac{\mathrm{V}_d}{11}\cos\left(11\theta_4+\frac{\pi}{3}\right)\right)=0 \qquad (4.26)$$

$$\frac{8}{\pi}\cos\left(\frac{\pi}{6}\right)\times\left(\mathrm{V}_d\cos\left(\theta_1-\frac{\pi}{3}\right)-\mathrm{V}_d\cos\left(\theta_2-\frac{\pi}{3}\right)+\mathrm{V}_d\cos\left(\theta_3-\frac{\pi}{3}\right)+\mathrm{V}_d\cos\left(\theta_4-\frac{\pi}{3}\right)\right)$$

$$=35.82 \qquad (4.27)$$

To solve the above set of equations, the MATLAB program has been used. The function fsolve in MATLAB uses Newton-Raphson's method to solve the non-linear equations. The four unknown angles will be as follows:

$$\theta_1 = 0.3712^{\circ} = 0.00647\ rad$$

$$\theta_2 = 20.5045^{\circ} = 0.35787\ rad$$

$$\theta_3 = 25.4500^{\circ} = 0.44418 rad$$

$$\theta_4 = 35.0481^{\circ} = 0.61170\ rad$$

4.3 Simulation Model and Results

To compare the results of using the π/2 method and the π/3 method for both the five- and seven-level inverters, MATLAB Simulink was used to construct the three-phase CHB multilevel inverter. Each CHB is connected with a 12V DC source. Each IGBT will be injected by a control signal using a pulse generator.

4.3.1 Simulation Results for Five-Level Inverter

In this section, the simulation results for the three-phase five-level inverter will be provided, where the three switching angles have been found using both the π/2 method and

the π/3 method to eliminate the fifth and seventh harmonic contents. Figure 4.6 shows the constructed three-phase five-level CHB in MATLAB.

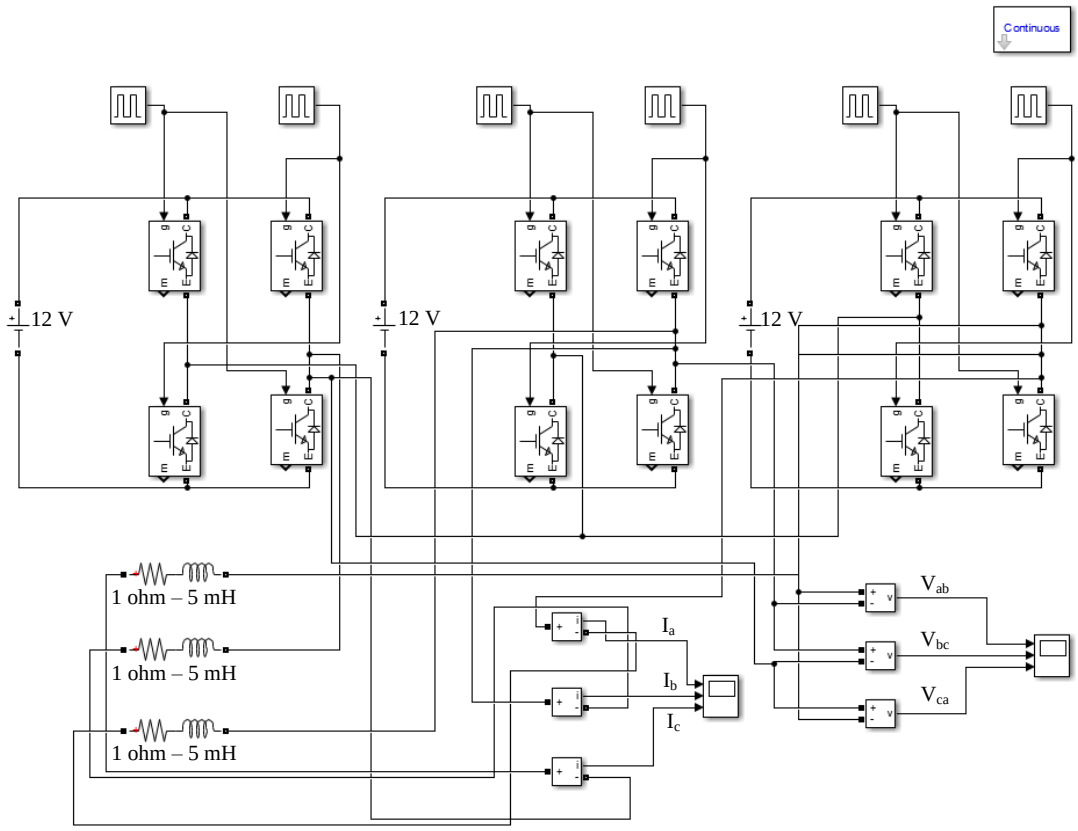

Figure 4.6: MATLAB model for three-phase five-level CHB

4.3.1.1 Simulation Results for Five-Level Inverter Using π/2 Method

In this simulation, the unknown angles that have been found by the π/2 method in sub section 4.2.1.1 have been used to generate the control signal by the pulse generator. These signals were directly injected in the IGBT to control the output voltage waveform. Figures 4.7 and 4.8 show the output voltage for the single- and three-phase, respectively.

Figures 4.9 and 4.10 show the harmonic content spectrum for the single-phase voltage and the three-phase voltage, respectively. A balanced three-phase delta connected load (1 Ohm, 5 mH) has been connected to the constructed inverter. Figures 4.11 and 4.12 present the phase current waveform and harmonic contents, respectively.

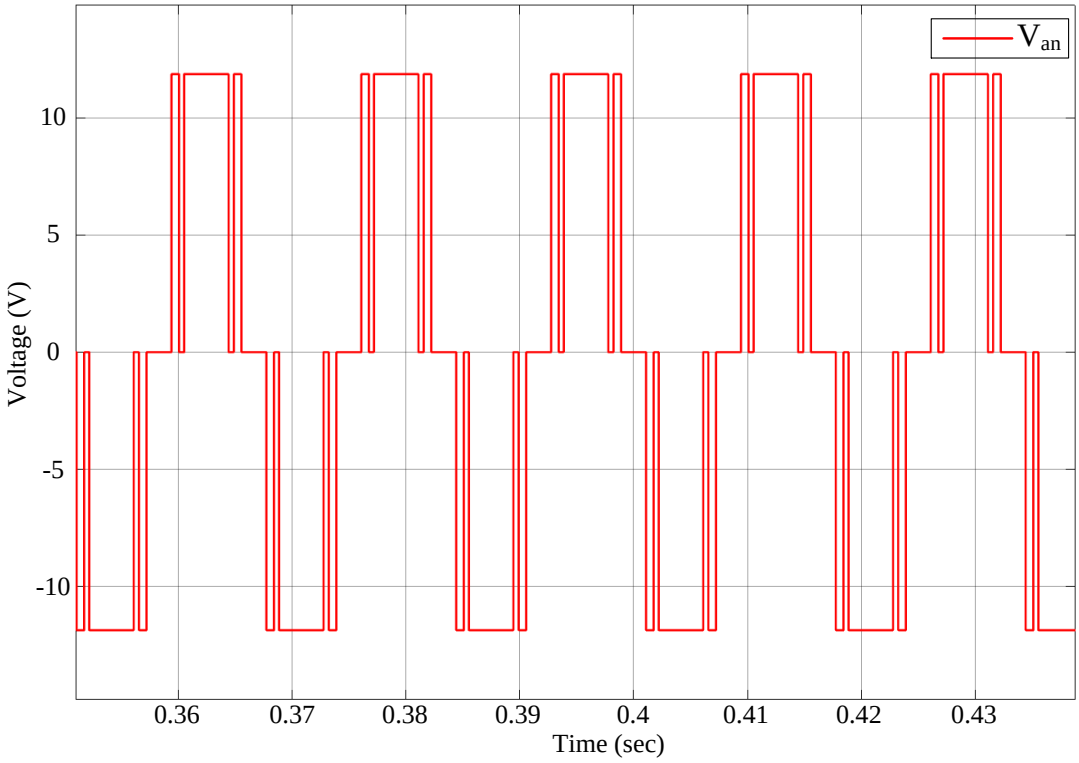

Figure 4.7: Single-phase output voltage waveform using π/2 method

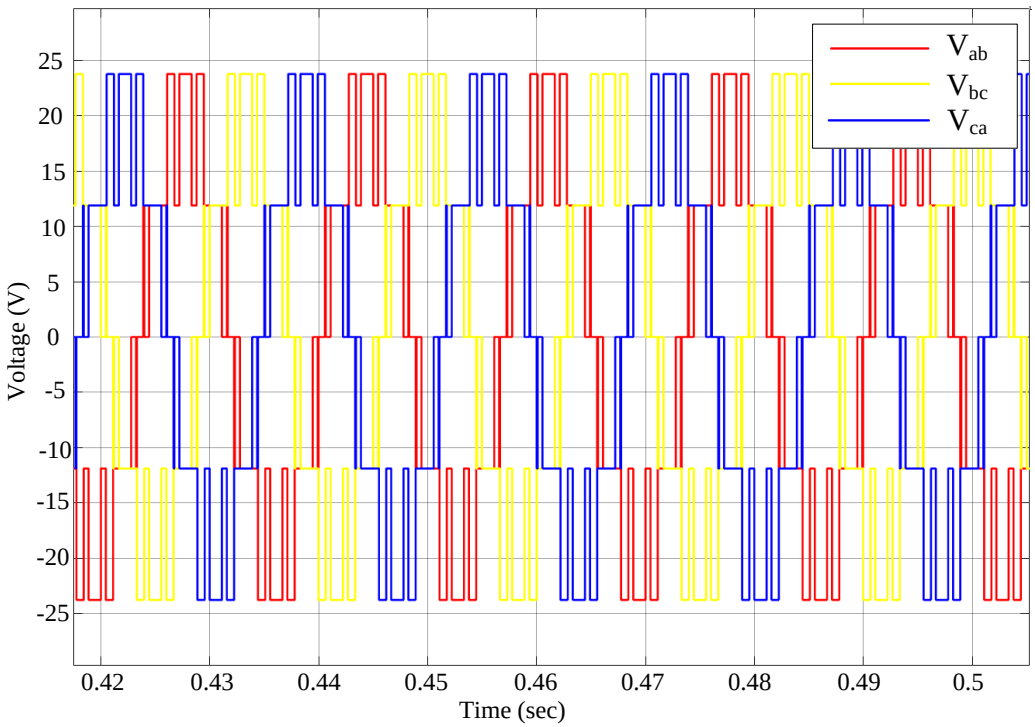

Figure 4.8: Three-phase output voltage waveform using π/2 method

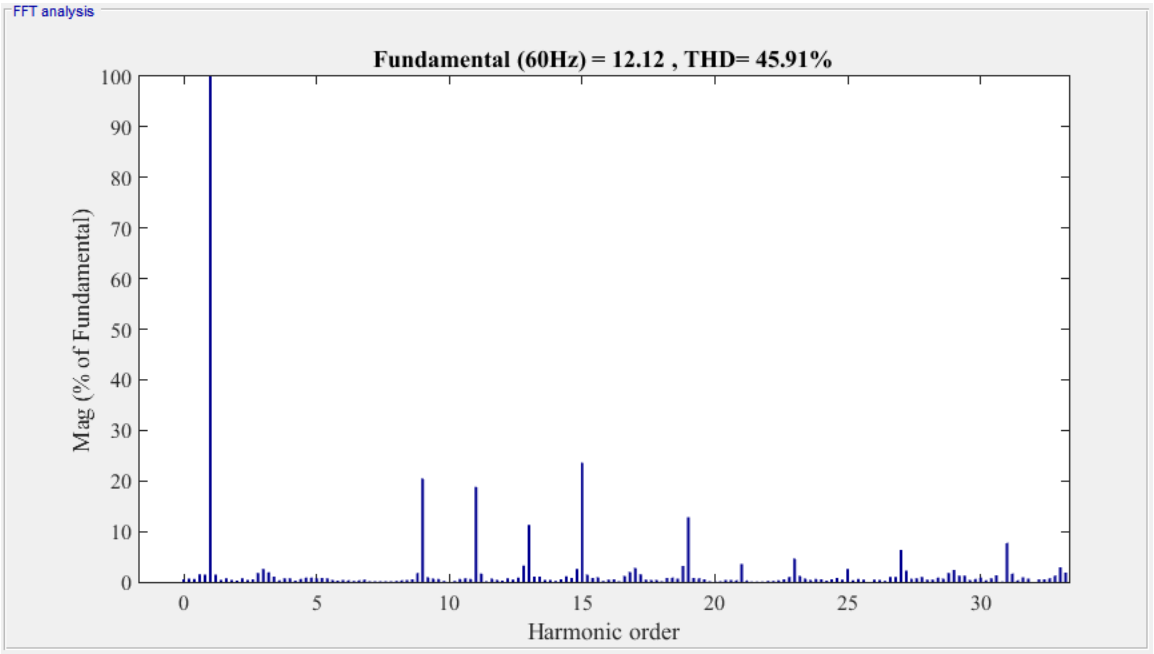

Figure 4.9: Single-phase output voltage harmonic contents using π/2 method

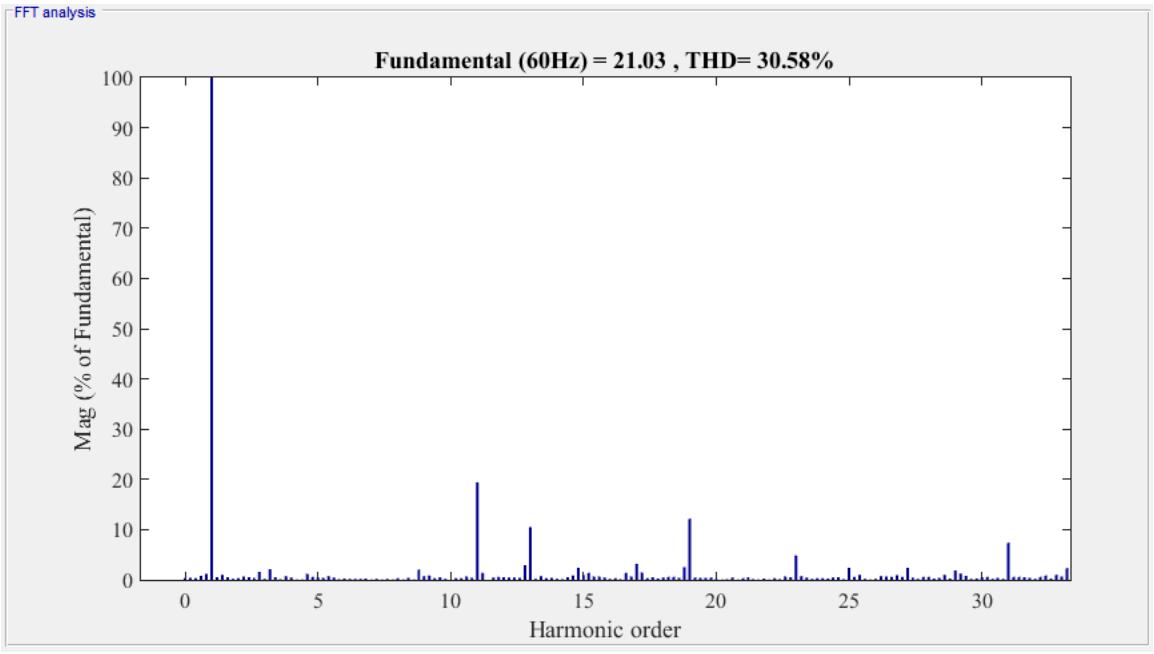

Figure 4.10: Three-phase output voltage harmonic contents using π/2 method

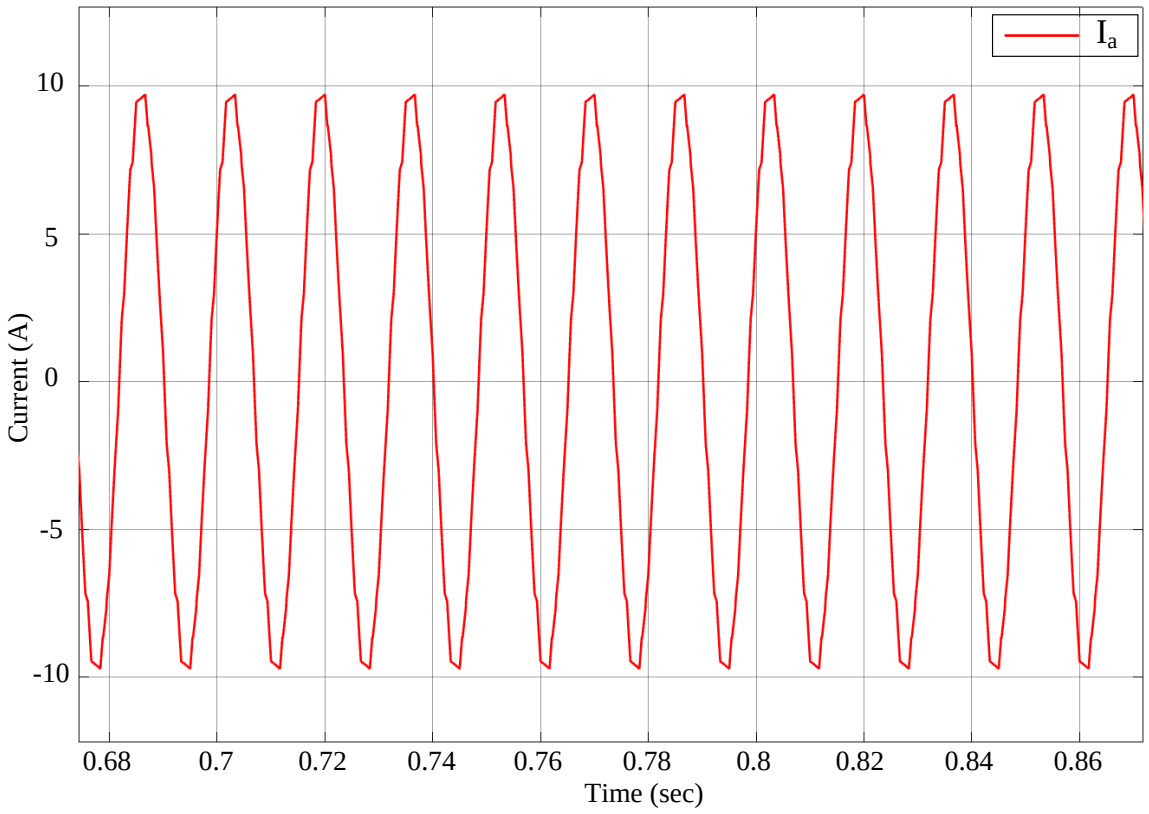

Figure 4.11: Phase current waveform using π/2 method

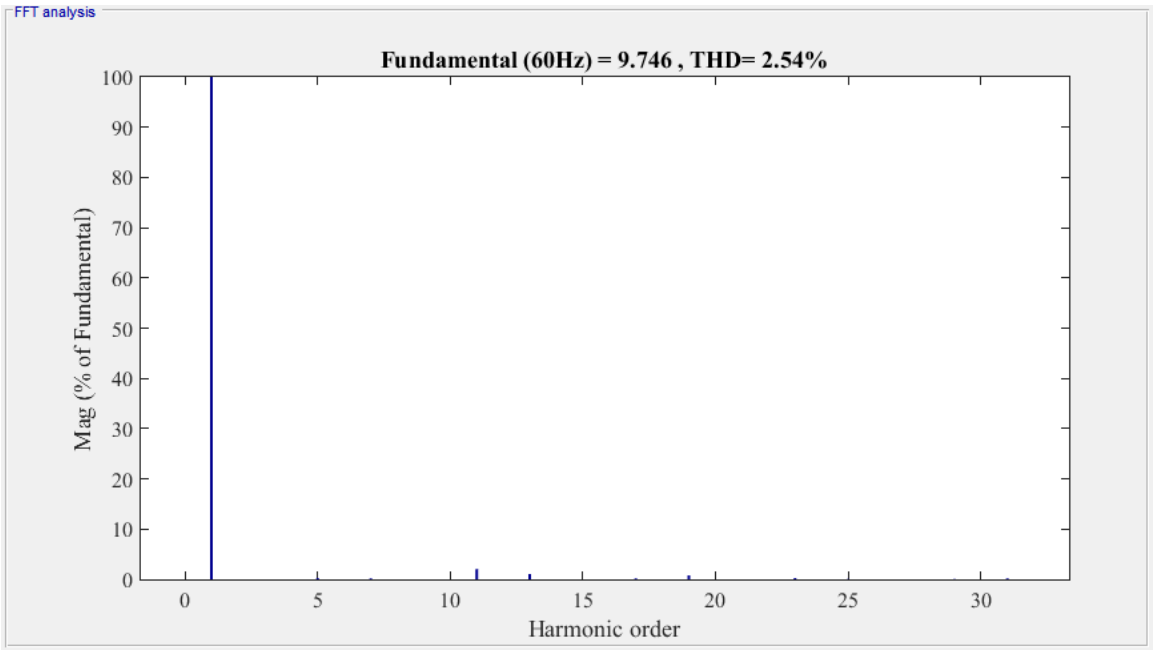

Figure 4.12: Phase current harmonic contents using π/2 method

4.3.1.2 Simulation Results for π/3 Method

In this simulation, the three switching angles that have been found by the π/3 method in sub section 4.2.1.2 have been used to generate the control signal by the pulse generator. These signals were directly injected in the IGBT to control the output voltage waveform. Figures 4.13 and 4.14 show the output voltage for the single- and three-phase, respectively. Figures 4.15 and 4.16 show the harmonic content spectrum for the single-phase voltage and the three-phase voltage, respectively. A balanced three-phase delta connected load (1 Ohm, 5 mH) has been connected to the constructed inverter. Figures 4.17 and 4.18 present the phase current waveform and harmonic contents, respectively.

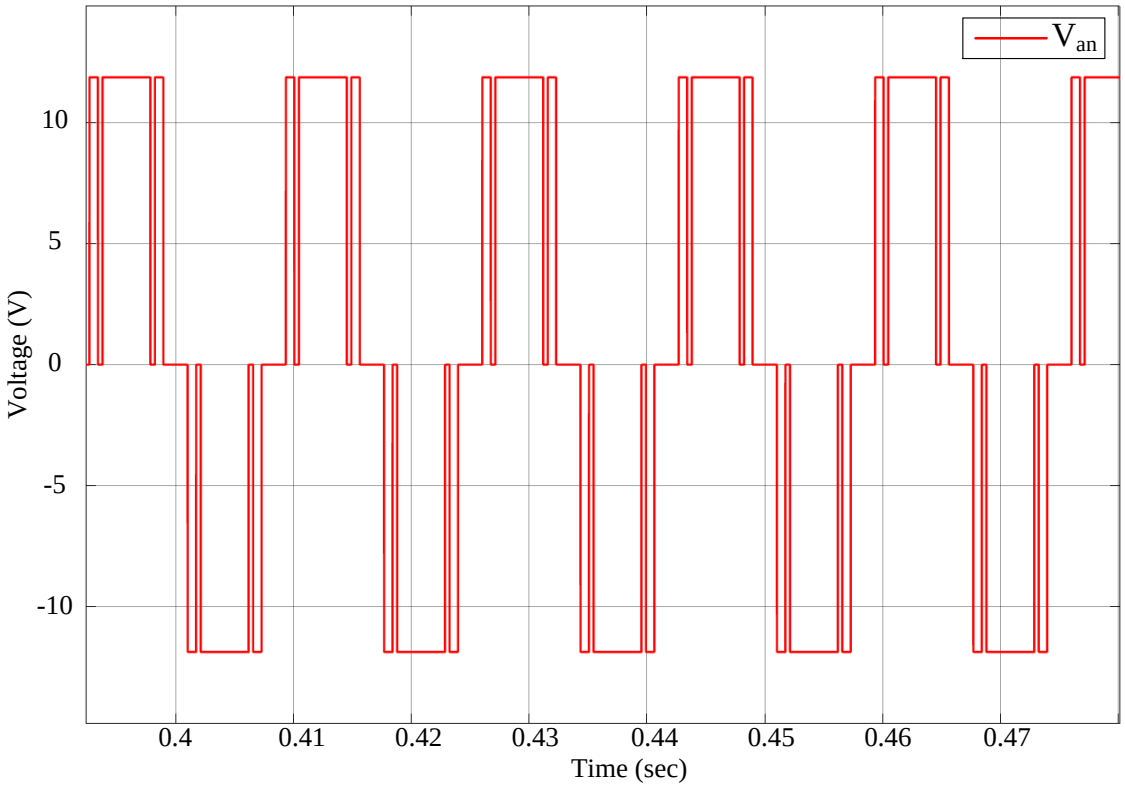

Figure 4.13: Single-phase output voltage waveform using π/3 method

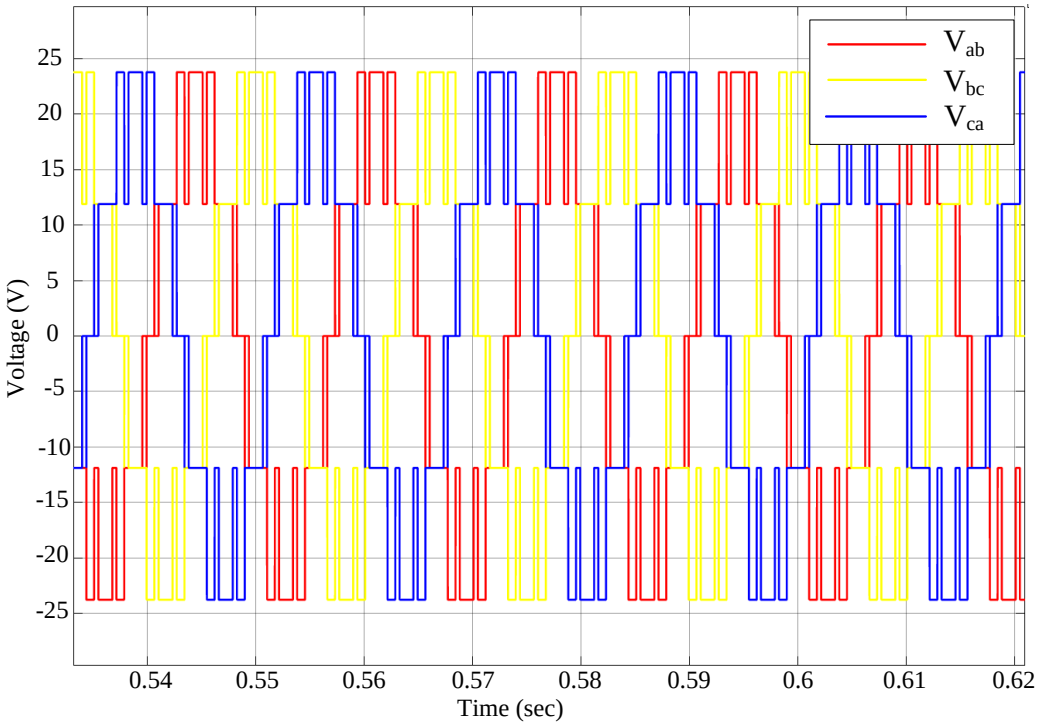

Figure 4.14: Three-phase output voltage waveform using π/3 method

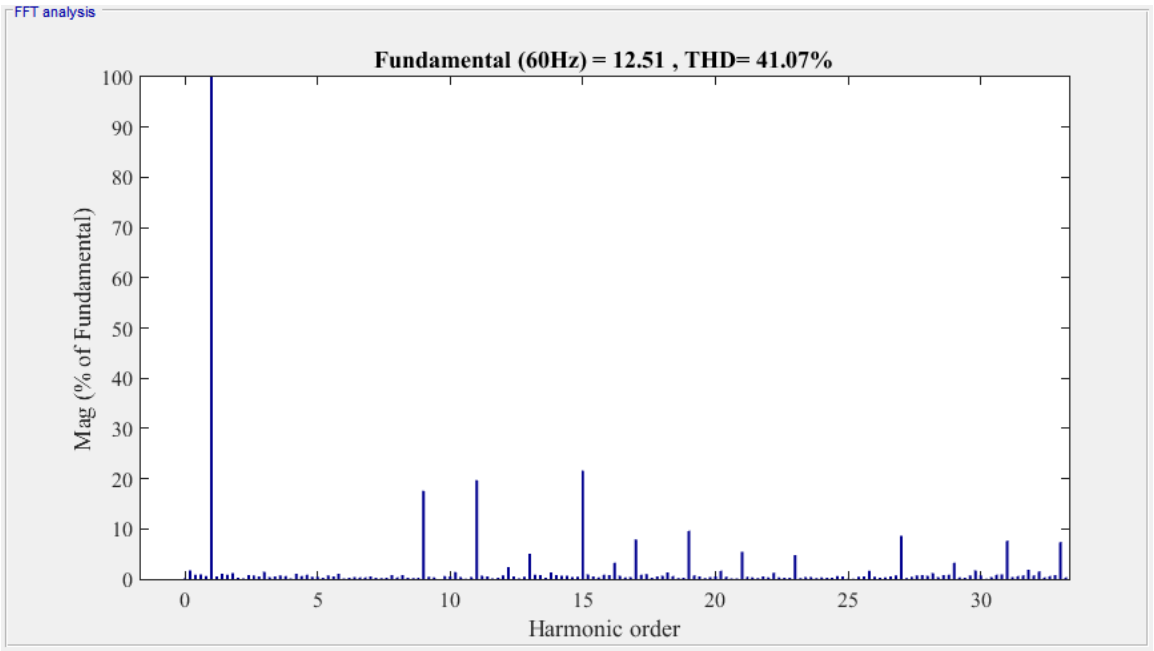

Figure 4.15: Single-phase output voltage harmonic contents using π/3 method

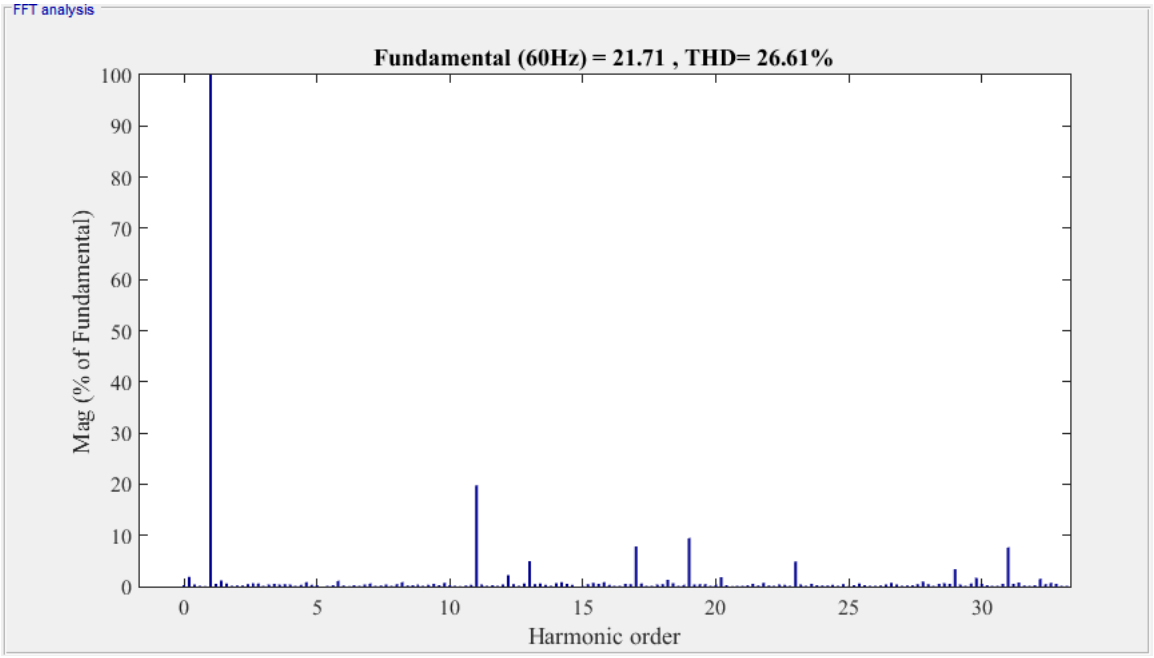

Figure 4.16: Three-phase output voltage harmonic contents using π/3 method

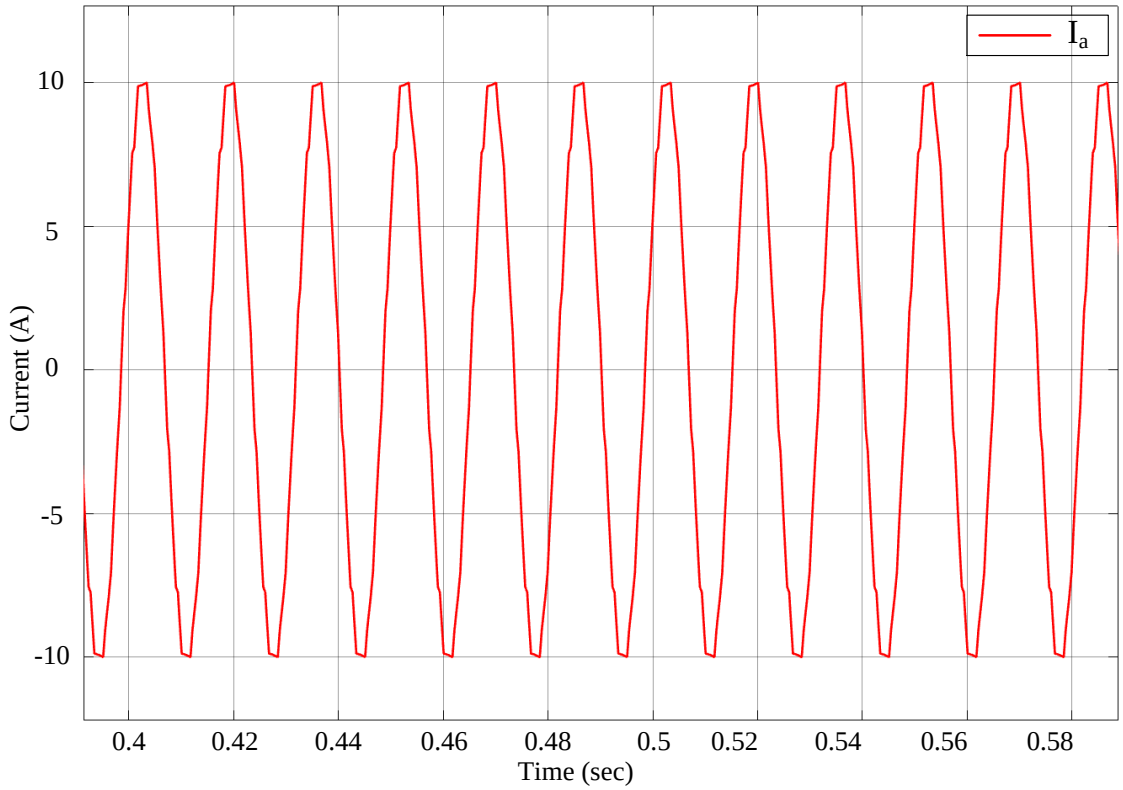

Figure 4.17: Phase current waveform using π/3 method

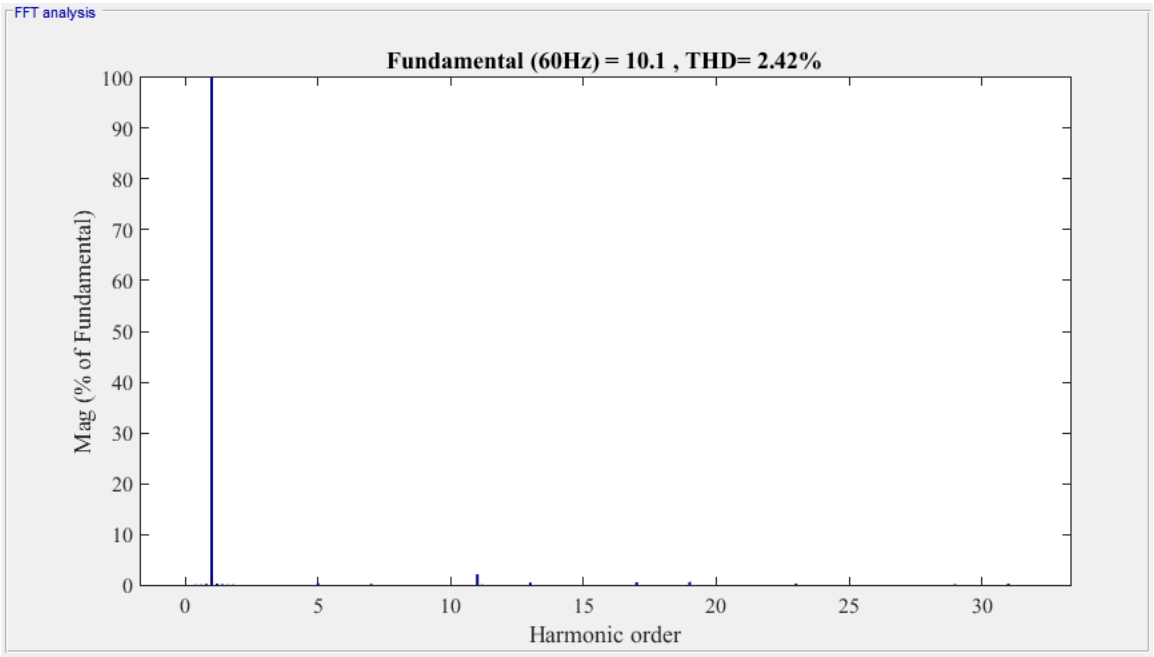

Figure 4.18: Phase current harmonic contents using π/3 method

4.3.2 Simulation Results for Seven-Level Inverter

In this section, the simulation results for the three-phase seven-level inverter will be provided, where the four switching angles have been found using both the π/2 method and the π/3 method to eliminate the fifth, seventh and eleventh harmonic contents. Figure 4.19 shows the constructed three-phase seven-level CHB in MATLAB.

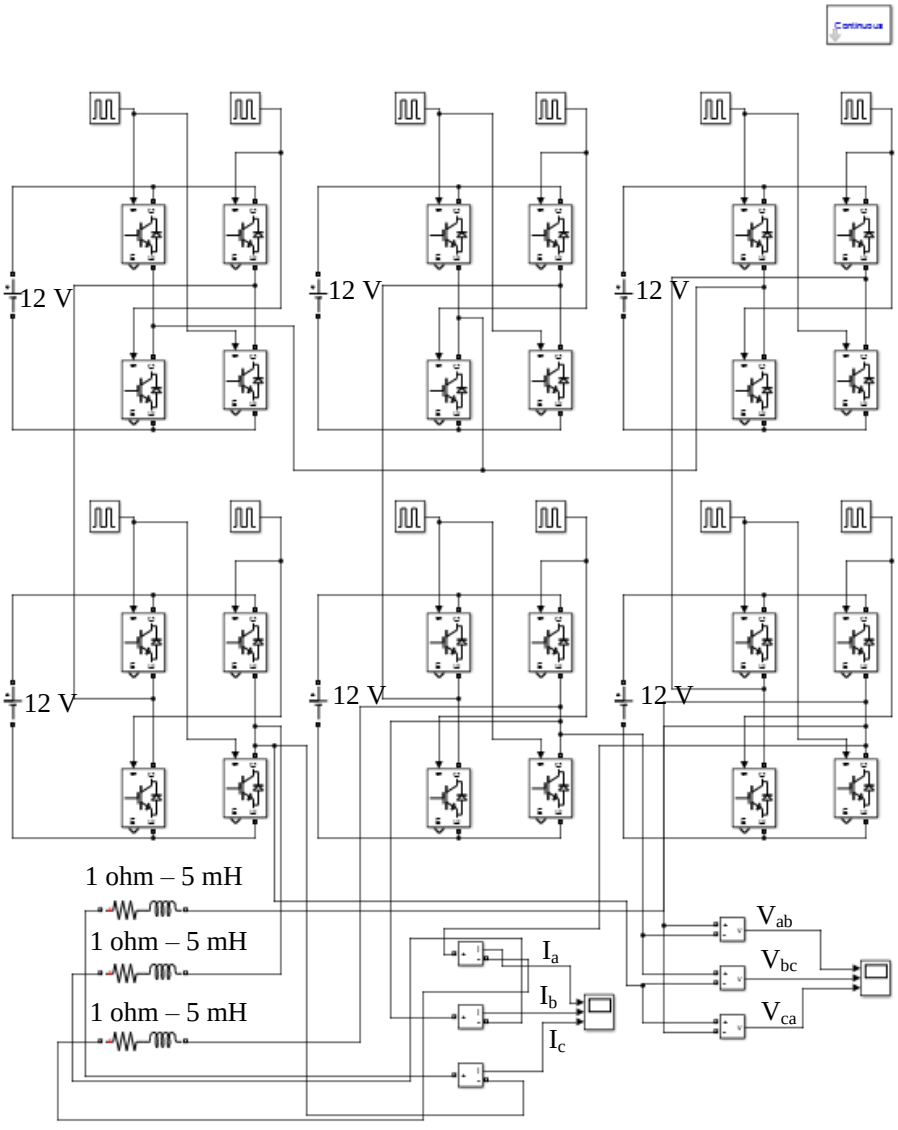

Figure 4.19: MATLAB model for three-phase seven-level CHB

4.3.2.1 Simulation Results for Seven-Level Inverter Using π/2 Method

In this simulation, the four switching angles that have been found by the π/2 method in sub section 4.2.2.1 have been used to generate the control signal by the pulse generator. These signals were directly injected in the IGBT to control the output voltage waveform. Figures 4.20 and 4.21 show the output voltage for the single- and three-phase, respectively. Figures 4.22 and 4.23 show the harmonic content spectrum for the single-phase voltage and the three-phase voltage, respectively. A balanced three-phase delta connected load (1 Ohm, 5 mH) has been connected to the constructed inverter. Figures 4.24 and 4.25 present the phase current waveform and harmonic contents, respectively.

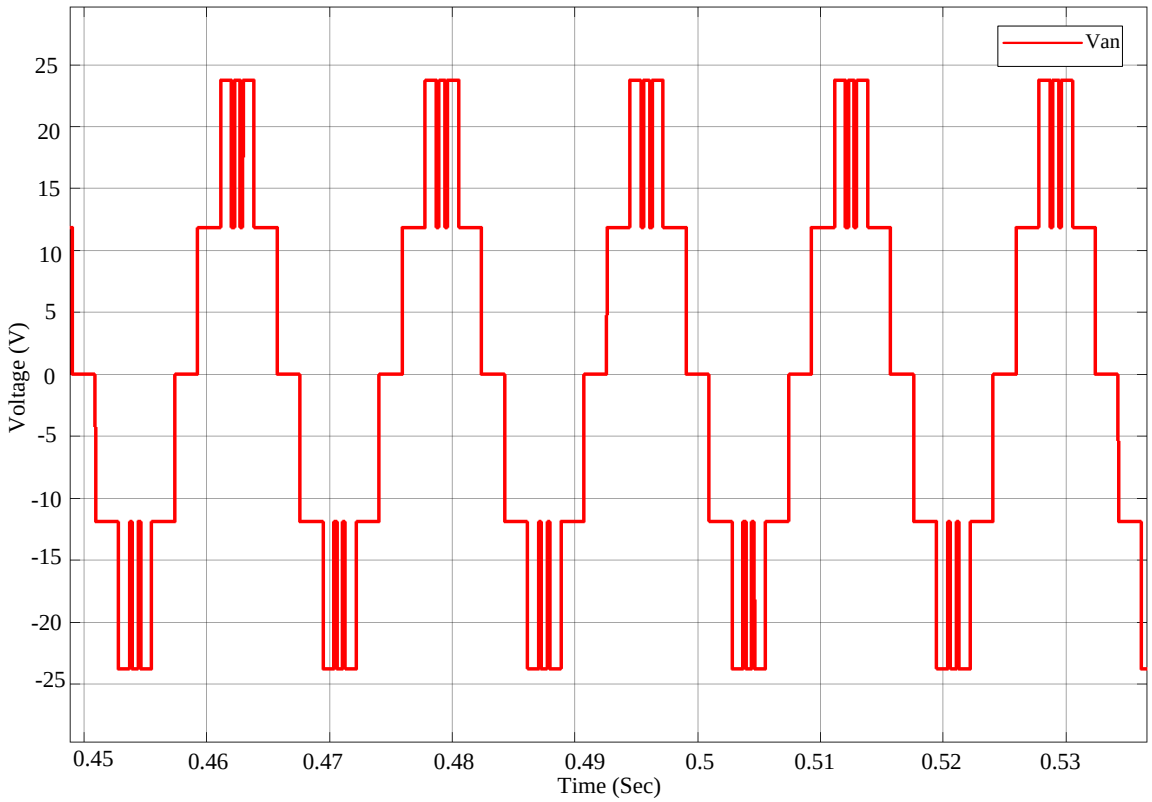

Figure 4.20: Single-phase output voltage waveform using π/2 method

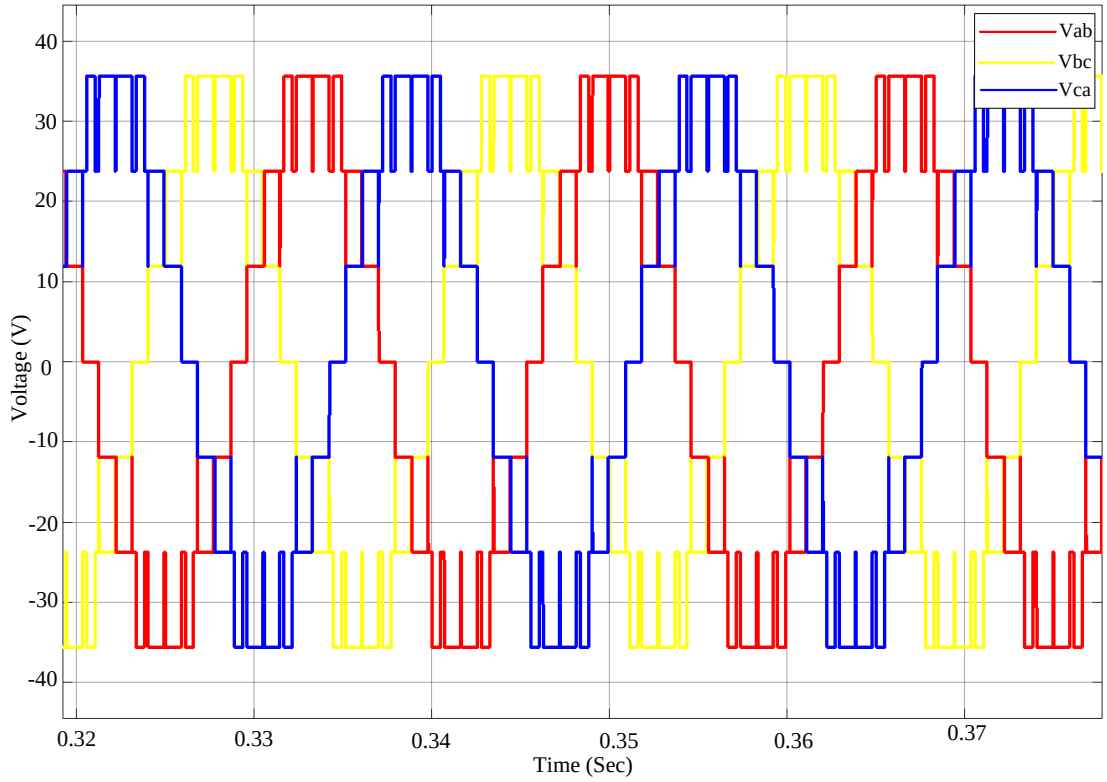

Figure 4.21: Three-phase output voltage waveform using π/2 method

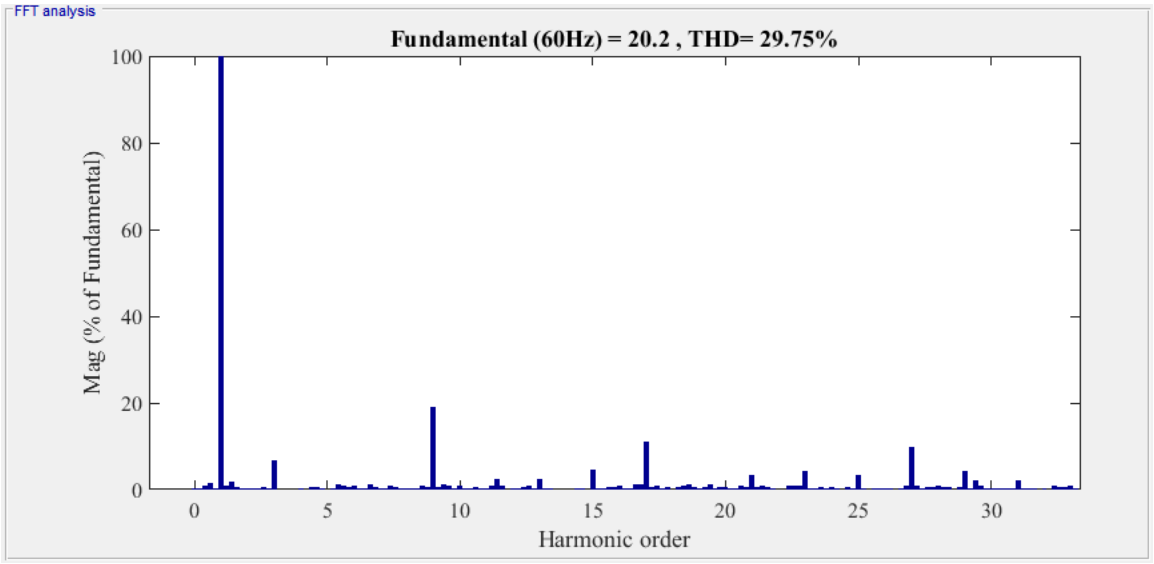

Figure 4.22: Single-phase output voltage harmonic contents using π/2 method

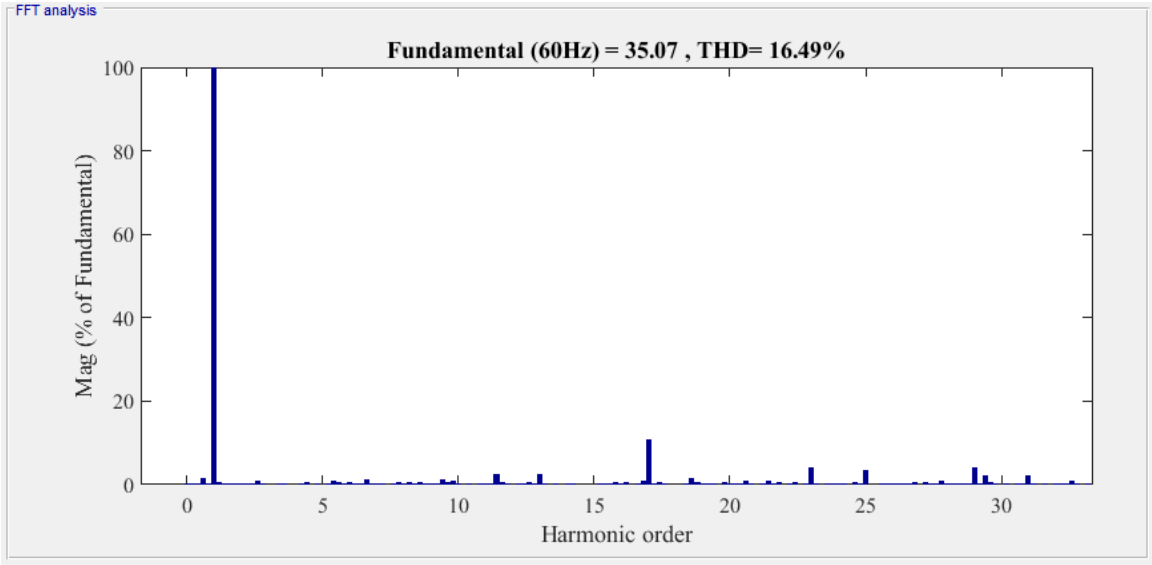

Figure 4.23: Three-phase output voltage harmonic contents using π/2 method

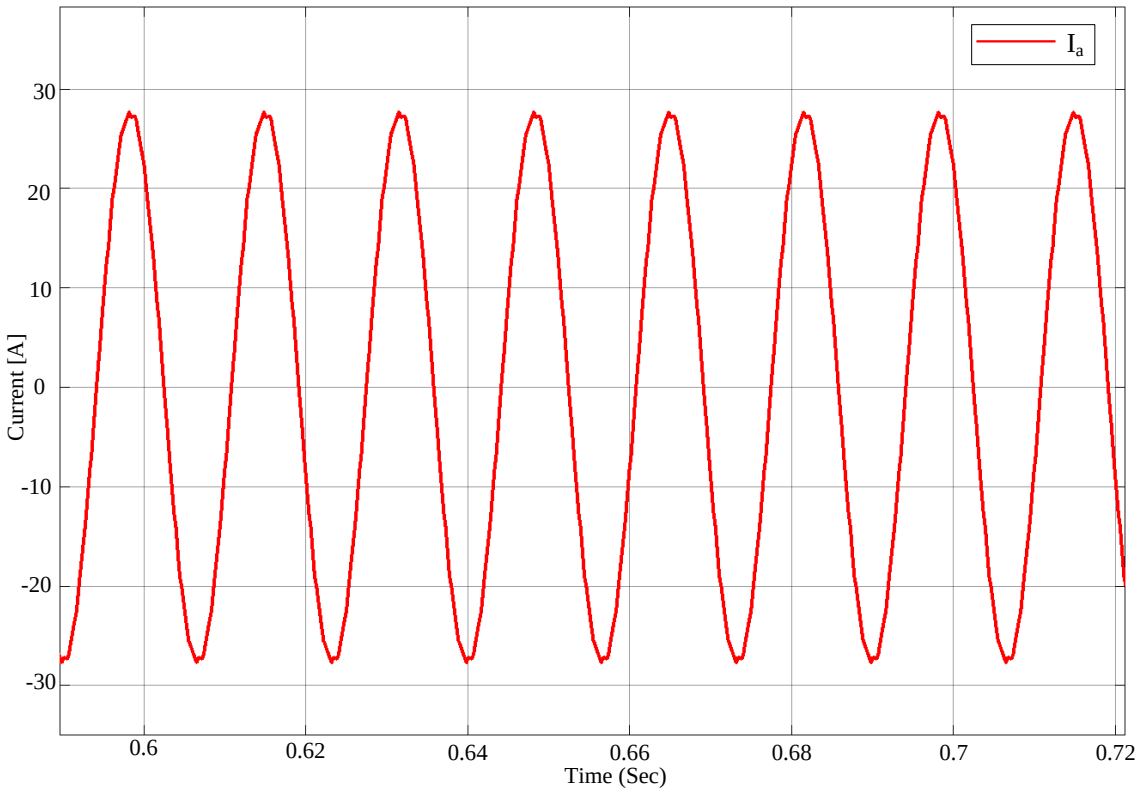

Figure 4.24: Phase current waveform using π/2 method

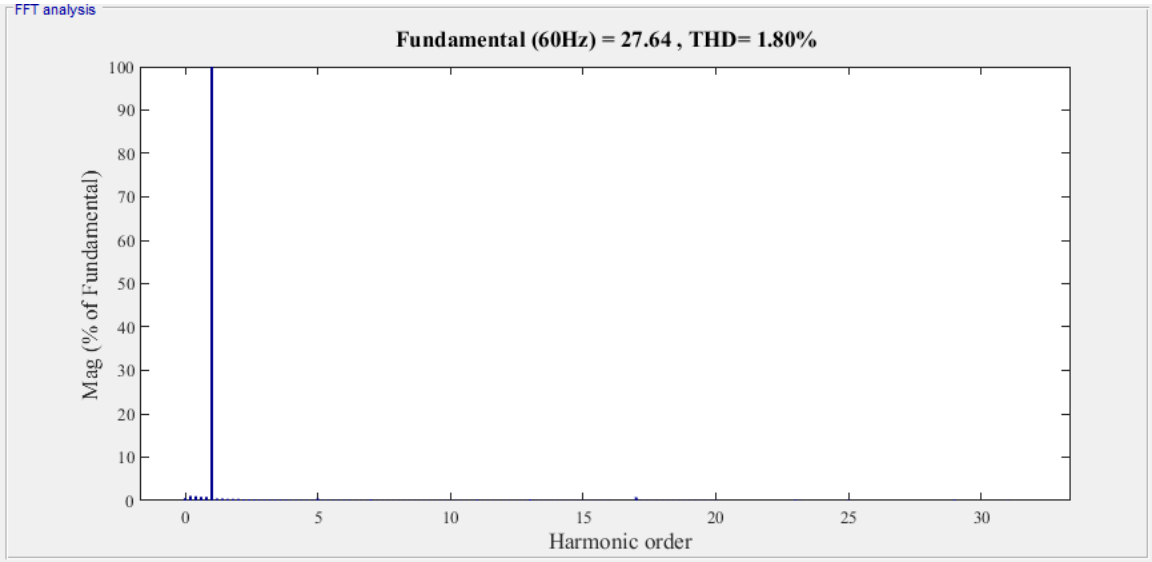

Figure 4.25: Phase current harmonic contents using π/2 method

4.3.2.2 Simulation Results for Seven-Level Inverter Using π/3 Method

In this simulation, the four switching angles that have been found by the π/3 method in sub section 4.2.2.2 have been used to generate the control signal by the pulse generator. These signals were directly injected in the IGBT to control the output voltage waveform. Figures 4.26 and 4.27 show the output voltage for the single- and three-phase, respectively. Figures 4.28 and 4.29 show the harmonic content spectrum for the single-phase voltage and the three-phase voltage, respectively. A balanced three-phase delta connected load (1 Ohm, 5 mH) has been connected to the constructed inverter. Figures 4.30 and 4.31 present the phase current waveform and harmonic contents, respectively.

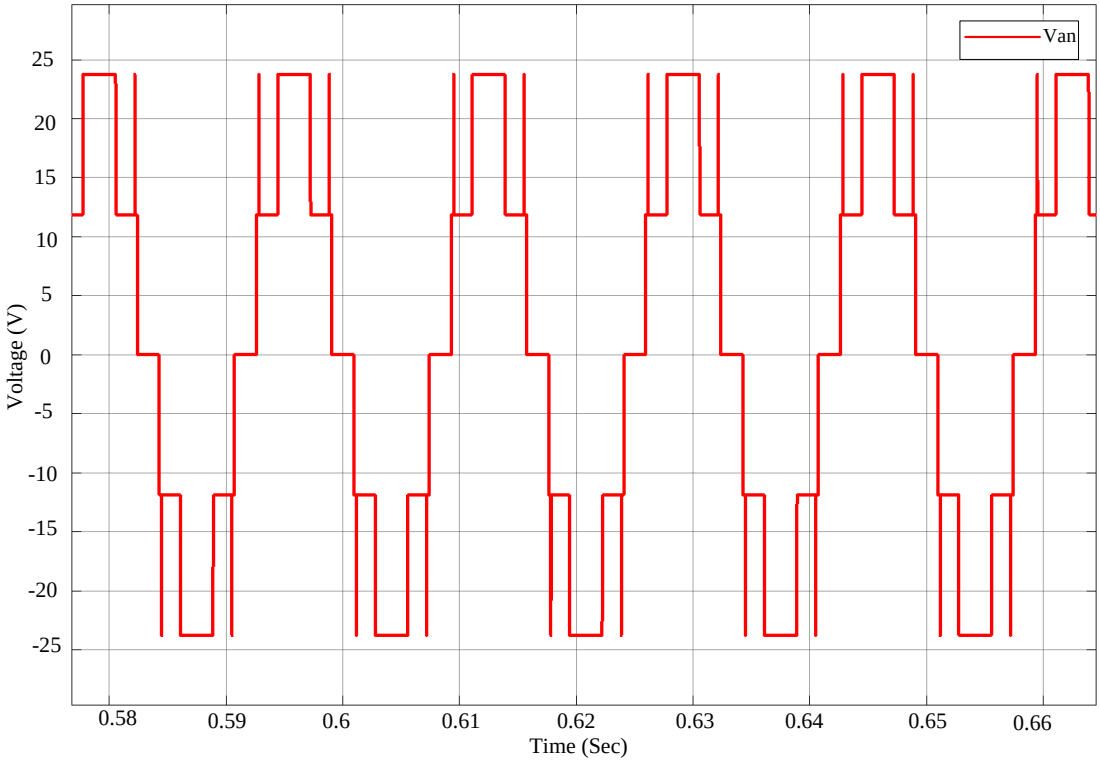

Figure 4.26: Single-phase output voltage waveform using π/3 method

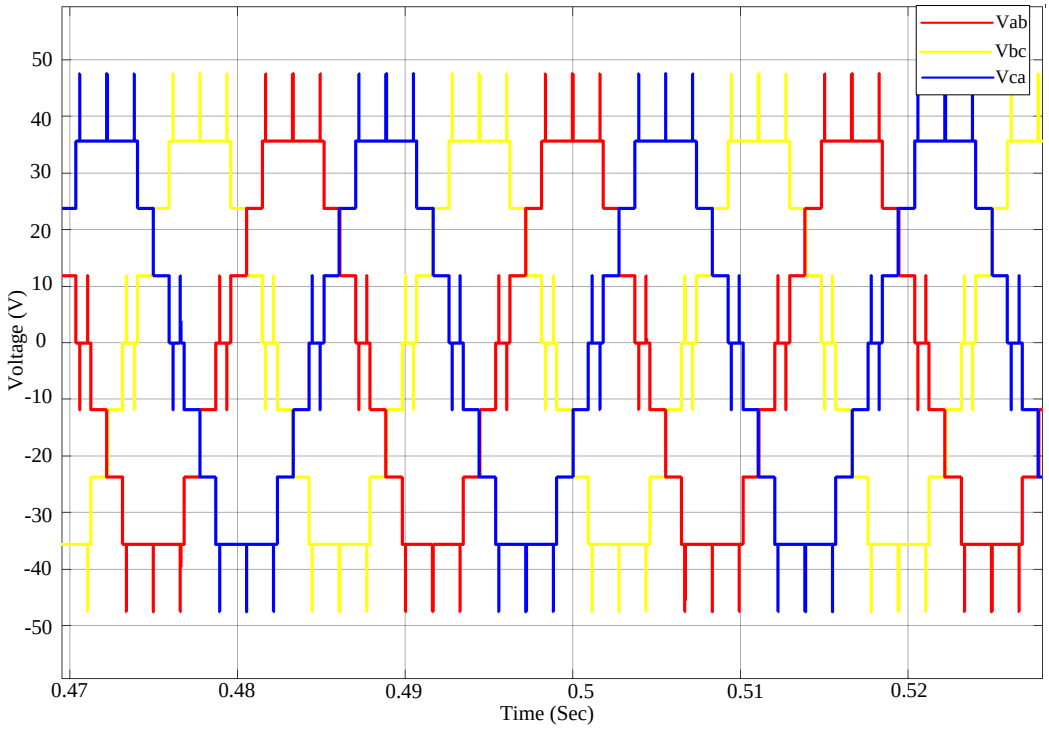

Figure 4.27: Three-phase output voltage waveform using π/3 method

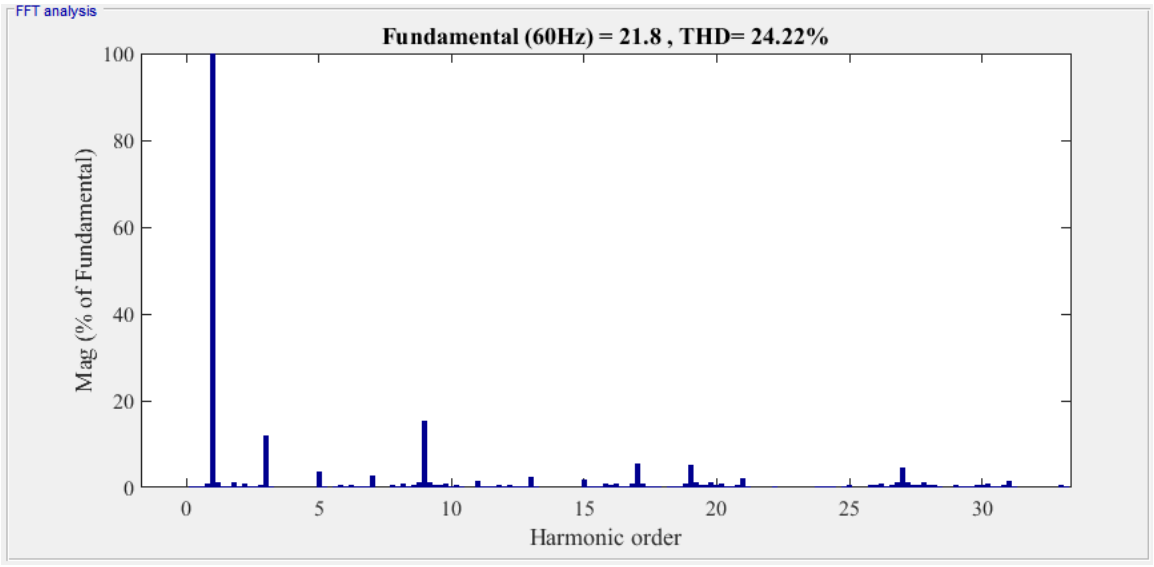

Figure 4.28: Single-phase output voltage harmonic contents using π/3 method

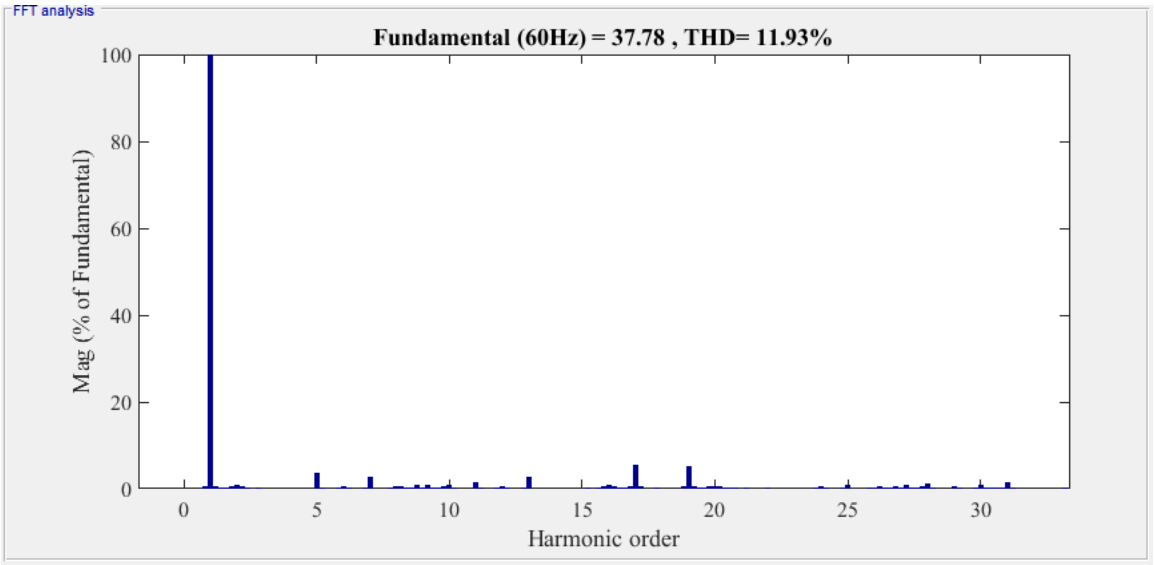

Figure 4.29: Three-phase output voltage harmonic contents using π/3 method

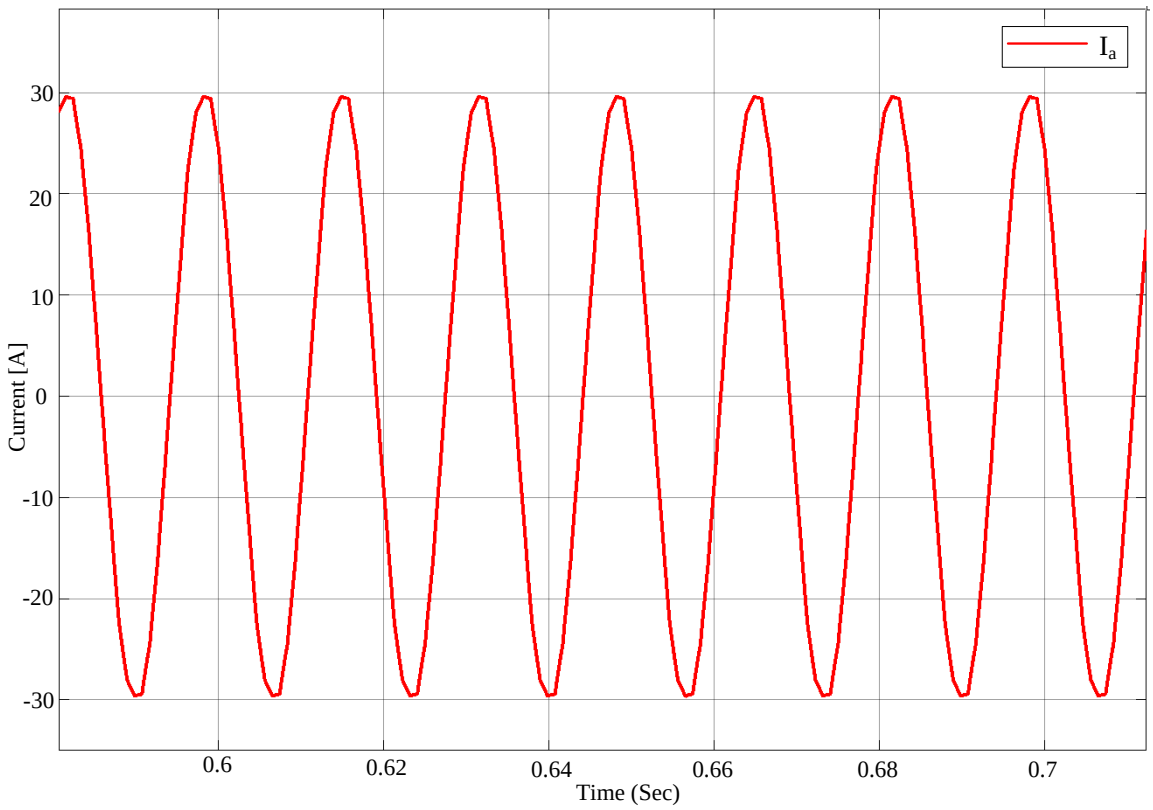

Figure 4.30: Phase current waveform using π/3 method

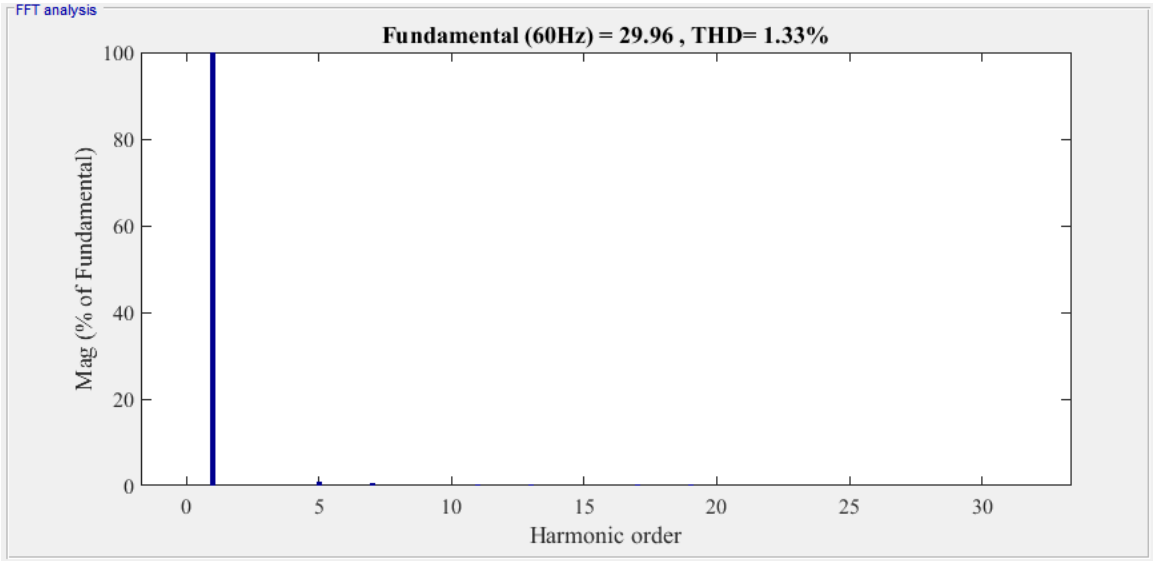

Figure 4.31: Phase current harmonic contents using π/3 method

4.4 Analysis

The simulation results were previously for certain modulation index values to get an overview of the simulation results for the five-level three-phase inverter and to recognize the difference between the two methods. A variety of simulation has been done for both methods at different modulation indices, as shown in Figure 4.32. Figure 4.33 shows the fifth harmonic contents for both methods at different modulation indices. Figure 4.34 shows the seventh harmonic contents for both methods at different modulation indices. Figure 4.35 shows the eleventh harmonic contents for both methods, which is the first non-zero harmonic. Figure 4.36 shows the fundamental component amplitude for both methods at different modulation indices.

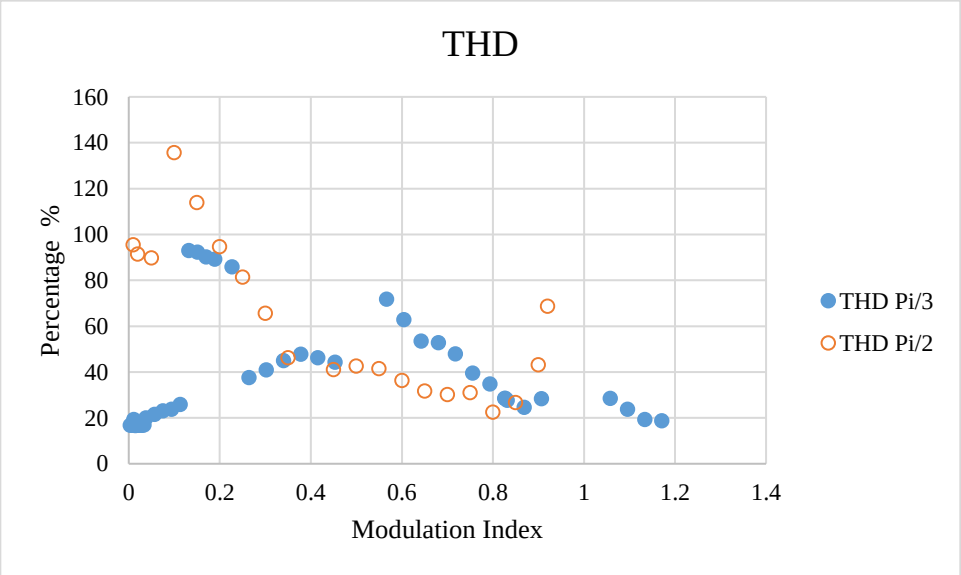

Figure 4.32: THD for both methods at different modulation indices

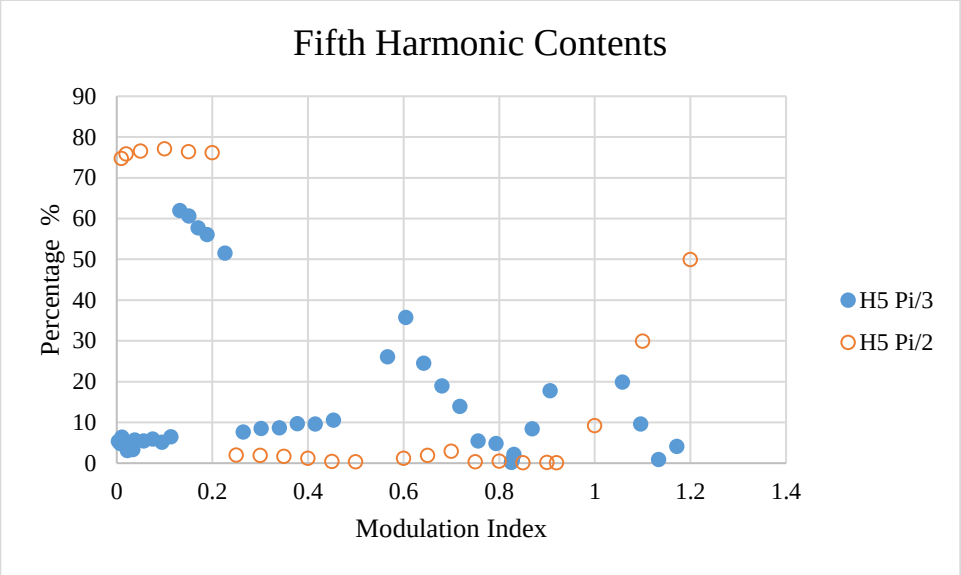

Figure 4.33: Fifth harmonic contents for both methods at different modulation indices

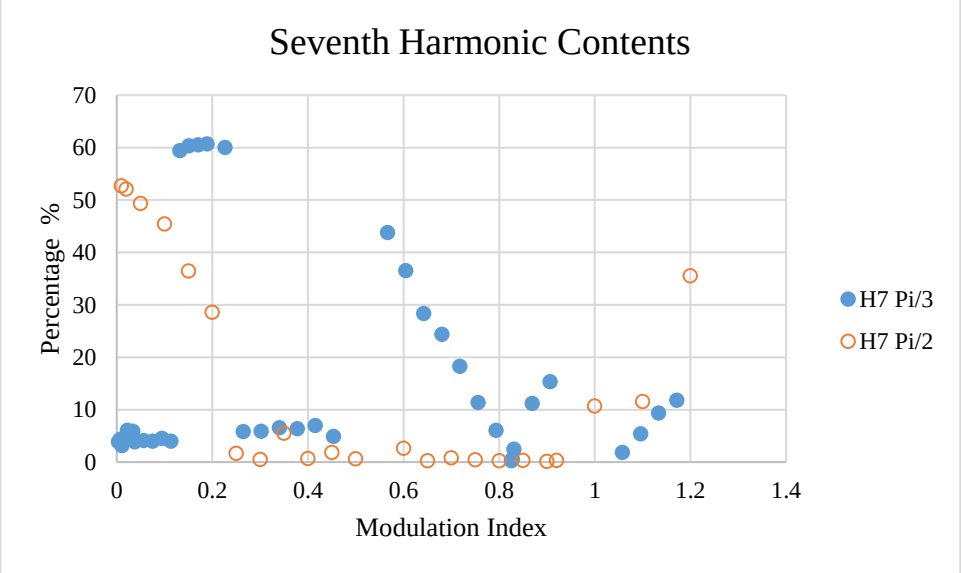

Figure 4.34: Seventh harmonic contents for both methods at different modulation indices

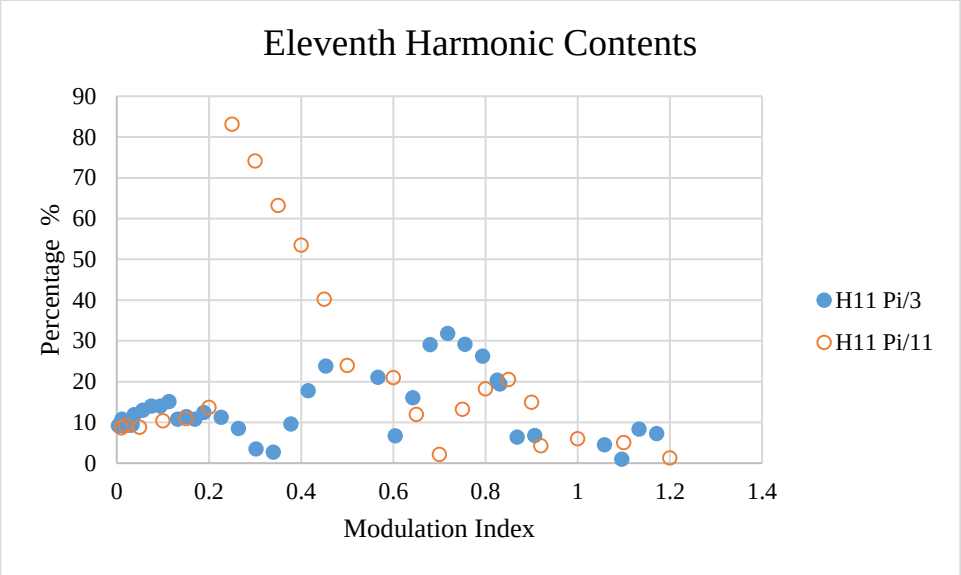

Figure 4.35: Eleventh harmonic contents for both methods at different modulation indices

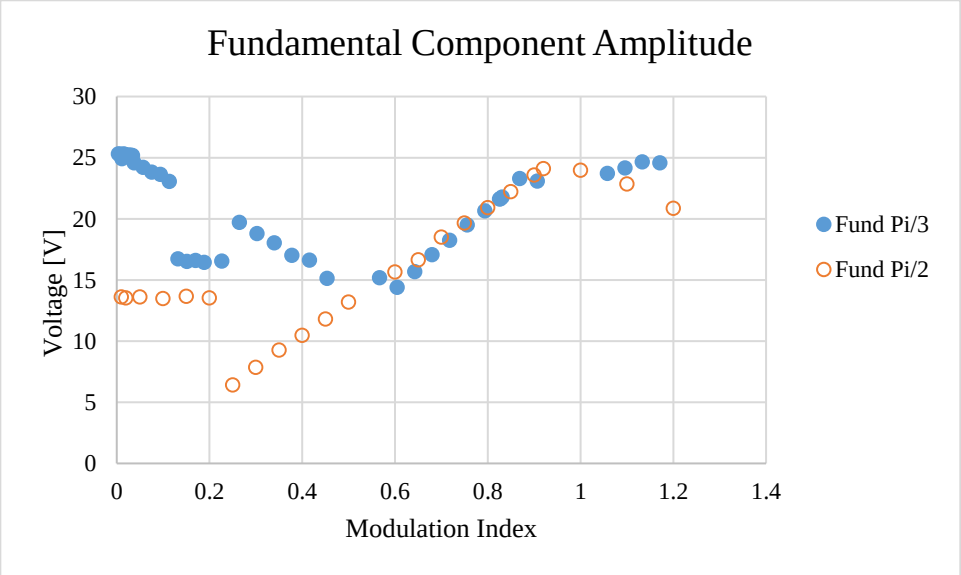

Figure 4.36: Fundamental component amplitude for both methods at different modulation indices

A variety of simulations have been done for both methods at different modulation indices to get an overview of the simulation results for the seven-level three-phase inverter and to recognize the difference between the two methods. Figure 4.37 shows THD for both

methods at different modulation indices. Figures 4.38, 4.39, and 4.40 show the fifth, seventh, and eleventh harmonic contents for both methods at different modulation indices, respectively. Figure 4.41 shows the thirteenth harmonic contents for both methods, which is the first non-zero harmonic. Figure 4.42 shows the fundamental component amplitude for both methods at different modulation indices.

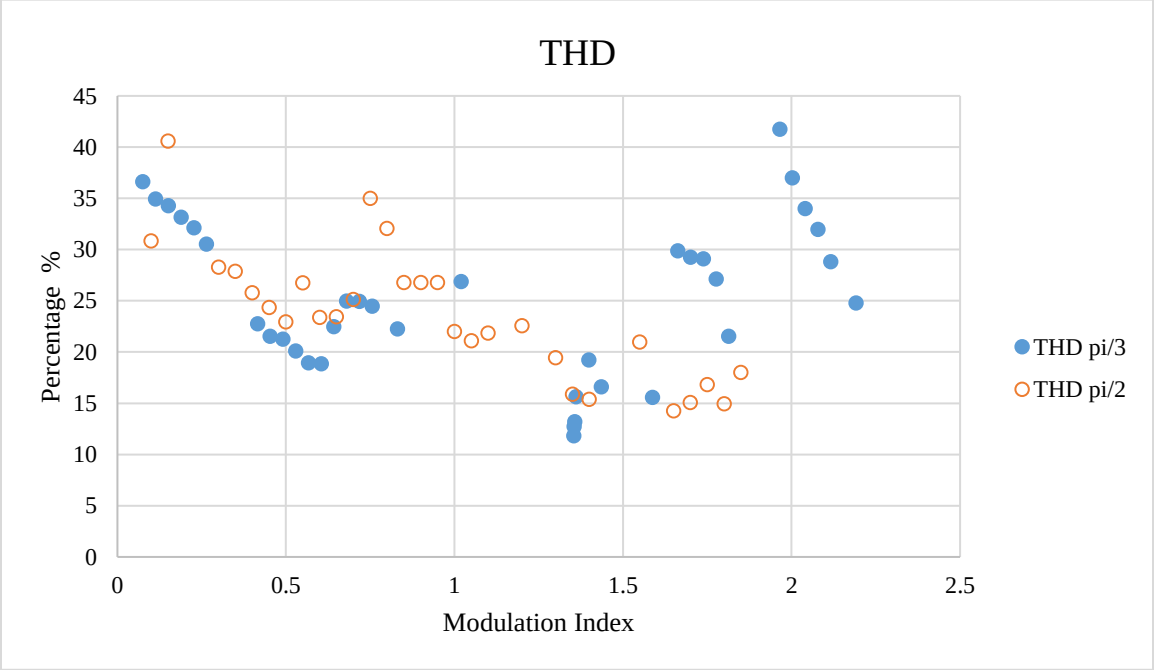

Figure 4.37: THD for both methods at different modulation indices

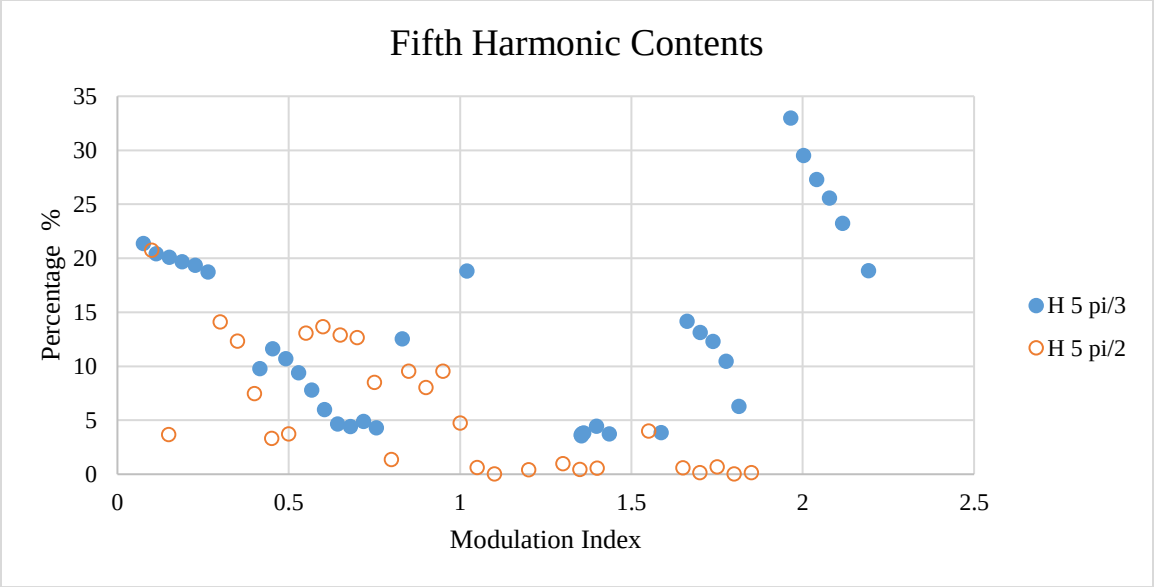

Figure 4.38: Fifth harmonic contents for both methods at different modulation indices

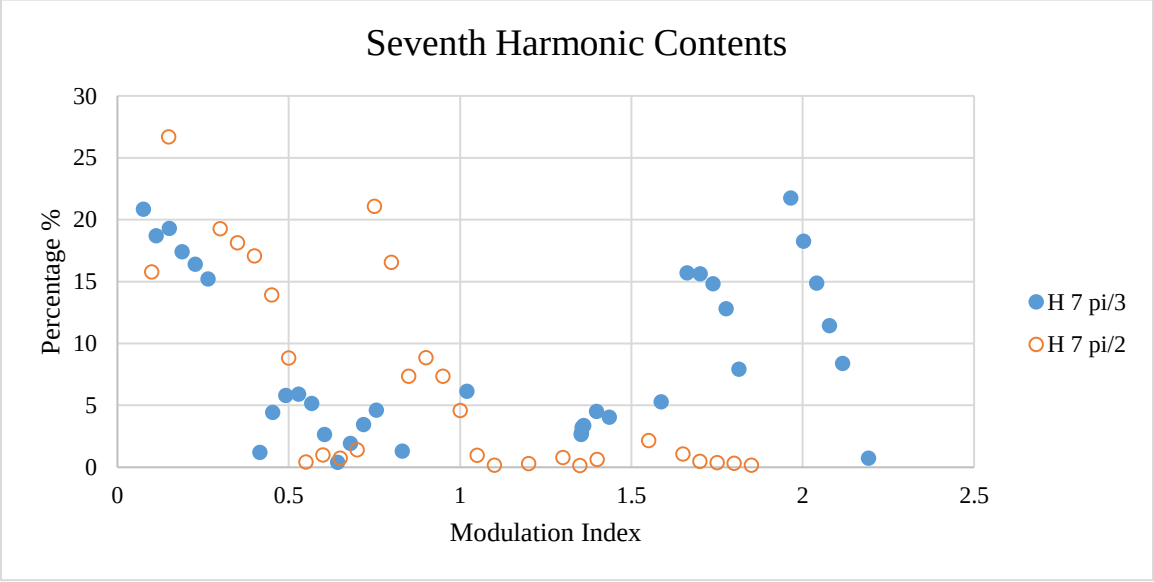

Figure 4.39: Seventh harmonic contents for both methods at different modulation indices

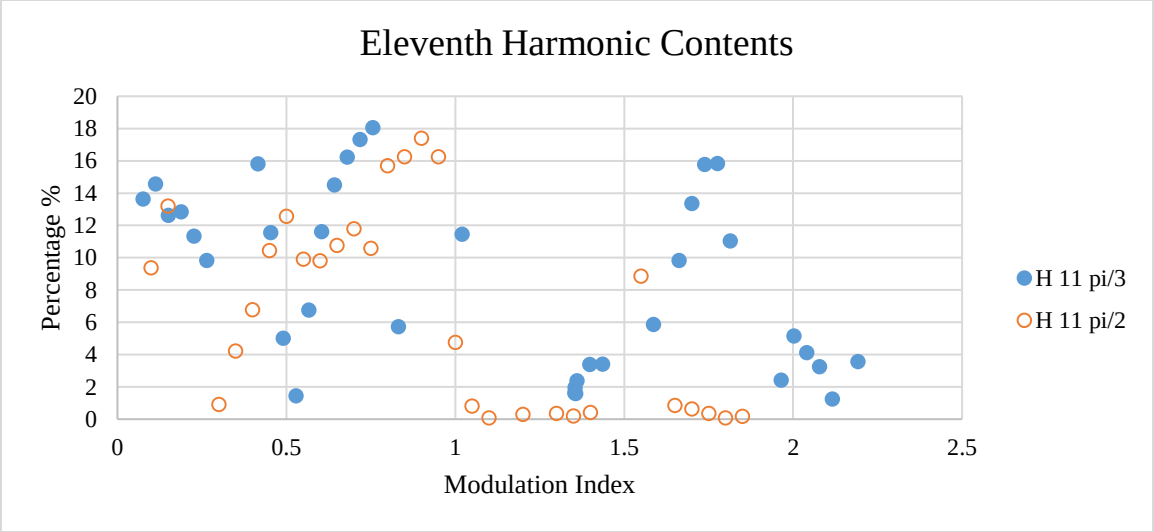

Figure 4.40: Eleventh harmonic contents for both methods at different modulation indices

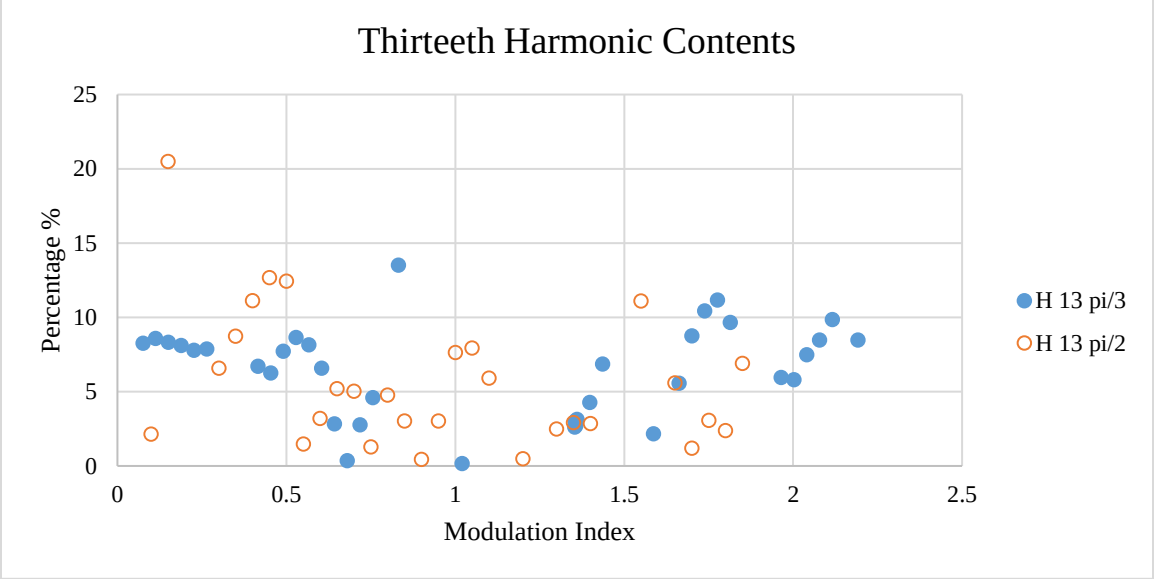

Figure 4.41: Thirteenth harmonic contents for both methods at different modulation indices

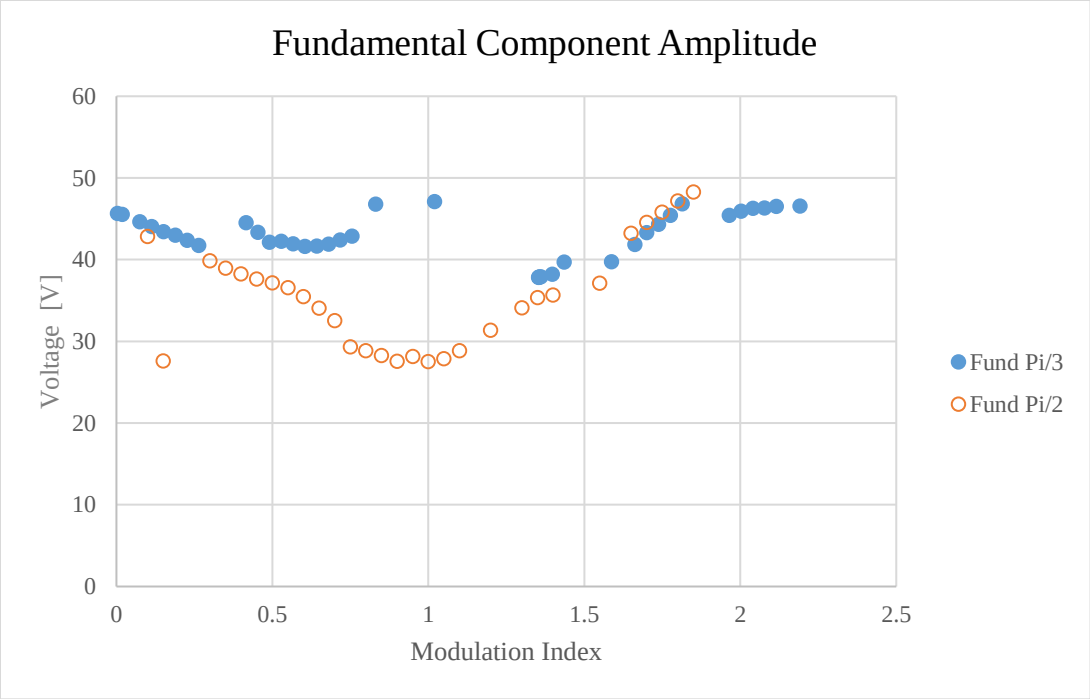

Figure 4.42: Fundamental component amplitude for both methods at different modulation indices

Based on the above comparison charts, Tables 4.1 and 4.2 have been developed to illustrate the differences in the THD results between the two method that have been used to find switching angles. Table 4.1 shows the THD values for the five-level inverter for both methods. Table 4.2 shows the THD values for the seven-level inverter.

Table 4.1: THD values for the five-level inverter for both methods

Method	Min Voltage THD (%)	Max Voltage THD (%)
π/2 Method	22.52	135.77
π/3 Method	16.75	92.96

Table 4.2: THD values for the seven-level inverter for both methods

Method	Min Voltage THD (%)	Max Voltage THD (%)
π/2 Method	14.27	40.6
π/3 Method	11.83	41.74

From the two tables above, it can be concluded that the minimum THD provided by the π/3 method is lower than the one provided by the π/2 method by 25% in the five-level inverter and 17% in the seven-level inverter. Also, it can be seen from the presented comparison charts that a lower THD can be delivered using the π/3 method during low modulation indices. This satisfies the main purpose of the VSPWM for minimizing the THD at a wide range of modulation indices.

Based on the above comparison charts, Tables 4.3 and 4.4 have been developed to illustrate the differences in the fundamental components value between the two method that have been used to find switching angles. Table 4.1 shows the THD values for the five-level inverter for both methods. Table 4.2 shows the THD values for the seven-level inverter.

Table 4.3: Fundamental component values for the five-level inverter for both methods

Method	Min Value (V)	Max Value (V)
π/2 Method	6.423	24.11
π/3 Method	14.4	25.31

Table 4.4 Fundamental components values for the seven-level inverter for both methods

Method	Min Value (V)	Max Value (V)
π/2 Method	27.52	48.3
π/3 Method	37.81	47.1

From the above two tables, better fundamental frequency amplitude values can be generated with the π/3 method. The minimum value for the fundamental component that can be generated by the π/3 method is higher than the minimum value that can be generated by the π/2 method by 125% in the five-level inverter and 38% in the seven-level inverter. In addition, a lower content can be noted for the values of the first non-zero harmonic contents.

4.5 Conclusion

In this chapter, the theoretical methodology was discussed. Both the π/2 method and the π/3 method were presented to derive the set of equations needed to find the unknown switching angles. The π/2 method looks to the waveform from a single-phase perspective. The π/3 method looks to the waveform from a three-phase perspective. Several sets of equations have been presented and solved for five- and seven-level inverters. The values of the unknown switching angles were different in each method.

A simulation model has been built for the five- and seven-level inverters using the MATLAB program to run the single-phase and the three-phase model of the proposed solutions. The simulation has been done for both inverters, and the unknown switching angles were found using both the π/2 method and the π/3 method. The single- and the three-

phase output voltage were presented with their harmonic contents. Also, the line current and its harmonic contents were illustrated.

To get a better look at the results, both inverter outcomes have been compared depending on the findings of the unknown angles. These angles have been found in two different methods. The comparison has been done at different modulation indices to provide an overview of the results.

Based on the comparison, the three-phase perspective decreases the output voltage THD by 25% in the five-level inverter and by 17% in the seven-level inverter. Also, the three-phase perspective increases the minimum value for the fundamental component by 125% in the five-level inverter and by 38% in the seven-level inverter.

CHAPTER 5

EXPERIMENT RESULTS

5.1 Introduction

All of the simulation results in this thesis have been done using MATLAB simulation software, with ideal condition for the switches and diodes. In this chapter, the experiment methodology and results will be shown for two methods that have been used to calculate the unknown switching angles for the five-level inverter to validate the simulation results.

The first section will illustrate the experimental construction and the equipment that have been used to generate the desired output voltage waveform in terms of the controller and the used inverter connection. The next section will provide the experiment results for both methods.

5.2 Experiment Methodology

In this research, an actual experiment has been built. This section has been divided in to two subsections. The first subsection will present the general items that have been used. The second subsection will discuss the control methodology in the experiment.

5.2.1 General Equipment

A three-phase, Wye-connected, five-level (three-phase perspective) cascade H-bridge multilevel inverter was used. The used inverter data sheet is provided in the appendix. The power electronic switches were IGBT with maximum DC voltage 750V and maximum current 30A. Lead acid rechargeable (12V) batteries were used as a separate DC source for the CHB.

For measurements and monitoring, a digital multi-meter and digital storage oscilloscope were used. In addition, a power and energy analyzer and logger was used to measure the THD and display real-time monitoring on a computer.

5.2.2 Experiment Control Methodology

In this experiment, a Raspberry Pi 3 Model B was used to generate the control signal for several IGBTs to generate the desirable output voltage waveform.

The Raspberry Pi is an inexpensive, open-source, credit card-size and single-board computer introduced in 2012 by the Raspberry Pi Foundation [42]. The Raspberry Pi can be used by connecting it to a monitor and using a standard mouse and keyboard. Several programming languages can be used with Raspberry Pi, such as: Scratch, Python, HTML5, and JavaScript. These programming languages allows the Raspberry Pi to do everything a desktop computer can do. In this experiment, Python was selected as the programming language. Different models have been released by the Raspberry Pi Foundation; the most recent was Raspberry Pi 3 Model B, which is the model used in this experiment. Table 5.1 shows Raspberry Pi models' features:

Table 5.1: Raspberry Pi model features

Model	Raspberry Pi 3 Model B	Raspberry Pi Zero	Raspberry Pi 2 Model B	Raspberry Pi Model B+
Release Date	2/29/2016	11/25/2015	2/2/2015	7/14/2014
SoC	BCM2837	BCM2835	BCM2836	BCM2835

CPU	Quad Cortex A53 @ 1.2 GHz	Arm11 @ 1 GHz	Quedan Cortex A7 @ 900 MHz	Arm11 @ 700 MHz
Instruction Set	ARMv8-A	ARMv6	ARMv7-A	ARMv6
GPU	400 MHz VideoCore IV	250 MHz VideoCore IV	250 MHz VideoCore IV	250 MHz VideoCore IV
RAM	1 GB SDRAM	512 MB SDRAM	1 GB SDRAM	512 MB SDRAM
Storage	Micro-SD	Micro-SD	Micro-SD	Micro-SD
Ethernet	10/100	none	10/100	10/100
Wireless	802.11n/Bluetooth 4.0	none	none	none
Video Output	HDMI/Composite	HDMI/Composite	HDMI/Composite	HDMI/Composite
Audio Output	HDMI/Headphones	HDMI	HDMI/Headphones	HDMI/Headphones
GPIO	40	40	40	40
Price ($)	35	5	35	35

Figure 5.1 presents the Raspberry Pi 3 Model B components:

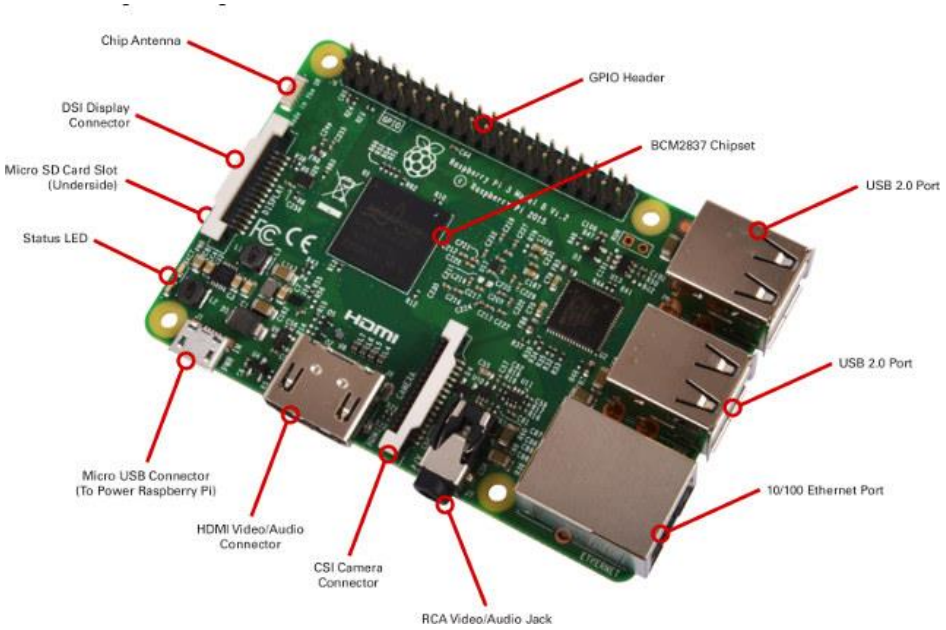

Figure 5.1: Raspberry Pi 3 Model B components [43]

One of the main parts of the Raspberry Pi is the GPIO header, which consists of 40 pins. Each pin has a function, as shown in Figure 5.2. The control signal has been taken from the output pins in the GPIO header. This control signal from the GPIO consists of highs and lows. If it is high, the output voltage is 3.3V; if it is low, the output voltage is 0. On the other hand, to control the IGBT inside the inverter, the high signal must be 15V. Thus, an amplification circuit has been built to increase the voltage amplitude of the control signal that is generated from the Raspberry Pi from 3.3V to 15V. The operational amplifier is the one that has been used. Chip LM324-N from Texas Instruments has been implemented with combinations of resistors to amplify the voltage to the desirable value. Figures 5.3 and 5.4 present the experiment block diagram and experiment actual setup, respectively.

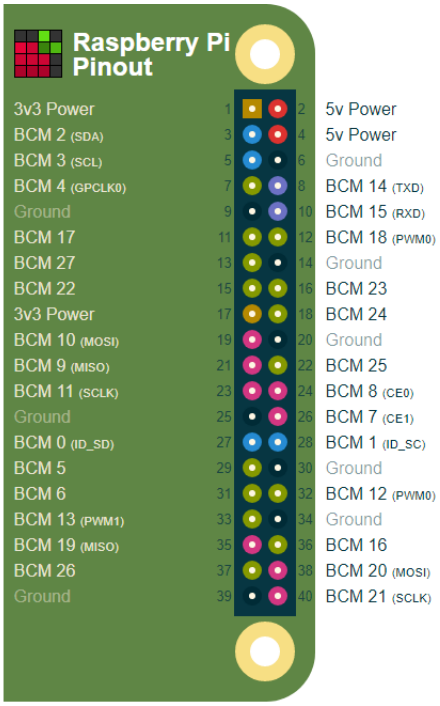

Figure 5.2: GPIO header map [44]

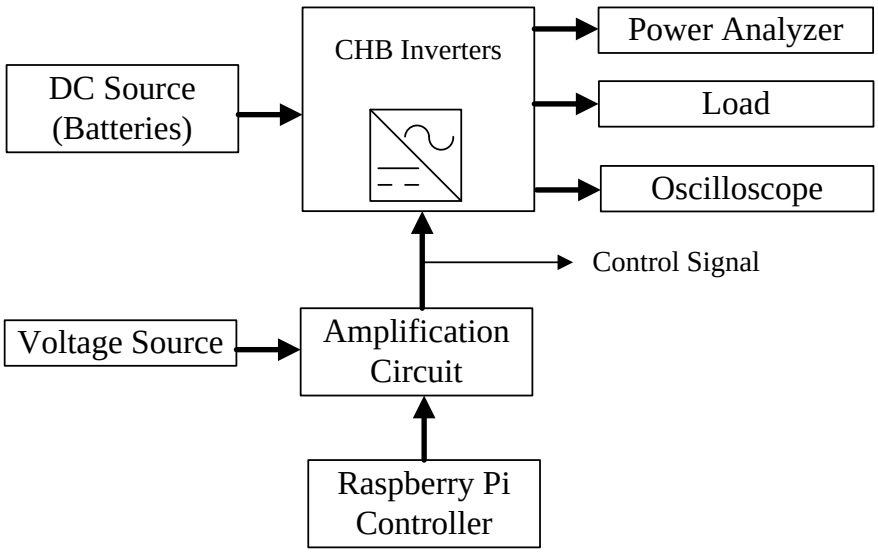

Figure 5.3: Experiment block diagram

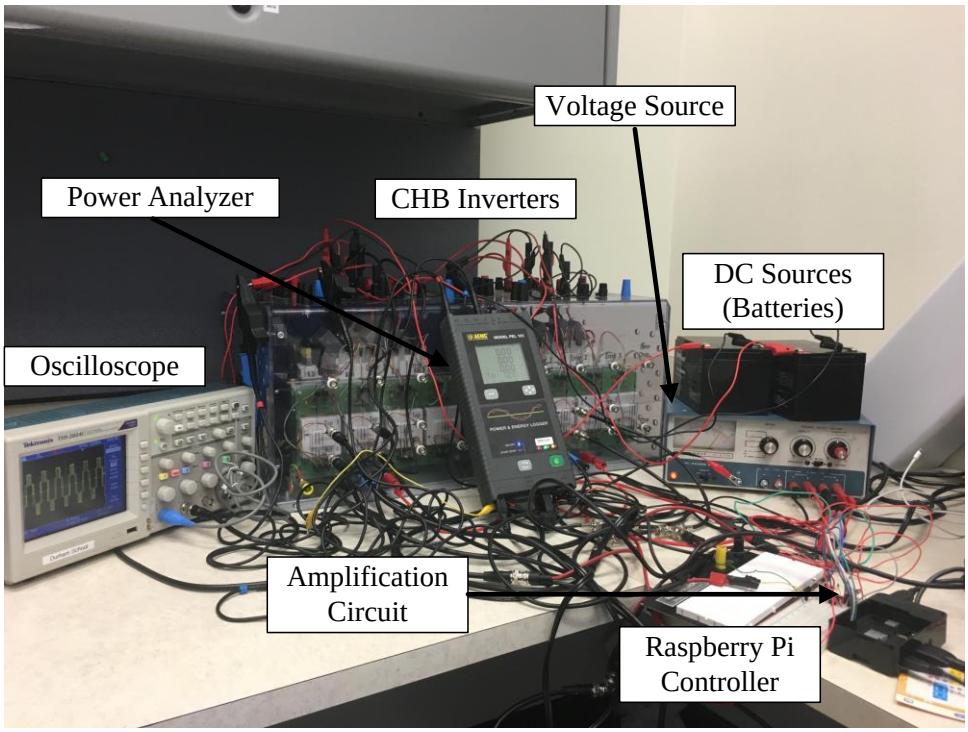

Figure 5.4: Experiment actual setup

5.3 Experimental Result

To validate the simulation results for the five-level inverter, an experiment was built, as discussed in Section 5.2 The output voltage waveform results were taken from digital oscilloscope. Also, the harmonic contents charts were recoded using a power analyzer connected to a PC. Next, a load of 21 Ohms was connected to validate the harmonic contents in the output current. Figures 5.5 and 5.6 show the line-to-line output voltage waveform using the $\pi/2$ method and the $\pi/3$ method, respectively. Figures 5.7 and 5.8 portray the line-to-line output voltage harmonic contents using the $\pi/2$ method and the $\pi/3$ method, respectively. Figures 5.9 and 5.10 show the output line current harmonic contents using the $\pi/2$ method and the $\pi/3$ method, respectively.

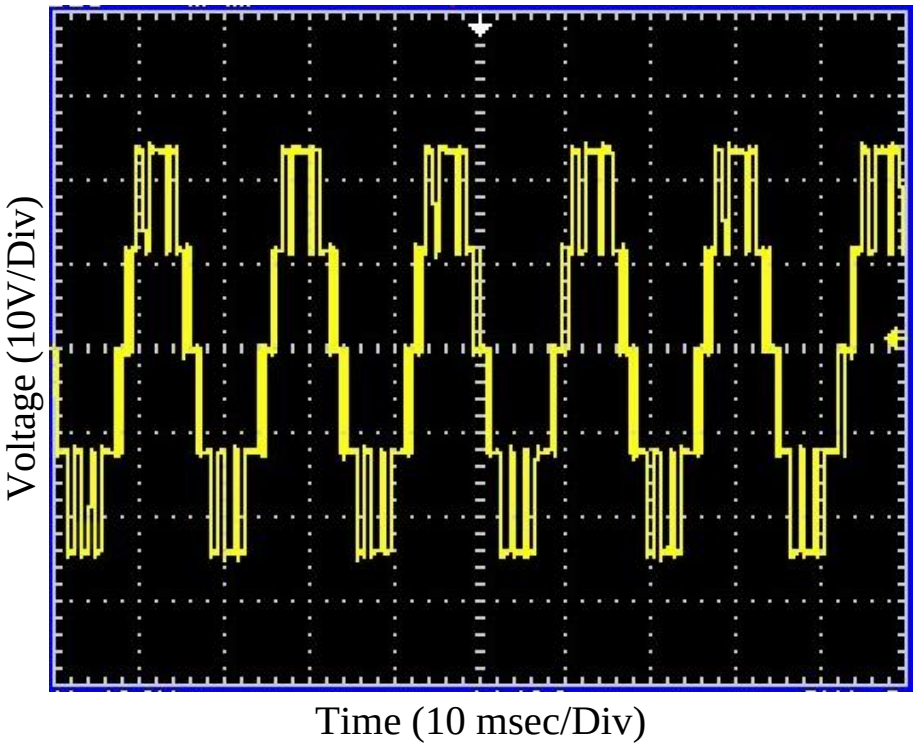

Figure 5.5: Line-to-line output voltage waveform using π/2 method

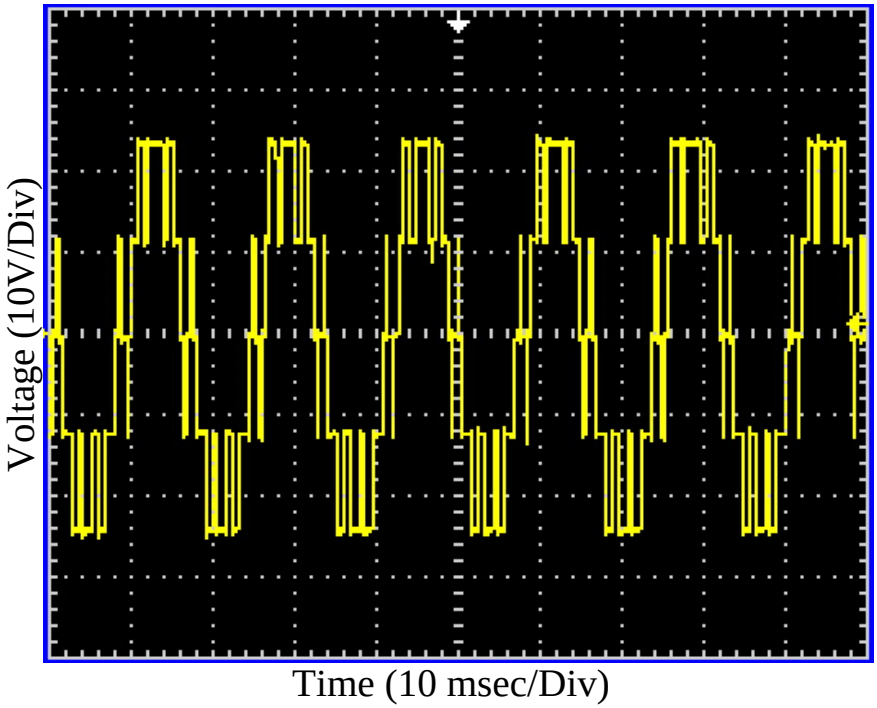

Figure 5.6: Line-to-line output voltage waveform using π/3 method

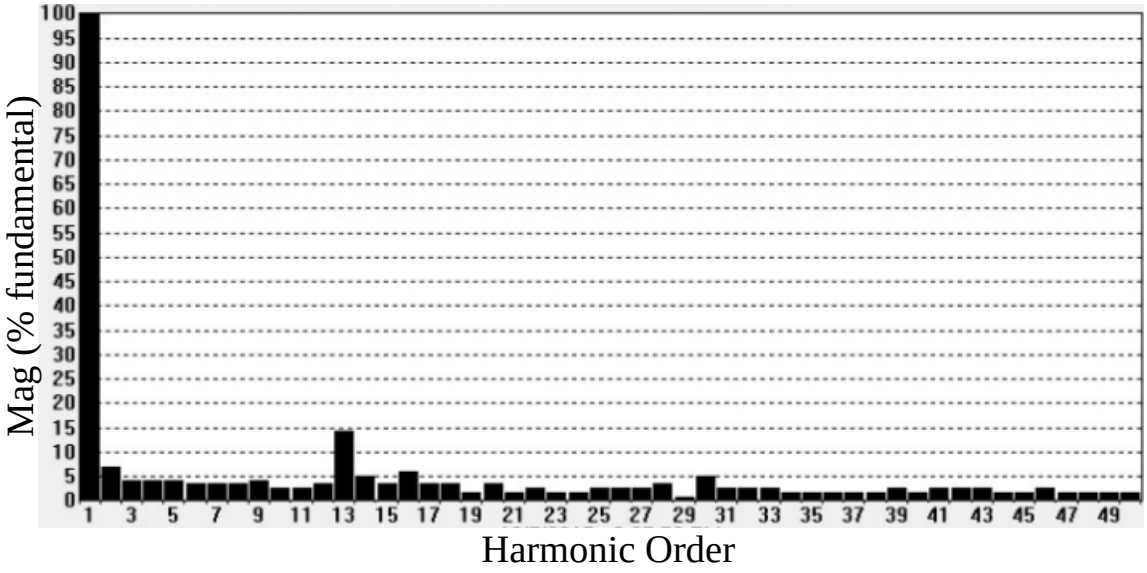

Figure 5.7: Line-to-line output voltage harmonic contents using π/2 method

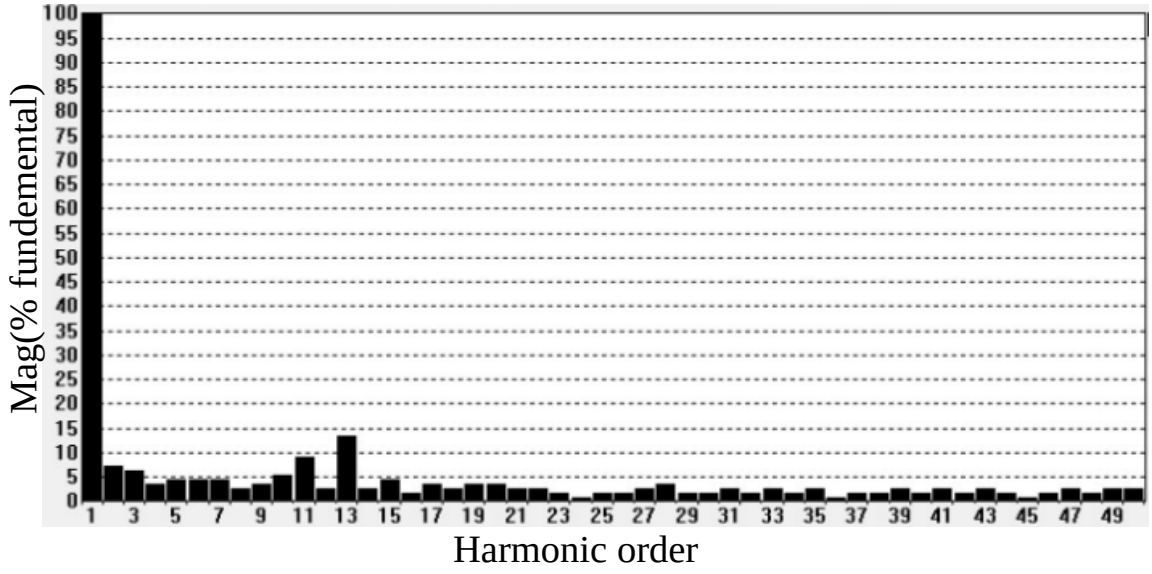

Figure 5.8: Line-to-line output voltage harmonic contents using π/3 method

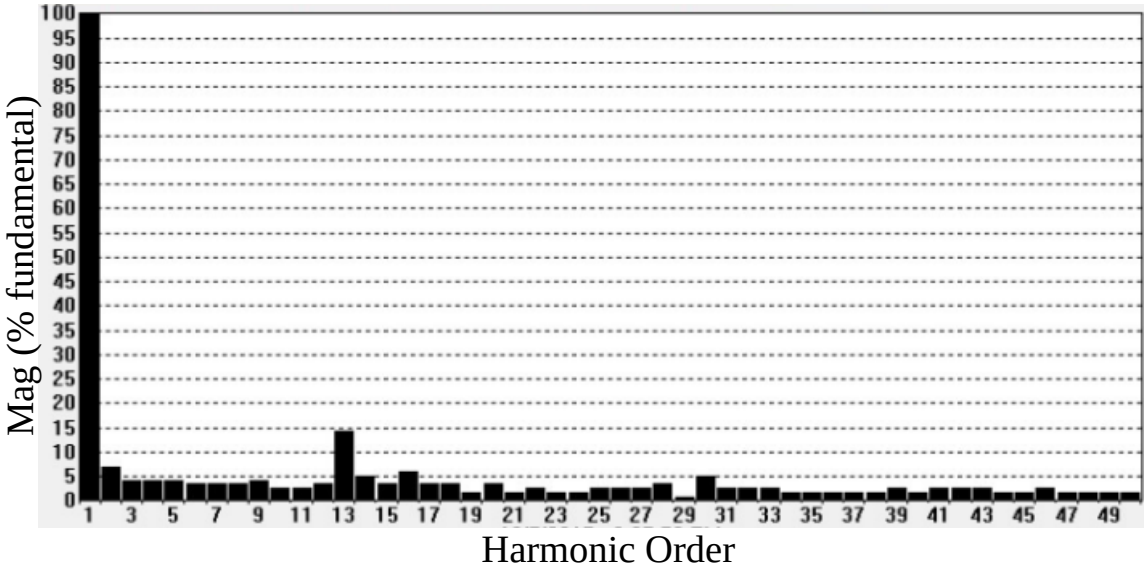

Figure 5.9: Output line current harmonic contents using π/2 method

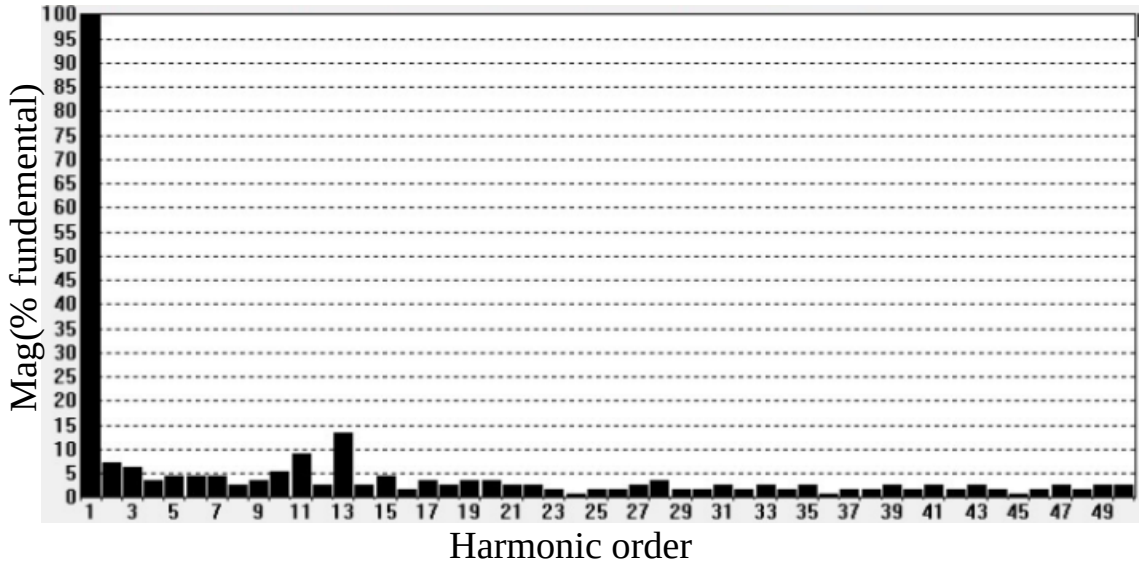

Figure 5.10: Output line current harmonic contents using π/3 method

5.5 Conclusion

In this chapter, the experiment methodology for the five-level inverter was illustrated. The main purpose of the experiment was to validate the simulation results that are presented in Chapter 4. A detailed discussion has been provided about the equipment and controller that were used. The results for the three-phase system validate the simulation results from the THD, the eliminated harmonic contents, and the fundamental component differences between the two methods. Then, to validate the simulation results, the experiment results were presented for the three-phase parameters. Table 6.1 shows the simulation and the experimental results.

Table 6.1: The simulation and experimental results

	Single phase perspective method		Three phase perspective method	
	Simulation	Experiment	Simulation	Experiment
Fundamental	21V	20.2 V	21.7 V	20.9 V
THD	30.58 %	27.5 %	26.61%	24.26 %

The next chapter will provide a brief summary of the thesis. Also, it will give the conclusions that have been made regarding the research. Finally, an illustration and suggestions for future work will be presented.

CHAPTER 6

SUMMARY AND FUTURE WORK

6.1 Introduction

This chapter will include both the thesis summary and future work. Section 6.2 will provide a summary for the thesis. Section 6.3 will include the final results and conclusion of the work. In Section 6.4, a presentation of extension for this work and new ideas in the field of multilevel inverters will be provided.

6.2 Thesis Summary

Chapter 1 presented the motivation behind this thesis by giving a brief summary about the value and development of multilevel inverters. Also, it provided the objective of the work and the thesis outline.

Chapter 2 illustrated the general idea of the multilevel inverters and its working principle. Then, a detailed discussion was presented for the three most well-known topologies: H-bridge inverter (CHB), neutral point clamped (NPC), and the flying capacitor (capacitor-clamped). In addition, the advantages and disadvantages of each of these three topologies was mentioned.

Chapter 3 covered the multilevel inverter modulation techniques and illustrated the classification of them depending on their switching frequency. However, it provided the idea of the Fourier series to eliminate several harmonic orders and the derivation for both the $\pi/2$ method from the single-phase perspective and the $\pi/3$ method from the three-phase perspective.

The purpose of Chapter 4 was to discuss the methodology that has been used in this research. An illustration of the theoretical part of this research was provided, as well as the idea behind the VSPWM and the benefits of such a modulation technique. In addition, the chapter provided the derivation of the sets of equations that were used to find the three switching angles in both methods to eliminate the fifth and the seventh harmonic orders in the VSPWM for five-level inverters—as well as to find the four switching angles in both methods to eliminate the fifth, seventh, and eleventh harmonic orders for seven-level inverters. The derivation has been made for a certain modulation index. To get a better overview of the behavior of both methods at different modulation indices, a comparison between the two methods was presented for both inverters. Finally, depending on the finding of the unknown angles for the VSPWM, a three-phase H-bridge multilevel inverter was constructed using the MATLAB program. The simulation results were presented for each inverter for both the single-phase and the three-phase for both methods that were used to find the unknown angles.

The experimental methodology was presented in Chapter 5 to validate the simulation results. The general equipment that was used to construct the experiment was illustrated. Also, Chapter 5 described the construction of the Raspberry Pi that was used as a controller in this research. In addition, the chapter illustrated the circuits used with this type of controller to allow it to control the inverter. Then, the construction of the actual experiment was shown. Finally, the experimental results were presented to validate the previous simulation results.

6.3 Thesis Conclusions

The multilevel level inverters took a place in today's market due to their advantages over other types of inverters. Also, the CHB gained more importance in recent years because of its advantages over other topologies for the multilevel inverter. The THD for any inverting process is considered one of the most important features. Also, the low harmonics order is the most dangerous harmonic for any system. The number of the eliminated harmonics in the CHB depends on the number of voltage levels. To increase the number of the eliminated harmonics without increasing the level, the switching frequency must increase. In case of high frequency, the efficiency of the inverter decreases. So, to keep high efficiency and to eliminate more low harmonic orders, the VSPWM was represented. To find the switching angles in the VSPWM for both five- and seven-level inverters, two different methods have been presented. The first method finds them from the single-phase perspective in the interval $(0, \pi/2)$, and the other method finds them from the three-phase perspective in the interval $(0, \pi/3)$. The results show that the three-phase perspective method decreases the output voltage THD by 25% in the five-level inverter and by 17% in the seven-level inverter. Also, the three-phase perspective method increases the minimum value for the fundamental component by 125% in the five-level inverter and by 38% in the seven-level inverter. On the other hand, finding the angles from the three-phase perspective guarantees the three-phase output voltage signal shape that guarantees a minimum amplitude for the output generated voltage.

6.4 Future Work

6.4.1 Validation on other topologies

To provide better efficiencies and better output quality for the generated voltage from other MI topologies, an extension to this work can be done by testing and operating different MI topologies using the same concept of the VSPWM with the three-phase method to find the unknown angles and compare it with the single-phase method.

6.4.2 Unequal DC sources

In this research, three equal DC voltage sources were used to build the five-level inverter. Another concern for future research is using different voltage sources and finding the switching angles using the three-phase method to find the switching angles and then apply it to the CHB multilevel inverter to investigate the effect of the unequal sources on the results regarding the THD and the fundamental frequency components amplitude.

6.4.3 Seven-level inverter Experiment

The simulation was built to cover both five- and seven-level inverters. The experiment was built to validate the five-level inverter only. The extension for this work is to validate the seven-level inverter simulation results.

6.4.4 Harmonics elimination depending on the application

In this thesis, an elimination to the low order harmonics for the five- and seven-level inverters was studied as a conclusion to provide the lowest THD. Another general study will be conducted to eliminate a different harmonics order at different modulation indices to derive the optimal eliminated harmonic contents for each MI application.

6.4.5 Input control methodology

All of the above future work was regarding the inverter itself. A new idea of increasing the system efficiency and solving the problem of unequal DC sources will be done by monitoring and controlling the battery strings, which will control the input side of the inverter. Figure 2.8 illustrated the output wave from two CHB multilevel inverters.

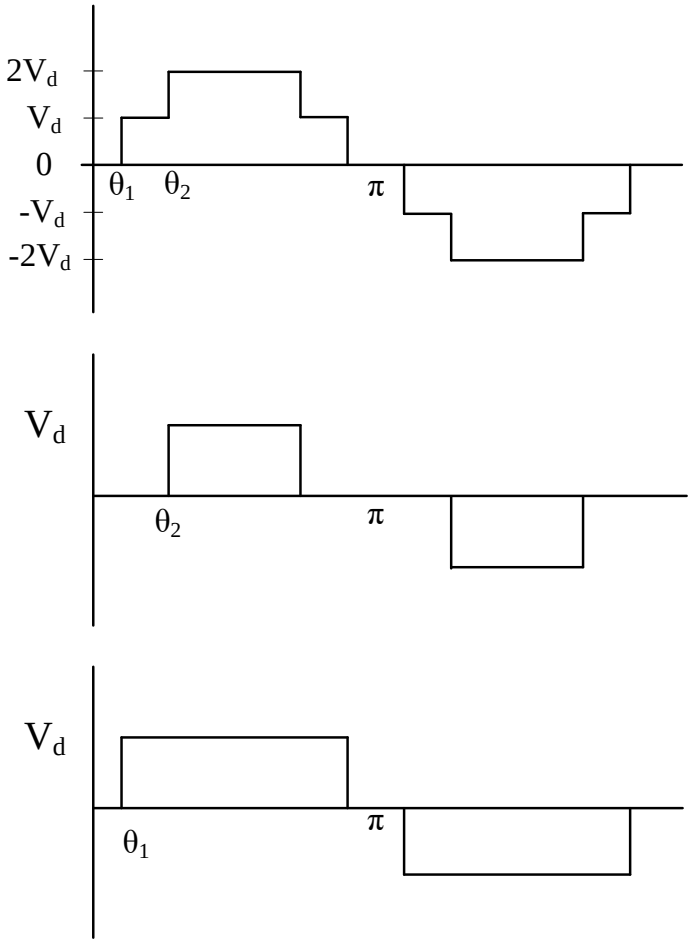

Figure 2.8: Voltage output from the lower cell, upper cell, and total voltage from both cells

It can be seen that the output from the lower cell is much larger than the output from the upper cell. This difference in discharge in each cycle creates an imbalance in the state of charge of the batteries that affects the performance of the system. It also creates an undesired output voltage waveform. A proposed solution for this problem is monitoring

the battery bank strings to provide a good indication of the strings' state. Depending on this state, an algorithm can be built to control which string will be used as a source on each cycle to keep a healthy, balanced battery bank. Power electronic switches will be installed on top of each string to allow this type of control. Figure 6.1 illustrates the schematic diagram for the proposed control methodology for the single-phase five-level CHB.

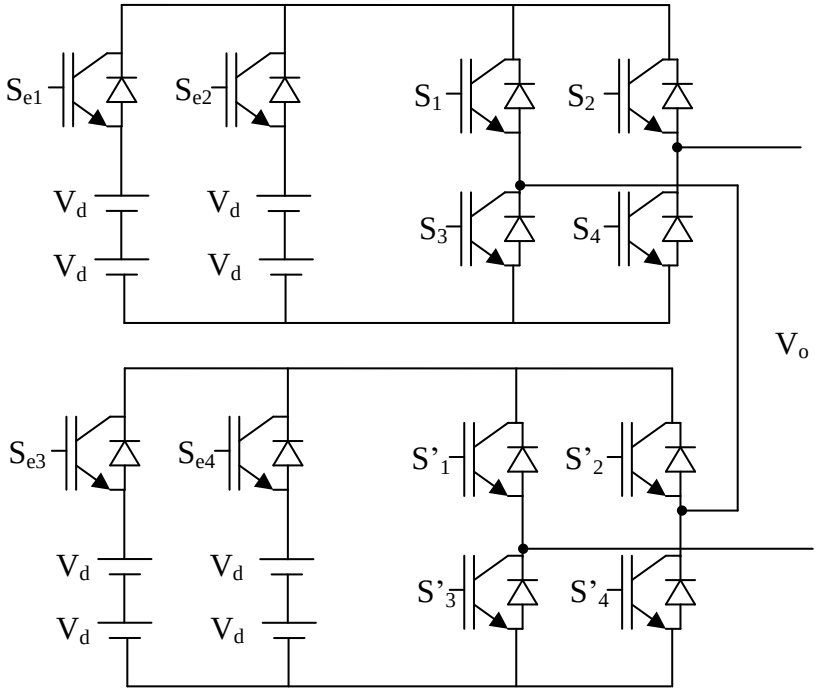

Figure 6.1: Proposed control methodology for single-phase five-level CHB

In this case, the number of power switches will not be as high as if each single battery was controlled separately. It is a promising solution, especially for high-power applications where multistring battery banks will be used to supply the MIs. In addition, the imbalance in the sources in such applications will provide undesired harmonic contents in the generated voltage signal.

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APPENDIX

Table 1: Switching angles, harmonic contents, and THD for a five-level inverter using π/2 method

m_a	θ_1	θ_2	θ_3	H5	H7	H11	THD	Fundamental (V)
0.01	15.166	44.6618	74.6984	74.72	52.7	8.66	101.25	13.62
0.02	15.334	44.3224	74.3963	75.82	52.1	9.33	101.1	13.53
0.05	15.838	43.2965	73.4877	76.55	49.37	8.84	98.62	13.62
0.1	16.676	41.555	71.9637	77.08	45.46	10.39	95.59	13.48
0.15	17.495	39.7615	70.426	76.42	36.47	10.96	91.41	13.66
0.2	18.266	37.8949	68.8715	76.16	28.57	13.69	89.86	13.52
0.25	55.583	63.5916	82.5557	2.02	1.67	83.15	135.77	6.423
0.3	54.633	64.0672	80.8792	1.88	0.53	74.16	114	7.85
0.35	53.650	64.364	79.0508	1.66	5.51	63.19	94.7	9.265
0.4	52.612	64.3694	76.976	1.2	0.71	53.45	81.46	10.47
0.45	51.468	63.8533	74.4707	0.46	1.86	40.23	65.68	11.8
0.5	50.065	62.2669	71.1289	0.37	0.66	24	46.21	13.18
0.55	N.S	N.S	N.S	N.S	N.S	N.S	N.S	N.S
0.6	41.623	48.734	59.201	1.23	2.63	21.01	41.17	15.65
0.65	34.291	41.8415	55.3328	1.94	0.28	12	42.67	16.64
0.7	29.730	39.4188	52.8316	2.93	0.83	2.17	41.53	18.49
0.75	26.431	38.5453	50.4575	0.37	0.47	13.24	36.31	19.64
0.8	23.630	38.0607	47.8397	0.51	0.29	18.21	31.71	20.91

0.85	20.968	37.1168	44.4691	0.11	0.33	20.51	30.22	22.23
0.9	17.863	33.1446	38.233	0.16	0.17	14.95	31.12	23.59
0.92	15.215	26.9516	32.1732	0.08	0.34	4.29	22.52	24.11
1	15.655	59.9916	62.9177	9.2	10.69	6.01	26.72	23.98
1.1	9.7466	43.9985	52.7766	29.94	11.57	5.03	43.2	22.85
1.2	1.1533	38.2031	54.1532	49.97	35.59	1.26	68.76	20.85

Table 2: Switching angles, harmonic contents, and THD for a five-level inverter using π/3 method

m_a	θ_1	θ_2	θ_3	H5	H7	H11	THD	Fundamental (V)
0.00377	14.886	15.127	44.937	5.37	3.85	9.19	16.8	25.31
0.00755	14.772	15.255	75.125	4.83	4.34	9.18	16.8	25.28
0.01133	14.658	15.383	44.811	6.39	3.15	10.7	19.3	24.92
0.01511	14.543	15.511	75.252	5	4.18	9.14	16.7	25.3
0.01889	14.429	15.64	75.315	4.63	4.57	9.3	16.8	25.25
0.02267	14.315	15.768	75.378	3.07	6.09	9.44	16.9	25.15
0.02645	14.201	15.897	75.442	3.98	5.21	9.42	16.8	25.21
0.03023	14.086	16.026	75.505	3.54	5.66	9.29	16.8	25.21
0.03400	13.972	16.155	75.569	3.3	5.88	9.43	16.9	25.17
0.03778	13.858	16.284	44.367	5.66	3.87	11.9	20.0	24.56
0.05668	13.284	16.933	44.049	5.47	4.13	12.9	21.5	24.21
0.07557	12.709	17.588	43.731	5.94	3.98	13.9	23.1	23.82
0.09446	12.132	18.250	43.415	5.14	4.52	14.0	23.7	23.64
0.11336	11.554	18.918	43.101	6.47	3.99	15.	25.8	23.05
0.13225	2.0692	2.2714	26.173	61.9	59.4	10.7	92.9	16.71
0.15115	2.3399	2.608	25.613	60.6	60.3	11.4	92.2	16.51
0.17004	2.6022	2.9475	25.047	57.7	60.5	10.8	90.1	16.59
0.18893	2.8551	3.2898	24.473	56.1	60.6	12.4	89.2	16.43
0.22672	3.3274	3.9831	23.300	51.5	60.0	11.2	85.8	16.54
0.26451	6.8348	24.679	40.873	7.66	5.84	8.47	37.6	19.71

0.30230	5.6211	26.327	40.500	8.53	5.91	3.45	41.0	18.8
0.34008	4.3876	28.128	40.292	8.64	6.56	2.68	45.0	18.03
0.37787	3.1286	30.195	40.362	9.67	6.39	9.6	47.7	17.01
0.41566	1.8346	32.728	40.944	9.58	6.97	17.8	46.2	16.61
0.45345	0.4887	36.238	42.626	10.5	4.93	23.8	44.3	15.13
0.49123	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.
0.52902	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.
0.56681	3.7081	4.5372	13.694	26.0	43.8	21.0	71.8	15.18
0.60460	1.2985	12.174	19.155	35.7	36.5	6.71	62.8	14.4
0.64238	4.2282	17.502	24.806	24.5	28.3	16.0	53.5	15.67
0.68017	6.2219	19.911	28.683	18.9	24.3	29.0	52.8	17.06
0.71796	8.013	20.992	31.544	13.9	18.2	31.8	47.8	18.24
0.75575	9.8249	21.515	33.907	5.48	11.4	29.1	39.5	19.5
0.79354	11.795	21.872	36.021	4.84	6.08	26.2	34.8	20.64
0.82565	13.738	22.292	37.733	0.2	0.26	20.3	28.5	21.61
0.82754	13.864	22.326	37.833	0.75	0.57	19.8	28.4	21.65
0.83132	14.123	22.399	38.033	2.16	2.47	19.4	27.7	21.78
0.86911	17.303	23.715	40.092	8.46	11.2	6.41	24.5	23.28
0.90690	23.357	28.2774	42.7717	17.75	15.36	6.75	28.36	23.07
0.94469	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.
0.982478	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.
1.020265	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.
1.058053	6.6095	12.5874	47.8754	19.93	1.83	4.52	28.51	23.72

1.095841	7.2179	15.7122	50.0118	9.62	5.38	1.01	23.77	24.15
1.133628	7.0172	18.1313	52.3081	0.89	9.36	8.33	19.31	24.65
1.171416	6.4371	20.2673	55.0812	4.09	11.84	7.25	18.83	24.57
1.209204	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.

Table 3: Switching angles, harmonic contents, and THD for a seven-level inverter using π/2 method

m_a	θ_1	θ_2	θ_3	θ_4	H5	H7	H11	h13	THD	Fundamental (V)
0.1	29.63	34.45	64.66	68.12	20.7	15.8	9.38	2.13	30.8	42.82
0.15	52.97	56.36	76.00	81.95	3.68	26.7	13.2	20.4	40.6	27.61
0.2	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
0.25	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
0.3	24.53	39.64	61.20	71.25	14.1	19.2	0.9	6.57	28.3	39.88
0.35	23.08	41.14	60.38	71.87	12.3	18.1	4.21	8.72	27.8	38.96
0.4	21.45	42.88	59.62	72.32	7.48	17.0	6.78	11.1	25.7	38.24
0.45	19.46	45.03	59.03	72.45	3.33	13.9	10.4	12.6	24.3	37.64
0.5	16.55	48.75	59.12	71.79	3.73	8.84	12.5	12.4	22.9	37.17
0.55	12.65	57.05	64.87	72.15	13.0	0.43	9.9	1.48	26.7	36.56
0.6	12.41	60.21	69.29	76.49	13.6	1	9.81	3.19	23.3	35.46
0.65	12.79	61.51	70.04	79.08	12.9	0.75	10.7	5.2	23.4	34.08
0.7	13.27	62.44	69.73	80.96	12.6	1.42	11.8	5.02	25.1	32.53
0.75	20.84	44.63	52.79	85.55	8.49	21.0	10.5	1.28	35.0	29.34
0.8	18.49	47.32	52.56	85.50	1.37	16.5	15.6	4.76	32.0	28.85
0.85	15.04	61.90	64.15	85.37	9.53	7.37	16.2	3.02	26.7	28.27
0.9	15.61	56.71	58.29	86.07	8.02	8.87	17.4	0.43	26.7	27.57
0.95	16.01	76.73	79.74	86.40	9.53	7.37	16.2	3.02	26.7	28.15
1	16.65	70.23	74.26	88.57	4.74	4.59	4.75	7.63	22.0	27.52

1.05	17.26	67.98	73.95	89.79	0.62	0.98	0.81	7.93	21.1	27.86
1.1	17.86	66.42	74.44	89.06	0.03	0.17	0.07	5.91	21.8	28.84
1.15	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.2	18.99	63.87	76.18	86.96	0.4	0.3	0.29	0.49	22.5	31.36
1.25	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.3	20.00	61.57	78.60	85.30	0.98	0.8	0.35	2.49	19.4	34.11
1.35	20.44	60.44	80.32	84.96	0.45	0.15	0.19	2.91	15.9	35.34
1.4	0	39.37	59.79	84.88	0.56	0.65	0.42	2.84	15.3	35.67
1.45	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.5	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.55	21.80	56.37	74.02	78.03	3.99	2.18	8.86	11.1	20.9	37.12
1.6	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	
1.65	13.55	39.55	48.38	55.18	0.6	1.08	0.86	5.59	14.2	43.23
1.7	12.31	35.64	45.08	51.94	0.14	0.5	0.64	1.18	15.0	44.58
1.75	10.85	32.99	43.58	49.19	0.68	0.39	0.35	3.07	16.8	45.83
1.8	9.345	30.53	41.06	45.09	0.03	0.33	0.08	2.37	14.9	47.2
1.85	13.54	13.54	20.39	32.99	0.15	0.18	0.17	6.89	18.0	48.28
1.9	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.

Table 4: Switching angles, harmonic contents, and THD for a seven-level inverter using π/3 method

m_a	θ_1	θ_2	θ_3	θ_4	H5	H7	H11	h13	THD	Fundamental (V)
0.0037	9.90	10.07	29.92	49.98	20.7	20.9	13.0	8.04	36.12	45.65
0.0188	9.54	10.68	29.63	49.91	20.8	20.7	13.2	8.04	36.95	45.55
0.0755	8.21	11.46	28.51	49.60	21.3	20.8	13.6	8.25	36.64	44.64
0.1133	7.33	12.18	27.74	49.36	20.4	18.7	14.5	8.57	34.96	44.06
0.1511	6.46	12.90	26.96	49.10	20.1	19.3	12.6	8.32	34.29	43.42
0.1889	5.59	13.60	26.15	48.82	19.6	17.4	12.8	8.11	33.17	42.98
0.2267	4.73	14.29	25.32	48.54	19.3	16.4	11.3	7.79	32.12	42.36
0.2645	3.86	14.96	24.46	48.25	18.7	15.2	9.82	7.87	30.53	41.73
0.3023	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
0.3400	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
0.3778	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
0.4156	1.41	32.66	48.62	55.34	9.78	1.21	15.8	6.7	22.76	44.51
0.4534	0.22	31.38	45.76	51.20	11.6	4.45	11.5	6.25	21.55	43.35
0.4912	0.95	30.05	43.01	48.13	10.7	5.82	5.01	7.72	21.25	42.12
0.5290	2.14	28.63	40.23	45.43	9.38	5.91	1.44	8.64	20.11	42.25
0.5668	3.31	27.05	37.28	42.99	7.78	5.18	6.75	8.15	18.94	41.92
0.6046	4.44	25.14	34.11	40.98	5.99	2.65	11.6	6.58	18.85	41.61
0.6423	5.48	22.83	31.22	39.95	4.66	0.42	14.5	2.82	22.48	41.66

0.6801	6.44	20.71	29.66	39.75	4.42	1.95	16.2	0.34	24.99	41.9
0.7179	7.39	19.10	29.20	39.61	4.9	3.46	17.3	2.76	24.95	42.39
0.7557	8.39	17.82	29.27	39.34	4.29	4.63	18.0	4.6	24.49	42.87
0.7935	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
0.8313	5.77	24.85	45.21	57.14	12.5	1.31	5.72	13.5	22.25	46.81
0.8691	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
0.9069	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
0.9446	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
0.9824	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.0202	7.33	11.43	40.63	46.00	18.8	6.16	11.4	0.16	26.88	47.09
1.0580	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.0958	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.1336	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.1714	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.2092	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.2469	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.2847	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.3225	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.3535	0.37	20.50	25.45	35.04	3.65	2.66	1.63	2.61	11.83	37.81
1.3546	0.36	20.71	25.20	35.15	3.55	2.78	1.96	3	12.73	37.88
1.3565	0.34	21.02	25.51	35.31	3.77	3.22	1.58	2.7	13.22	37.86
1.3603	0.28	21.56	26.03	35.62	3.83	3.38	2.37	3.12	15.65	37.92
1.3981	0.56	25.63	29.55	37.88	4.45	4.52	3.39	4.27	19.22	38.2

1.4359	1.62	30.72	34.33	40.15	3.72	4.05	3.41	6.86	16.62	39.7
1.4737	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.5115	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.5492	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.5870	4.45	14.18	19.68	38.10	3.84	5.29	5.87	2.17	15.59	39.75
1.6248	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.6626	5.90	12.99	21.71	46.69	14.1	15.7	9.83	5.57	29.87	41.87
1.7004	8.07	14.92	24.37	47.69	13.1	15.6	13.3	8.76	29.27	43.32
1.7382	10.1	16.06	26.42	48.79	12.3	14.8	15.7	10.4	29.1	44.31
1.7760	12.6	17.39	28.26	49.92	10.4	12.8	15.8	11.1	27.14	45.44
1.8138	16.8	20.55	30.28	51.05	6.27	7.94	11.0	9.66	21.53	46.84
1.8515	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.8893	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.9271	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
1.9649	3.92	8.151	35.34	55.25	32.9	21.7	2.41	5.94	41.74	45.41
2.0027	5.14	11.34	36.83	56.74	29.5	18.2	5.16	5.81	37.02	45.93
2.0405	5.25	13.52	38.36	58.17	27.3	14.8	4.13	7.48	34.02	46.28
2.0783	4.94	15.37	39.94	60	25.5	11.4	3.25	8.47	31.99	46.34
2.1161	4.40	17.08	41.60	59.05	23.2	8.41	1.24	9.85	28.81	46.51
2.1538	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S
2.1916	2.91	20.38	45.37	55.59	18.8	0.76	3.56	8.47	24.79	46.55
2.2294	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S.	N.S

The following Python program was used with Raspberry Pi to generate the control signal for the three-phase CHB using the π/2 method:

```
from time import sleep
import time


def init_gpio():
    if RP_ACTIVE:
        import RPi.GPIO as GPIO
        GPIO.setmode(GPIO.BCM)
        for key in gpio_dic:
            GPIO.setup(gpio_dic[key]['gpio'], GPIO.OUT)

    for key in gpio_dic:
        gpio_dic[key]['next'] = gpio_dic[key]['delay']


def cleanup():
    if RP_ACTIVE:
        import RPi.GPIO as GPIO
        GPIO.cleanup()


def show_result(gpio):
    if RP_ACTIVE:
        import RPi.GPIO as GPIO
        GPIO.output(gpio['gpio'],gpio['val'])
        # print ('time: {}: gpio_{}, {}, {}'.format(time.time(),
gpio['gpio'], gpio['t'], gpio['val']))

    else:
        # print ('time: {}: gpio_{}, {}, {}'.format(time.time(),
gpio['gpio'], gpio['t']-1, (gpio['val'] + 1) % 2 ))
        print ('time: {}: gpio_{}, {}, {}'.format(time.time(),
gpio['gpio'], gpio['t'], gpio['val']))


def process_gpio(gpio, counter):
    if abs(gpio['t'] + counter - gpio['next']) < 1 :
        gpio['t'] = gpio['next']
        gpio['next'] = gpio['t'] + steps[gpio['step']]
        gpio['step'] = (gpio['step'] + 1) % 6
        show_result(gpio)

        gpio['val'] = (gpio['val'] + 1) % 2

    else:
        gpio['t'] += counter

    return (gpio['next'] - gpio['t'])
```

```
def looper():
    counter = 0
    while(1):
        min_val = 1000000
        for key in gpio_dic:
            diff = process_gpio(gpio_dic[key], counter)
            if diff < min_val:
                min_val = diff
        # print(min_val)
        sleep((min_val -1)/1663000.0)
        counter = min_val


steps = [668.074, 452.731, 3903.7314, 452.7314, 668.074, 9427.3287]

gpio_dic = {
        'GPIO_17': {'gpio':17, 'delay': 1093.995, 'step':0, 't': 0,
'val': 1, 'next':0 },
        'GPIO_27': {'gpio':27, 'delay': 9427.328, 'step':0, 't': 0,
'val': 1, 'next':0 },
        'GPIO_22': {'gpio':22, 'delay': 6649.55, 'step':0, 't': 0,
'val': 1, 'next':0 },
        'GPIO_23': {'gpio':23, 'delay': 14982.884, 'step':0, 't': 0,
'val': 1, 'next':0 },
        'GPIO_24': {'gpio':24, 'delay': 12205.106, 'step':0, 't': 0,
'val': 1, 'next':0 },
        'GPIO_25': {'gpio':25, 'delay': 20538.439, 'step':0, 't': 0,
'val': 1, 'next':0 },
        }

RP_ACTIVE = True



init_gpio()
looper()
cleanup()
```

The following Python program was used with Raspberry Pi to generate the control signal for the three-phase CHB using the π/3 method:

```
from time import sleep
import time


def init_gpio():
    if RP_ACTIVE:
        import RPi.GPIO as GPIO
        GPIO.setmode(GPIO.BCM)
        for key in gpio_dic:
            GPIO.setup(gpio_dic[key]['gpio'], GPIO.OUT)

    for key in gpio_dic:
        gpio_dic[key]['next'] = gpio_dic[key]['delay']


def cleanup():
    if RP_ACTIVE:
        import RPi.GPIO as GPIO
        GPIO.cleanup()


def show_result(gpio):
    if RP_ACTIVE:
        import RPi.GPIO as GPIO
        GPIO.output(gpio['gpio'],gpio['val'])
        # print ('time: {}: gpio_{}, {}, {}'.format(time.time(),
gpio['gpio'], gpio['t'], gpio['val']))

    else:
        # print ('time: {}: gpio_{}, {}, {}'.format(time.time(),
gpio['gpio'], gpio['t']-1, (gpio['val'] + 1) % 2 ))
        print ('time: {}: gpio_{}, {}, {}'.format(time.time(),
gpio['gpio'], gpio['t'], gpio['val']))


def process_gpio(gpio, counter):
    if abs(gpio['t'] + counter - gpio['next']) < 1 :
        gpio['t'] = gpio['next']
        gpio['next'] = gpio['t'] + steps[gpio['step']]
        gpio['step'] = (gpio['step'] + 1) % 6
        show_result(gpio)

        gpio['val'] = (gpio['val'] + 1) % 2

    else:
        gpio['t'] += counter

    return (gpio['next'] - gpio['t'])

def looper():
    counter = 0
```

```
    while(1):
        min_val = 1000000
        for key in gpio_dic:
            diff = process_gpio(gpio_dic[key], counter)
            if diff < min_val:
                min_val = diff
        # print(min_val)
        sleep((min_val -1)/1663000.0)
        counter = min_val


steps = [717.921, 391.7361, 4061.555, 391.7361, 717.921, 9359.564]

gpio_dic = {
        'GPIO_17': {'gpio':17, 'delay': 1026.23, 'step':0, 't': 0,
'val': 1, 'next':0 },
        'GPIO_27': {'gpio':27, 'delay': 9359.56, 'step':0, 't': 0,
'val': 1, 'next':0 },
        'GPIO_22': {'gpio':22, 'delay': 6581.787, 'step':0, 't': 0,
'val': 1, 'next':0 },
        'GPIO_23': {'gpio':23, 'delay': 14915.120, 'step':0, 't': 0,
'val': 1, 'next':0 },
        'GPIO_24': {'gpio':24, 'delay': 12137.342, 'step':0, 't': 0,
'val': 1, 'next':0 },
        'GPIO_25': {'gpio':25, 'delay': 20470.675, 'step':0, 't': 0,
'val': 1, 'next':0 },
        }

RP_ACTIVE = True



init_gpio()
looper()
cleanup()
```

TEXAS INSTRUMENTS

LM124-N, LM224-N
LM2902-N, LM324-N

SNOSC16D – MARCH 2000 – REVISED JANUARY 2015

LMx24-N, LM2902-N Low-Power, Quad-Operational Amplifiers

1 Features

- Internally Frequency Compensated for Unity Gain
- Large DC Voltage Gain 100 dB
- Wide Bandwidth (Unity Gain) 1 MHz (Temperature Compensated)
- Wide Power Supply Range:
  - Single Supply 3 V to 32 V
  - or Dual Supplies ±1.5 V to ±16 V
- Very Low Supply Current Drain (700 µA) —Essentially Independent of Supply Voltage
- Low Input Biasing Current 45 nA (Temperature Compensated)
- Low Input Offset Voltage 2 mV and Offset Current: 5 nA
- Input Common-Mode Voltage Range Includes Ground
- Differential Input Voltage Range Equal to the Power Supply Voltage
- Large Output Voltage Swing 0 V to V^+ – 1.5 V
- **Advantages:**
  - Eliminates Need for Dual Supplies
  - Four Internally Compensated Op Amps in a Single Package
  - Allows Direct Sensing Near GND and V_{OUT} also Goes to GND
  - Compatible With All Forms of Logic
  - Power Drain Suitable for Battery Operation
  - In the Linear Mode the Input Common-Mode, Voltage Range Includes Ground and the Output Voltage
  - Can Swing to Ground, Even Though Operated from Only a Single Power Supply Voltage
  - Unity Gain Cross Frequency is Temperature Compensated
  - Input Bias Current is Also Temperature Compensated

2 Applications

- Transducer Amplifiers
- DC Gain Blocks
- Conventional Op Amp Circuits

3 Description

The LM124-N series consists of four independent, high-gain, internally frequency compensated operational amplifiers designed to operate from a single power supply over a wide range of voltages. Operation from split-power supplies is also possible and the low-power supply current drain is independent of the magnitude of the power supply voltage.

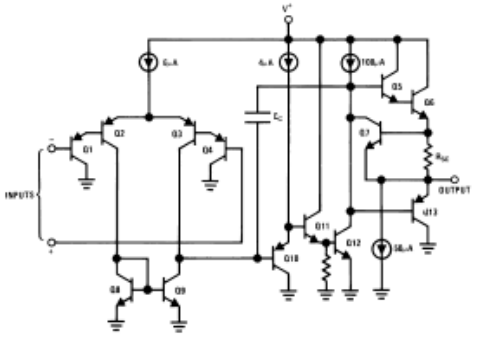
Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124-N series can directly operate off of the standard 5-V power supply voltage which is used in digital systems and easily provides the required interface electronics without requiring the additional ±15 V power supplies.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM124-N	CDIP (14)	19.56 mm × 6.67 mm
LM224-N		
LM324-N	CDIP (14)	19.56 mm × 6.67 mm
	PDIP (14)	19.177 mm × 6.35 mm
	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
LM2902-N	PDIP (14)	19.177 mm × 6.35 mm
	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Schematic Diagram



SEMITEACH IGBT

IGBT Module stack

SEMITEACH - IGBT
3-phase retifier + IGBT inverter + brake chopper

datasheet

Ordering No. 08753450
Description SEMITEACH IGBT
SKM50GB12T4, SKHI22A, SKD51/14

Features

- Multi-function IGBT converter
- IP2x protection for safety hazards
- Transparent enclosure to allow visualisation of internal part
- External connector for easy wiring
- Built in isolated IGBT driver and IGBT protection
- Forced-air cooled heatsink

Typical Applications

- Education : various converter configuration possible :
- 3-phase inverter+brake chopper
- Buck or boost converter
- single phase inverter
- single or 3-phase rectifier

Footnotes

1) The user shall ensure air ventilation for proper cooling

Remarks

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee, expressed or implied is made regarding delivery, performance or suitability.

Absolute maximum ratings			
Symbol	Conditions	Values	Unit
$I_{OUT\ MAX}$	Maximum permanent output current	50	A_{RMS}
$I_{IN\ MAX}$	Maximum permanent input current	50	A_{DC}
$V_{OUT\ MAX}$	Maximum output voltage	400	V_{AC}
$V_{BUS\ MAX}$	Maximum DC bus voltage	750	V_{DC}
f_{OUT}	Maximum inverter output frequency	600	Hz
f_{SW}	Maximum switching frequency	60	kHz

Electrical characteristics / Typical application			$T_{AIR\ COOLING\ 1)}$ = 30°C unless otherwise specified			
Symbol	Conditions		min	typ	max	Unit
Ratings						
$I_{OUT\ RATED}$	Rated output current	No overload, tamb = 30°C Chip junction T°< 150°C, (Max junction temperature = 175°C) With SEMIKRON axial fan assembly		50		A_{RMS}
V_{OUT}	Rated output voltage			400		V_{AC}
PF	Power factor			1		-
P_{OUT}	Rated output power			20		kW
f_{SW}	Inverter switching frequency			5		kHz
f_{OUT}	Output frequency			60		Hz
V_{BUS}	Rated DC voltage			750		V_{DC}
$P_{LOSS\ INV}$	Total power losses			700		W
η	Inverter efficiency			-		%

Protection & measurement					
Symbol	Conditions	min	typ	max	Unit
Thermal trip	Temperature trip level (Normally Open type: NO)		71		°C
Temperature sensing $T_{analogue\ OUT}$	Scaling over 30°C...110°C temperature range				mV/°C
	Linear temperature range	30		110	°C
	Accuracy of analogue signal over 65°C...110°C range	-1,6		1,6	°C
	Max. output current			5	mA
	Max. voltage range	0		10	V_{DC}

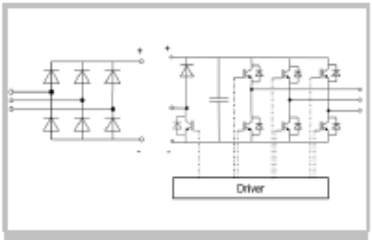
Axial fan data					
Heatsink fans	V_{SUPPLY}	Heatsink fan DC voltage supply		230	Vac
	P_{FAN}	Rated power at V_{SUPPLY} per fan, PWM 100%		16	W

Filtering characteristics					
V_{BUS}	Rated DC voltage applied to the caps bank with switching		640	700	V_{DC}
$V_{DC\ CAP}$	Max DC voltage applied to the caps bank without switching			800	V_{DC}
τ_{disch}	Discharge time of the capacitors (5%)		-		s
C_{DC}	Capacitor bank capacity		0,88	1,32	mF
LTE	Calculated LTE of the caps with forced air cooling		-		kH

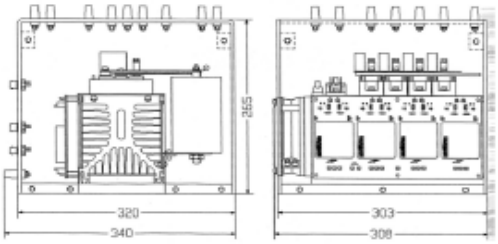
Stack insulation				
V_{INSUL}	Frame / Power stage AC/DC (insulation test voltage AC, 60s)		1 500	V

Driver Characteristics					
Symbol	Conditions	min	typ	max	Unit
Driver board data					
V_S	Supply voltage	14,4	15	15,8	V_{DC}
$I_{AP,\ IDLE}$	Supply primary current (no load)		20		mA
$I_{AP,\ LOAD}$	Max. supply primary current			290	mA
VIT+	Input threshold voltage HIGH			12,6	V_{DC}
VIT-	Input threshold voltage LOW	4,6			V_{DC}
R_{IN}	Input resistance		10		kΩ

Weight			
	3-phase IGBT inverter	13,3	kg
	3-phase IGBT inverter including fan assembly	14,9	



B6U + B6CI + E1CIKF



General dimensions