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Characterization and Testing of a 5.8 kV SiC PiN Diode for Electric Space Propulsion Applications

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CHARACTERIZATION AND TESTING OF A 5.8 KV SIC PIN DIODE FOR ELECTRIC SPACE PROPULSION APPLICATIONS

by

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Inductive Pulsed Plasma Thrusters (IPPTs) are a type of in-space propulsion that has multiple advantages over conventional chemical propulsion for long-duration, deep space missions. Existing IPPT prototypes utilize spark gap switches, however these are subject to corrosion problems that make them unreliable for long-term use. Recent advances in solid state switching technology have opened up a variety of switching options that could provide greater reliability, controllability, and increased energy efficiency. Taking advantage of this, a novel thruster drive circuit topology containing a high-power silicon controlled rectifier (SCR) and series fast recovery diode (FRD) is proposed that is expected to increase the recapture efficiency of the thruster drive circuit, defined as the percentage of energy that remains on the capacitor bank following a single discharge cycle.

A conventional Si FRD from ABB and a prototype Silicon Carbide (SiC) PiN diode from Cree, Inc. were characterized and tested as part of an IPPT solid state switching module on the Flat-Plate Thruster (FPT) developed and constructed at the National Aeronautics and Space Administration (NASA) Marshall Space Flight Center (MSFC) Electric Propulsion Thruster Development Laboratory. Preliminary analytical characterization of the devices, including static performance, dynamic (switching) performance, and thermal analysis is described, as well as the construction of the FPT thruster and the experimental setup used for thruster switching data

collection. Collected experimental data shows that the proposed drive circuit topology results in a 20% higher recapture efficiency as compared to a topology containing no series diode. In addition, the superior reverse recovery characteristics of the Cree SiC diode as compared with the ABB Si diode result in an additional gain in recapture efficiency of approximately 5% across a range of capacitor bank charge voltages.

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Nomenclature

A_i	Cross-sectional area of i^{th} layer
$\vec{B}(t)$	Time-dependent magnetic field
C_1	Capacitor bank
c_i	Specific heat capacity
C_i	Thermal capacitance
d_i	Thickness of i^{th} layer
$(di/dt)_{max}$	Maximum current rise rate
$(dv/dt)_{max}$	Maximum voltage rise rate
D	Diffusion constant
E_C	Capacitor bank energy
E_{Cf}	Final capacitor bank energy
E_{Ci}	Initial capacitor bank energy
E_{rr}	Reverse recovery energy
E_θ	Azimuthal electric filed
F_m	Mounting force
i	Term index of i^{th} layer
$i(t)$	Time-dependent current
I_{DFo}	Initial diode forward current
I_{dRM}	Peak diode reverse recovery current
I_L	Load current
I_F	Diode forward current
$\bar{I}_F$	Vector of forward currents
$I_{F(AV)}$	Average forward current
I_{FSM}	Maximum non-repetitive forward surge current
I_o	Initial load current
$\hat{I}_{sp}$	Specific impulse
k	Thermal conductivity

k_i	Thermal conductivity of i^{th} layer
k_B	Boltzmann's constant
k_o	Coupling coefficient
L_c	Acceleration coil inductance
L_{eff}	Total effective coil inductance
L_{load}	Load inductance
L_o	Stray inductance
L_s	Drive circuit stray inductance
M	Mutual inductance
η_t	Thrust efficiency
P	Power pulse amplitude
Q_f	Charge contributing to reverse recovery
Q_{rr}	Reverse recovery charge
R_i	Thermal resistance of i^{th} layer
R_{load}	Load resistance
R_s	Drive circuit stray resistance
t	Thruster pulse duration
t_1	Time of 1st current zero crossing
$\mathrm{t_{rr}}$	Diode reverse recovery time
T	Absolute Temperature
T_C	Device case temperature
T_{jf}	Device final junction temperature
T_{ji}	Device initial junction temperature
T_{jMAX}	Maximum device junction temperature
V_c	DC power supply
V_c	Capacitor charge voltage
V_{cf}	Final capacitor bank charge voltage
V_{ci}	Initial capacitor bank charge voltage

V_D	Voltage across diode
V_{DC}	Forward voltage blocked by diode
$\bar{V}_F$	Vector of forward voltage drops
V_i	Effective volume of i^{th} layer
V_{pk}	Sinusoid peak voltage
V_R	Voltage across load resistor
V_{RRM}	Maximum reverse blocking voltage
V_{rms}	Root-mean-squared voltage
z	Axial distance
z_o	Electromagnetic decoupling distance
$Z_{th(j-c)}(t)$	Junction-to-case transient thermal impedance
ΔT_j	Chance in device junction temperature
ΔT_{j-c}	Change in the device junction-to-case temperature
ΔV_c	Change in capacitor charge voltage
η_r	Recapture efficiency
$\eta_{r,ideal}$	Ideal recapture efficiency
μ_q	Carrier mobility
ρ_i	Material mass density
τ_i	Thermal time constant of i^{th} layer

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CHAPTER 1
INTRODUCTION

First demonstrated in 1964 aboard NASA's SERT-1 probe, electric propulsion stands as a reliable alternative to chemical propulsion for in-space applications such as attitude control of satellites and long-duration spaceflight. Electric propulsion systems are generally capable of providing low thrust at high specific impulse, $\hat{I}_{sp}$, in the range of thousands of seconds [1]. This allows for the highly efficient use of propellant, reducing the amount of propellant that must be stored on-board a spacecraft and freeing mass and volume for additional payload.

A variety of electric propulsion systems exist today. The operating principle of several of these will be discussed in detail in Section 1.1. The inductive pulsed plasma thruster (IPPT) has multiple advantages over other types of electric propulsion systems, and is the focus of this work. Current state-of-the-art high and medium-power IPPTs employ spark gaps or mechanical switches [2]. Recent advances in semiconductor technology have opened up a myriad of solid state switching options, including Insulated Gate Bipolar Transistors (IGBTs) and thyristors, as well as fast-switching diodes. Moreover, advances in the manufacturing of wide bandgap semiconductor devices, such as those made of silicon carbide (SiC), may make it possible to optimize certain drive topologies (discussed in Section 1.2) to recover energy in the circuit and increase the circuit efficiency.

1.1 INDUCTIVE PULSED PLASMA THRUSTERS

The majority of electric propulsion systems take advantage of electrostatic or electromagnetic forces acting on charged particles to impart a high velocity to an ionized gas [1]. The initially neutral gaseous propellant must first be ionized by energy coupled from the thruster's drive circuit. In an inductive pulsed plasma thruster (IPPT), the neutral propellant is spread uniformly

over an inductive coil using a gas injection system, after which energy stored in a capacitor bank is discharged through the coil. The rapidly changing current in the coil results in a time-dependent magnetic field, $\vec{B}(t)$, as per Maxwell-Ampère's equation. The variation of the magnetic field in turn produces an azimuthal electric field, E_θ, in the propellant, in accordance with Faraday's Law. The electric field accelerates free electrons in the gas, causing them to collide with neutral particles and liberate additional electrons, until full avalanche breakdown of the gas results in the formation of a plasma current sheet.

The current sheet serves as a secondary ring of current that establishes a flux equal and opposite to that produced by the current in the coil. The opposing currents create a repelling force that accelerates the plasma away from the coil and out of the thruster nozzle, producing thrust. A quantitative analysis of IPPT operation can be found in [1]. A schematic drawing illustrating IPPT operation is shown in Figure 1-1 [1].

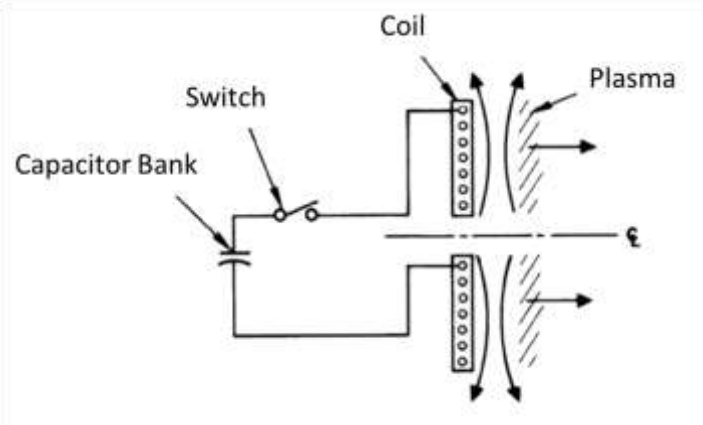


Figure 1-1. Schematic drawing illustrating IPPT operation- side view.

IPPTs have several advantages over other types of electric propulsion systems [1]. Primarily, the inductive coupling of the energy into the plasma means that the thrusters are electrodeless. This eliminates the problem of electrode erosion that exists in conventional pulsed plasma thrusters (PPTs), where metal electrodes must be in contact with the propellant. This extends the

lifetime of the thruster and allows for a wider variety of utilizable propellant gases. Additionally, the pulsed operation of IPPTs- as opposed to the steady-state operation of some types of electric propulsion systems, such as Hall thrusters- allows for a high degree of control over such thruster performance parameters as $\hat{I}_{sp}$, thrust efficiency, η_t, discharge energy per pulse, and average power level.

1.1.1 The Pulsed Inductive Thruster

The current state-of-the-art pulsed inductive thruster (PIT) is the PIT MkVa [3] (pronounced "Mark 5a" indicating design iteration 5a), the most recent iteration of a series of PITs developed at TRW Space Systems between 1965 and 1993. The basic operating principle of the PIT MkVa is the same as that described previously for IPPTs in general. The PIT MkVa consists of a spiral inductive coil mounted on a flat plate 1 m in diameter, with the total thruster mass exceeding 100 kg. A photograph of the PIT MkVa is shown in Figure 1-2 [3].

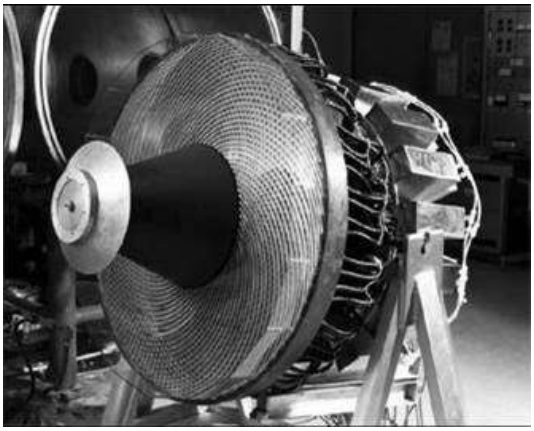


Figure 1-2. Photograph of PIT MkVa.

The PIT MkVa drive circuit uses a bank of 18 2μF capacitors to achieve a total of 4 kJ/pulse at a coil voltage of 32 kV. The pulse duration is several microseconds, and the capacitor bank is connected to the inductive coil though a parallel array of 18 spark gaps. It is important that the

firing of all spark gaps is synchronized. A single-shot test of the thruster using ammonia gas as the propellant demonstrated an $\hat{I}_{sp}$ in the range of 4000-8000 s at an η_t of 50%. The electric and performance parameters for the PIT MkVa thruster are summarized in Table 1-1 [3].

Table 1-1. Summary of PIT MkVa electrical and performance parameters.

Electrical		**Performance**	
Energy	4 kJ/pulse	Mass	>100 kg
Pulse Length	10s of μs	Diameter	1m
Coil Voltage	32 kV	η_t	50%
Average Operating Power	20 kW	I_{sp}	4000-8000 s
Capacitor Bank	9 μF	Lifetime	10^5 pulses
Switch	Spark Gap	Impulse	~ 1 N-s

1.1.2 Flat Plate Small-Scale PIT

For all iterations of the PIT thruster, spark gaps were used to discharge the high-energy capacitor bank through the inductive coil. Today, the availability of fast, high-power solid state switching devices makes it feasible to consider the use of semiconductor switches in modern IPPTs. In addition, novel pre-ionization schemes [4, 5] have led to a reduction in discharge energy per pulse for electric thrusters of this type. Pre-ionization will be discussed in greater detail below.

Solid state switches offer the advantage of greater controllability, reliability, and decreased drive circuit dimensions and mass. A potential disadvantage is the characteristic turn-on and turn-off time of the solid-state components in light of the short current rise time necessary to maximize

efficient coupling of energy into the plasma current sheet, as well as potential need to parallel devices for high-current operation.

A modular, small-scale IPPT has been designed at NASA Marshall Space Flight Center (MSFC) to serve as a flexible test-bed for solid state switching components, as well as other technologies that allow for repetitive (as opposed to single-shot) operation [2]. This variant will be referred to throughout this work as the Flat-Plate Thruster (FPT). Design specifications and a detailed description of the thruster fabrication are discussed in Chapter 4. This thruster is used as a testbed to collect switching data using several switch module configurations.

1.2 THE IPPT DRIVE CIRCUIT

At present, these types of IPPTs have an η_t around 50%, defined as the energy coupled into the propellant with respect to the initial energy stored in the capacitor [1]. Energy loss occurs in the coupling of the energy from the inductive coil into the plasma current sheet, as well as in the drive circuit. The drive circuit for an IPPT consists of a capacitor bank that is connected to the inductive coil through some type of switch. In its simplest form, the IPPT circuit can be modeled as a series resistance, R_s, inductance, L_c, and capacitance, C_1, i.e., an *RLC* circuit (Figure 1-3). In practice, additional stray inductance is also present.

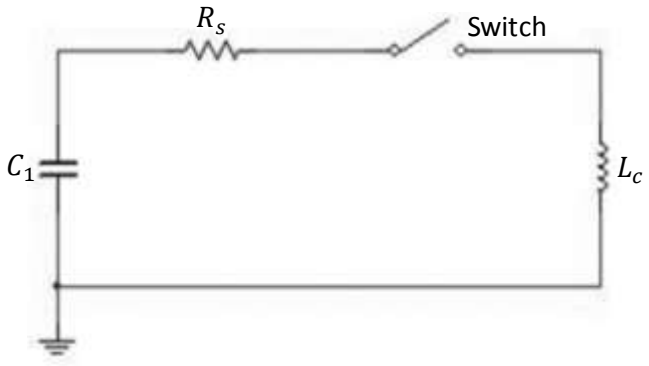


Figure 1-3. Series *RLC* circuit representing a basic IPPT circuit.

1.2.1 Diode-Clamped IPPT Circuit Topology

It has been previously shown [5, 6, 7] that the most efficient coupling of energy into the plasma current sheet of a pulsed inducted thruster occurs during the first current half-cycle of the capacitor discharge, when the coil current and current rise rate are maximum. After this time, the current sheet is largely decoupled from the inductive coil, and the remaining energy oscillates in the drive circuit and is dissipated as heat. For this reason, it is desirable to cut off- or clamp-current flow in the circuit at the first current zero crossing. This can be achieved by placing a fast recovery diode (FRD) in series with the solid state switch, as shown in Figure 1-4.

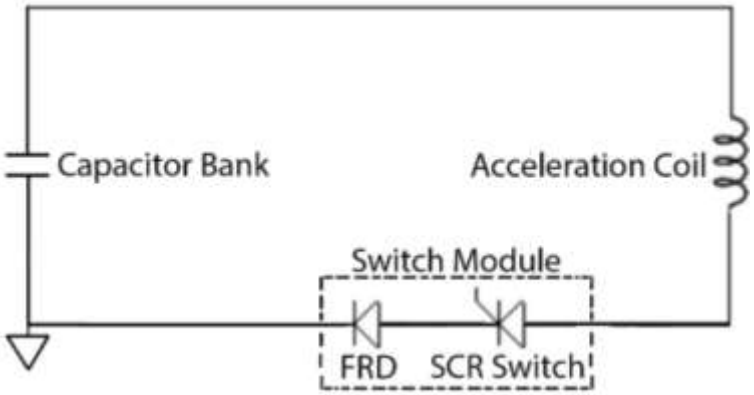


Figure 1-4. Diode-clamped IPPT circuit topology.

For this application, the main switch is chosen to be an asymmetric (blocks voltage in the forward direction only) silicone controlled rectifier (SCR), due to the controllability and high-power handling capability of this type of device. The asymmetric design of the SCR provides maximum voltage blocking capability while keeping the forward conduction power losses to as minimum. Depending on the power level of the particular IPPT, a different type of power semiconductor switch could be used, such as an Integrated Gate-Commutated Thyristors (IGCT), IGBT, or Metal Oxide Field Effect Transistor (MOSFET).

For an ideal SCR and diode, current cut-off would occur when the voltage polarity in the circuit reverses, thereby reverse biasing the diode and causing it to turn-off and block all current flow. This precludes energy oscillation in the circuit, so that a portion of the initial capacitor bank energy remains on the capacitor following a discharge cycle and may be applied toward a subsequent pulse. The percentage of the initial energy that remains is defined as the circuit recapture efficiency, η_r, and is used throughout this work to quantify circuit efficiency.

In practice, the diode reverse recovery time introduces a delay in turn-off and additional energy losses. These losses can be minimized by selecting a diode with the shortest possible reverse recovery time. In addition to increasing energy efficiency, the diode-clamped topology should also prevent excess heat generation and voltage reversal on either capacitor bank, thereby increasing component lifetime. This is of particular importance for long-duration space missions such as a Martian mission, which would require the capacitor bank to withstand up to 10^9 discharge cycles [1].

1.3 ADVANTAGES OF SILICON CARBIDE DEVICES

Silicon Carbide (SiC) is a wide bandgap material that can be used to construct semiconductor devices. For high-power and fast switching applications, SiC devices offer significant advantages to conventional Si transistors, thyristors, and diodes. The wider bandgap results in a breakdown voltage 10 times higher than that of Si [8], making it an ideal material for high voltage applications. This also means that a SiC device can be built with a thinner drift region to block a given voltage. This leads to a reduction in device size, and thereby a reduction in system size and weight. The polytype of SiC used in power device manufacturing is 4H-SiC. A summary of several important 4H-SiC and Si material properties are given in Table 1-2 [8].

Table 1-2. Summary of Si and SiC material properties.

Material	Bandgap Energy, eV	Thermal Conductivity, $Wcm^{-1}{}^{\circ}C^{-1}$	Breakdown Electric Field, Vcm^{-1}
Si	1.1	1.3	1.0e7
4H-SiC	3.26	3.7	2.0e7

In addition, the non-linearity of the relation between the drift region thickness and breakdown voltage allows for much thinner drift regions in wide bandgap devices, resulting in lower conduction voltage drop [8] and less time needed for reverse recovery due to a lower volume of excess charge carriers. SiC also has a high thermal conductivity as compared to other semiconductor materials, and can therefore operate at higher temperatures. Due to the wider bandgap, SiC devices will have lower leakage current at high temperatures than their Si counterparts. The material's greater ability to conduct heat can eliminate the need for heat sinks in some applications, thereby further reducing the size and weight of the system. SiC diodes are known to have shorter reverse recovery times and lower peak reverse recovery currents [9, 10, 11, 12] than similarly rated Si diodes, making them desirable for pulsed applications.

Several varieties of power diodes are available, each with its own advantages. PiN diodes have a lightly doped, near intrinsic region between the emitter and collector regions that make this type of power diode ideal for high voltage hold-off, however the high resistance of the drift region leads to higher conduction losses and slower switching times. As compared to conventional Si PiN diodes, the thinner drift region of the SiC PiN allows it to have a shorter reverse recovery time for the same rated blocking voltage. SiC Schottky diodes have virtually zero reverse recovery time and so may seem ideal for IPPT applications in this regard, however these devices have a relatively limited reverse voltage blocking capability [13], and so cannot be used at the voltage levels seen in typical IPPTs.

A variety of SiC power semiconductor devices are commercially available at this time and are becoming widely used for a variety of applications. Current disadvantages of SiC devices include the higher cost relative to conventional Si devices, as well as reliability issues due to the fact that manufacturing processes are still relatively new and it is difficult to grow large, defect-free wafers. Luckily, much research is currently being done on the development of SiC power semiconductor devices, and it is hoped that better manufacturing processes will soon lead to greater reliability and lower cost [14]. In light of the advantages discussed, it is proposed that replacing Si diodes with SiC diodes in the drive circuit topology of Figure 1-4 will further increase circuit efficiency and reduce stress on the capacitors and main switch, further extending component lifetime for long-duration space flight.

1.4 THESIS SCOPE AND OUTLINE

The motivation of this thesis is to investigate the use of a diode-clamped IPPT circuit topology, as well as possible advantages of using a SiC FRD in the circuit versus a conventional Si FRD. The different circuit topologies tested are compared on the basis of η_r to determine the configuration that minimizes circuit losses. This is approached in three ways:

- Through the characterization of a newly developed 5.8 kV SiC PiN diode from Cree, Inc. to determine current handling capability, reverse recovery response, on-state performance, and high-current performance. A comparison is made with a similarly-rated Si diode.
- Through a Simulink model of the IPPT drive circuit that is used to define a baseline for η_r in the ideal case.
- Through actual testing of the SiC diodes in a testbed IPPT at NASA-MSFC. Thruster fabrication is described, and experimental waveforms presented for a circuit

configuration with no series diode, a conventional Si fast-switching diode, and the prototype SiC PiN diode that is the focus of this work.

The next chapter will discuss the characterization of the Cree SiC power diode. This includes a preliminary thermal analysis that provides an estimate of the device current handling capability under conditions specific to IPPT circuits, static characterization that investigates on-state diode behavior, and dynamic characterization that investigates diode switching behavior. Chapter 3 presents a Simulink© model of the IPPT drive circuit and defines a maximum recapture efficiency, $\eta_{r,ideal}$, for an ideal, lossless circuit. Chapter 4 describes the experimental setup and test article fabrication for the FPT solid state switching proof-of-concept experiment. Data and observations from this experiment are presented in Chapter 5. Finally, conclusions regarding the performance of the diode-clamped circuit topology and the suitability of SiC power diodes for use in IPPT circuits are discussed in Chapter 6.

CHAPTER 2
DEVICE CHARACTERIZATION

Static and dynamic characterization was carried out on a prototype 5.8 kV SiC PiN diode from Cree, Inc. (Figure 2-1a) to investigate conduction and switching behavior, respectively. The results were compared with those for a 5.5 kV 5SDF 02D6004 fast switching diode from ABB (Figure 2-1b). The ABB diode is in a ceramic compression ("hockey puck") package and is mounted in a Wakefield clamp with a compressive force of approximately 16 kN. Prior to testing, thermal analysis was carried out in order to predict current handling capability for each device under conditions specific to our application.

Figure 2-1. Si and SiC test diodes. a) 5.8 kV SiC PiN diode from Cree, Inc. b) 5.5 kV Si fast diode from ABB Semiconductors.

2.1 THERMAL ANALYSIS

Thermal analysis was carried out on both diodes in order to estimate the maximum current density each could support for a pulse of 10 µs duration without experiencing permanent damage. Typically, power device datasheets provide maximum average on-state current ratings under the condition of a half sine wave at a frequency of 50 Hz, and maximum peak non-repetitive surge

current ratings under the condition of a 10 ms duration current pulse. The current magnitude is limited by the amount of heating incurred in the material. Excessive heating will cause irreversible damage to the semiconductor substrate, leading to device failure. For a short duration pulse (on the order of μs), there is little time for heating of the substrate to occur, so that a device can handle a high current for short duration with no damage.

The amount of time that heat from a current pulse remains in the die depends on the material properties of the die and device packaging. A material's thermal conductivity, k, is a measure of how well it conducts heat. Materials with high thermal conductivity (low thermal resistivity) will dissipate heat more rapidly than those with low thermal conductivity (high thermal resistivity). This reduces the amount of time that heat from a current pulse remains within the device die, and decreases the likelihood of device damage.

The thermal analysis carried out provides an estimate of the rise in the device junction temperature with respect to ambient, or case, temperature (denoted by ΔT_{j-c}) for a current pulse of a given magnitude. This is done by considering the thermal properties of the device material and packaging. One basic approach to this analysis entails using the datasheet provided by the manufacturer to calculate conduction power loss in the device from the given voltage-current (V-I) characteristic curve. One may then refer to the thermal impedance curve (and/or analytical function) provided therein to calculate the device final junction temperature, T_{jf}, following a current pulse of given duration. This calculation can be repeated over a range of forward currents, resulting in a plot of final junction temperature as a function of forward current pulse magnitude.

The above approach was followed as written for the ABB Si device, however, the unavailability of a datasheet for the prototype SiC diode necessitates a modified approach. In this case, the V-I characteristic of the diode was estimated using the datasheet from a commercially available SiC diode of comparable die area. A Cauer equivalent RC thermal network [15] was

then developed to model the thermal impedance of the prototype SiC diode's unique packaging. This approach is discussed in detail in the following section.

2.1.1 Diode RC Network Thermal Modeling

The prototype SiC diode die area is estimated to be approximately 0.36 cm^2. Assuming that the maximum allowable average current density of SiC is between 50 and 100 A/cm^2, the forward current rating of the diode is estimated to be between 18 A and 36 A. A commercially available Cree SiC Schottky diode (part number C4D20120A) with a forward current rating of 25.5 A and a reverse blocking voltage of 1.2 kV was chosen as a device of comparable die area. It should be noted that the SiC Schottky diode forward voltage drop will underestimate the forward voltage drop for a SiC PiN diode [13]. No Cree SiC PiN diodes are currently commercially available. For this reason, some margin must be added to the maximum current rating estimated using this approach.

The C4D20120A datasheet provides a series of V-I characteristic curves at ambient temperatures of -55, 25, 75, 125, and 175°C (Figure 2-2a). The linear portion of the 25°C curve was extended to a forward current of 10 kA using a linear extrapolation in MATLAB (Figure 2-2b). Using the extrapolated V-I curve, the on-state device power dissipation was calculated for a range of zero to 10 kA. For a pulse of short duration (generally < 1 s), the transient thermal impedance, $Z_{th(j-c)}(t)$, is used to calculate the device junction-to-case temperature as a function of an applied heat power pulse. The quantity is defined as follows:

$$\boldsymbol{Z_{th(j-c)}(t) = \frac{T_{jMAX} - T_c}{P} = \frac{\Delta T_{jc}}{P}} \tag{2-1}$$

where t is pulse duration, P is the pulse power amplitude, T_{jMAX} is the maximum junction temperature flowing the pulse, and T_C is the device case temperature. The transient nature of the

heating is captured by the thermal time constant, τ_i, where the subscript i is a term index. When the Cauer equivalent RC network thermal model is used, the term index refers to the physical layer of material in the device substrate or packaging, however this is not always the case [15].

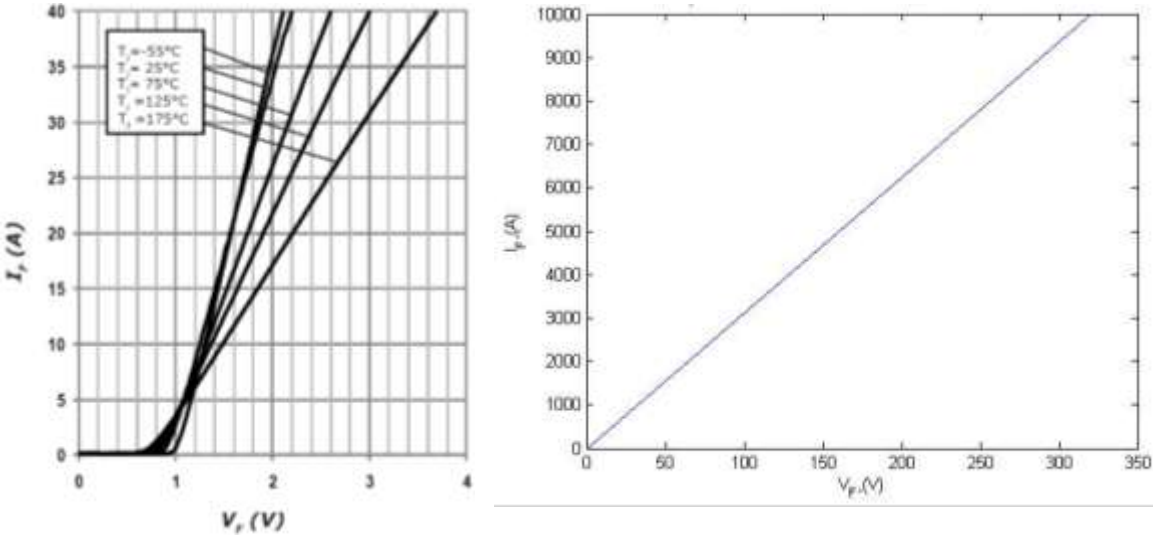


Figure 2-2. V-I characteristic curves for Cree C4D20120A SiC diode. a) Manufacturer-provided V-I curves. b) Curve at 25 °C extrapolated to a current of 100 kA.

The thermal time constant is defined as

$$\tau_i = R_i C_i \tag{2-2}$$

where R_i is thermal resistance of the physical layer and C_i is its thermal capacitance. These parameters can be calculated using material thermal properties and geometry as follows:

$$R_i = \frac{d_i}{k_i A_i} \tag{2-3}$$

where d_i is the layer thickness, A_i is the layer cross-sectional area , k_i is the thermal conductivity of the material of which the layer is composed. Similarly,

$$C_i = c_i \rho_i V_i \tag{2-4}$$

where c_i is the specific heat capacity of the material in the layer, ρ_i is the material's mass density, and V_i is the layer's effective volume. The prototype SiC PiN diode packaging leaves the die visible from the top through a layer of transparent silicone caulk. The high thermal resistivity of this material makes this a high impedance path for heat moving between the die and the device case. For this reason, it is assumed that no heat flows out across this material.

A schematic cross-sectional view of the SiC diode is shown in Figure 2-3 (not to scale). The SiC die is thermally and electrically connected to the copper (Cu) baseplate by a thin layer of solder. The baseplate serves as both the diode cathode and a heat sink for a majority of the heat generated in the die. An alternative path for heat dissipation is through two separate groups of aluminum (Al) wirebonds that connect from two edges of the die to two separate Cu tabs that both serve as the diode's anode. Photographs of the diode cross-section are shown in Figure 2-4a, Figure 2-4b, and Figure 2-4c.

The relevant thermal and geometrical parameters for the heat-conducting material layers (SiC, solder, Cu, and Al) are given in Table 2-1. The symmetry of the package is used to simply the thermal model to reflect heat generation and flow in just one half of the device. It should be noted that the thermal conductivity and heat capacity of each layer is given at an ambient temperature of 25°C [16] and that the temperature dependence of these parameters is not included in the model.

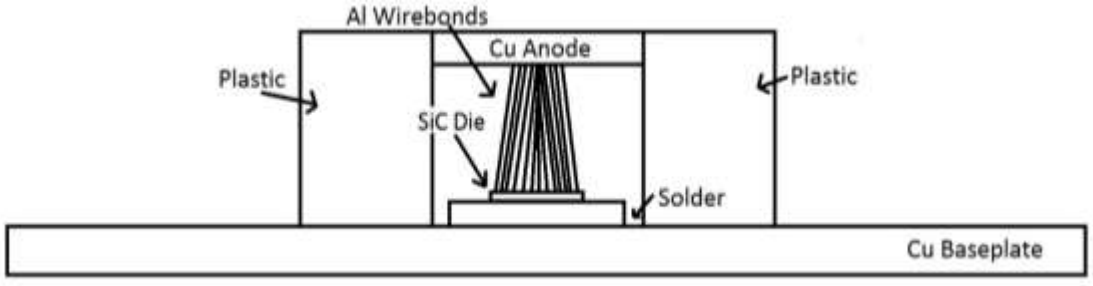
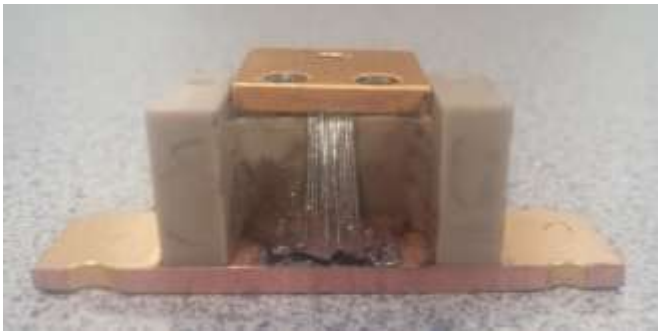
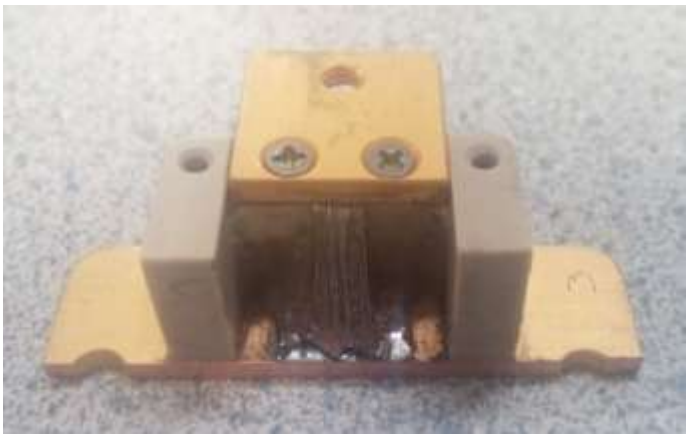


Figure 2-3. Schematic representation of Cree SiC diode cross-section.



(a)



(b)

(c)

Figure 2-4. Photographs of Cree SiC diode cross-section. a) The die and substrate layers are visible beneath the wirebonds. b) Alternate view. c) With the die and substrate layers removed, a thin layer of solder can be seen. This is used to connect the substrate to the Cu baseplate.

Table 2-1. Thermal and geometrical parameters of prototype SiC diode material layers for half of a device.

Material Layer	**Thickness (m)**	**Area (m^2)**	**Volume (m^3)**	**Density (g/m^2)**	**Specific Heat (J/g/℃)**	**Thermal Conductivity (W/m/℃)**
Silicon Carbide	1.5×10^{-4}	1.8×10^{-5}	2.7×10^{-9}	3.2×10^{6}	0.753	370
Solder	1.0×10^{-4}	4.2×10^{-6}	4.2×10^{-10}	9.7×10^{6}	0.130	38
Copper Cathode	2.3×10^{-3}	6.3×10^{-4}	1.5×10^{-6}	8.9×10^{6}	0.385	400
Aluminum Wirebonds	2.5×10^{-4}	3.9×10^{-5}	9.9×10^{-9}	2.7×10^{6}	0.900	205
Copper Anode	2.3×10^{-3}	2.6×10^{-4}	6.0×10^{-7}	8.9×10^{6}	0.385	400

For the SiC PiN diode, the thermal resistance, specific heat capacity, and thermal time constant for each physical layer, calculated using Equation 2-2, Equation 2-3, and Equation 2-4, are given in Table 2-2. The transient thermal model for half the device is represented by a Cauer equivalent RC thermal network (Figure 2-5). Here, the input current source represents the heat generated within the device die as a result of the power pulse applied. Each node has an associated temperature, and heat flows from high to low temperature wherever a temperature gradient exists across a layer.

In terms of the thermal resistivity and heat capacity parameters, the device transient thermal impedance can be described analytically as follows:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i (1 - e^{-t/\tau_i}) \tag{2-5}$$

where all variables are previously defined. The transient thermal impedance for a 10 µs pulse, $Z_{th(j-c)}(10\ \mu s)$, is calculated to be 0.0736 ℃/W. The change in junction temperature, ΔT_j, is found by multiplying $Z_{th(j-c)}(10\ \mu s)$ by a vector of power values (in Watts), calculated as

Table 2-1. Summary of Si and SiC material properties

Layer Index	***Material Layer***	R_i, ℃/W	C_i, J/℃	τ_i, s
$i = 1$	Silicon Carbide	0.0225	0.0065	0.0001
$i = 2$	Solder	0.6192	0.0005	0.0003
$i = 3$	Copper Cathode	0.0091	4.9819	0.0453
$i = 4$	Aluminum Wirebonds	0.0319	0.0239	0.0008
$i = 5$	Copper Anode	0.0220	2.0576	0.0453

$I_F * V_F$, where I_F is a vector of current values between zero and 10 kA, in steps of 1 A, and V_F is the forward voltage drop during conduction. Lastly, the device final junction temperature, T_{jf}, is found by adding ΔT_j to an initial junction temperature, T_{ji}, of 25 °C.

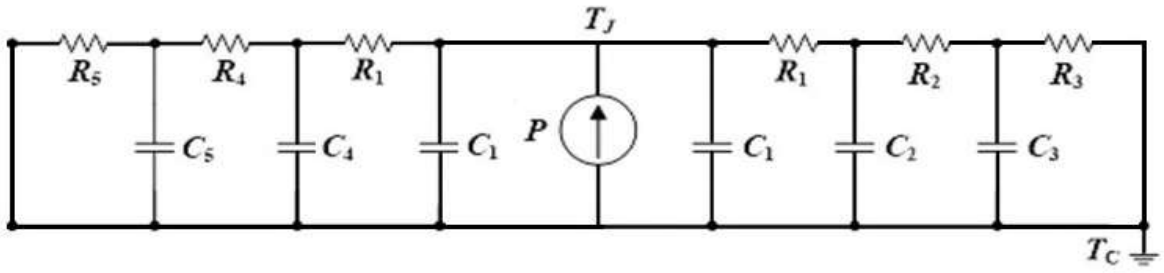


Figure 2-5. Cauer equivalent RC thermal network model for prototype Cree SiC diode.

The availability of a datasheet for the commercial ABB Si diode eliminates the need to develop a RC thermal network model of the device, as thermal resistance and thermal time constant values are provided for a 4th-order behavioral model. The extrapolated V-I characteristic curve for the device is shown in Figure 2-6a, and the transient thermal impedance curve provided in the datasheet appears in Figure 2-6b. It should be noted that the VI curve is for a junction temperature of 115°C, so that the extrapolated forward voltage drop will over-estimate the

voltage drop at room temperature (25°C). The values of R_i and τ_i for $i = 1, 2, 3, 4$ are given in Table 2-3 [17]. In this case, the index, i, does not represent a physical layer of material. For the ABB Si diode, the transient thermal impedance for a 10 µs pulse, $Z_{th(j-c)}(10\ \mu s)$, is calculated to be 1.64×10^{-6} ℃/W.

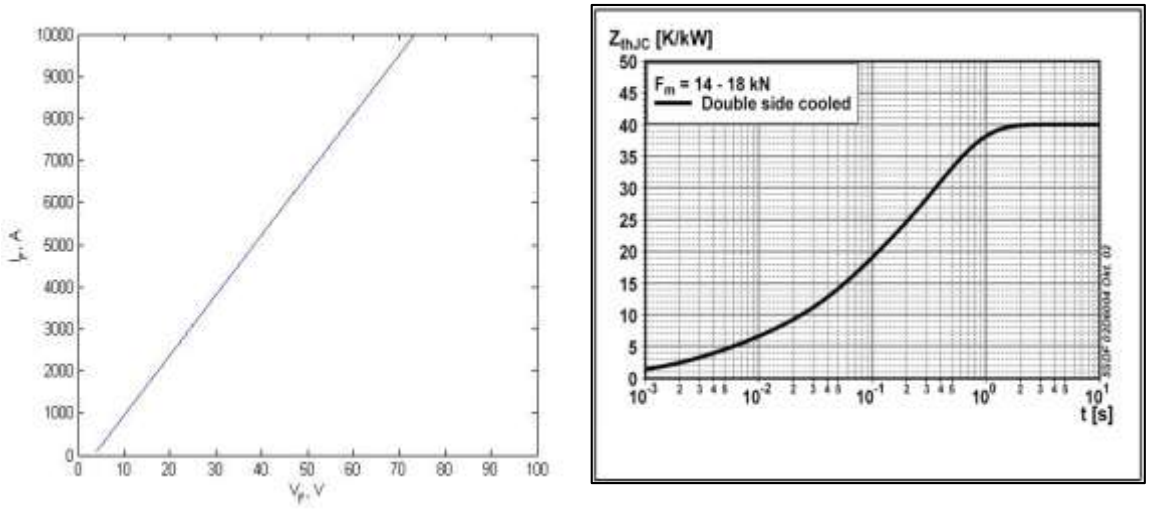


Figure 2-6. Si diode data used in thermal calculation. a) A V-I characteristic curve extrapolated to a current of 10 kA. b) Transient thermal impedance curve provide in diode

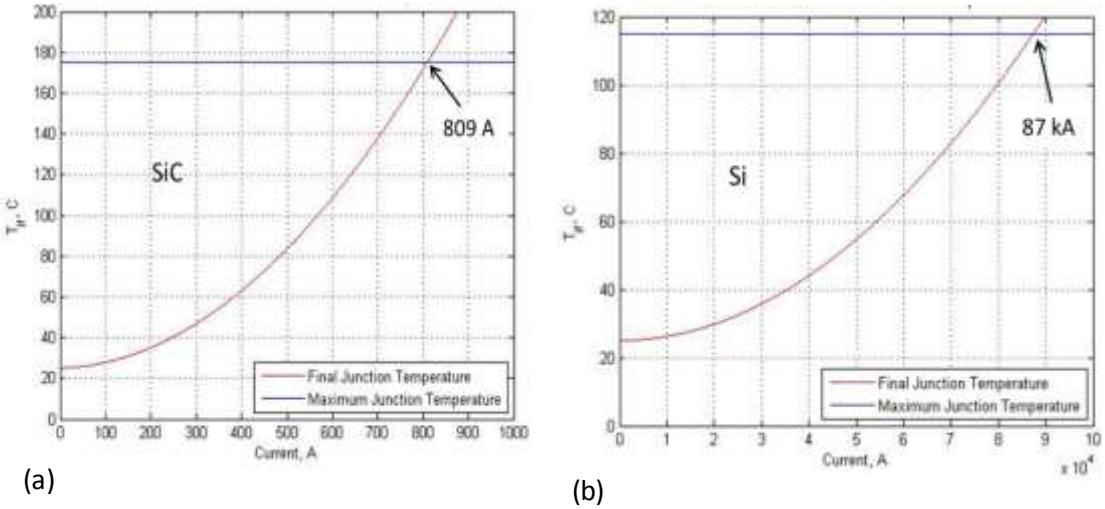
Table 2-3. Layer Thermal resistances time constants provided in Si diode datasheet.

i	**1**	**2**	**3**	**4**
$\boldsymbol{R_i}$, $^{\circ C}/_{\boldsymbol{W}}$	.025699	.009472	.003381	.001466
$\boldsymbol{\tau_i}$, **s**	0.3802	0.0483	0.0060	0.0018

2.1.2 Thermal Analysis Results and Discussion

Calculated final junction temperature, T_{jf}, as a function of forward current pulse magnitude is shown in Figure 2-7a for the prototype Cree SiC PiN diode and in Figure 2-7b for the ABB Si diode. The horizontal line in each figure indicates the maximum rated operating junction

temperature for each diode. For a SiC power diode, this value is 175°C, while for the Si diode is 115°C. A From the figure, the estimated maximum allowable current for a 10 □s pulse is defined as the value of the current pulse magnitude at which the junction temperature curve for the diode reaches its maximum rated operating junction temperature, i.e., the point where the curve crosses the horizontal line. For the Si diode, this is determined to be approximately 87 kA, while for the SiC diode it is determined to be approximately 809 A. These numbers provide order-or-magnitude estimates and are not regarded as being exact.



(a) (b)

Figure 2-7. Device final junction temperature as a function of current. a) Cree SiC diode. b) ABB Si diode.

In order to obtain a meaningful comparison between the maximum current ratings of the two devices, the maximum current rating of each diode is divided by the die area to estimate the maximum current density. For the SiC diode, this is found to be approximately $4.5 \times 10^3\ A/cm^2$ while for the Si diode it is $5.2 \times 10^3\ A/cm^2$. The comparable maximum current densities for the two diodes suggest that the SiC diode can operate at similar junction temperature as the Si diode with less packaging and a smaller heatsink, or no heatsink. This would allow for a

reduction in size and mass of the systems in which the device is used, and is a considerable advantage for spacecraft applications.

The results of the thermal analysis confirm that a shorter pulse duration allows the maximum surge current rating of a device to be considerably extended from that provided in a typical data sheet. For example, the maximum peak non-repetitive surge current rating (10 ms pulse) for the ABB 5SDF 02D6004 of 3 kA can potentially be exceeded to 10s of kA, without causing damage to the device, for very short pulses of a few μs duration. In particular, the analysis highlights the effect of packaging on device high-temperature operation and current handling. Although SiC has a greater thermal conductivity than Si, (3.7 $W cm^{-1} °C^{-1}$ versus 1.3 $W cm^{-1} °C^{-1}$) the device packaging is the limiting factor in how quickly heat can be removed from the SiC die. It is reasonable to conclude that the significantly higher current handling capability determined for the ABB Si diode is primarily the result of an active area that is 15 to 20 times larger than that of the SiC device, and of less importance, the use of double-side cooling for the Si compression package as compared to single-side cooling (primarily through the Cu baseplate) available in the prototype Cree SiC device.

While the thermal analysis results provide an initial estimated current rating for the SiC diode, in practice other factors may reduce the actual magnitude of forward current at which the device can be used. A prime example of this is observed in the following section, when SiC material defects manifest themselves in unpredictable medium-current behavior.

2.2 STATIC CHARACTERIZATION

Static characterization of the prototype Cree SiC PiN diode involves the generation of V-I characteristic curves for both low (0 to 5.25 A) and medium current (100-500 A). The temperature dependence of the forward voltage drop is also investigated, and all data is compared

to that for the ABB Si diode. The results are discussed in terms of device physics and material properties.

2.2.1 Low Current V-I Curves

Low current V-I curves for both diodes are generated using a Keithley Model 2440 SourceMeter (Figure 2-8). The SourceMeter is programmed and data collected using a LabVIEW©-based interface provided with the Keithley product. The output current is limited to 5.25 A. A Sun Electronic Systems thermal chamber (Figure 2-9) is used to heat or cool the device under test (DUT), which in this case is the Si or SiC diode. The chamber is programmed manually from the front control panel to maintain each desired ambient temperature for 40 minutes, which allows the die temperature to stabilize before data is taken.

Figure 2-8. Keithley Model 2440 SourceMeter front panel.

Figure 2-9. Sun Electronic Systems thermal chamber used to heat or cool device under test to the desired temperature.

The low current temperature-dependent V-I characteristic curves for the SiC and Si diodes are shown in Figure 2-10. Each set of data was averaged over separate datasets taken for two ABB 5SDF 02D6004 Si diodes and two prototype Cree SiC PiN diodes. Measurements were taken at -25°C, 25°C, 75°C, 125°C, and 175°C. No data was taken for the Si diode at 175°C, so as not to exceed the 115°C rated maximum junction temperature. It can be seen from Figure 2-10 that the SiC device has a higher turn-on voltage at each temperature than the Si devices. This is primarily a result of the charge carrier lifetime being lower in SiC than in Si, due to more efficient SRH-type carrier recombination in the SiC. In addition, the turn-on voltage for each device decreases with increasing temperature due to the carrier lifetime increase with temperature [18].

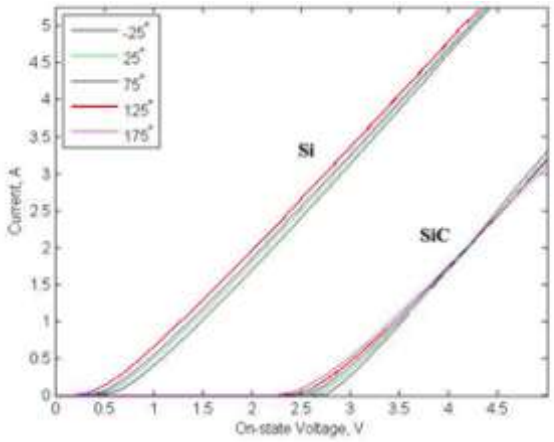


Figure 2-10. Temperature Dependence of Si and SiC low current V-I Characteristic.

A prominent feature of Figure 2-10 is the cross-over of the SiC V-I curves an on-state voltage of just over 4 V. This is caused by a three competing physical phenomena [19]:

1. An increase in minority carrier lifetime
2. A decrease in carrier bulk mobility due to increased lattice vibrations
3. Secondary effects, including surface energy states, that can affect carrier mobility

It is reasonable to predict that a similar cross-over occurs with the Si V-I curves at some higher on-state voltage. This is in agreement with the trend one would expect to see in the V-I curves at higher temperatures- namely, that the on-state voltage drop for a given diode increases with increases temperature. This is true because of the decreased carrier mobility that results from the increasing drift region resistance at higher temperatures. This behavior is in fact observed for the Si diode V-I curves at high forward current, as will be discussed in the following section.

2.2.2 Medium Current V-I Curves

In order to construct diode V-I characteristic curves at higher forward currents – 100 A, 200 A, 300 A, and 400 A- the circuit shown schematically in Figure 2-11a was used to simultaneously measure the current through and voltage across the diode under test. The physical setup of the circuit is shown in Figure 2-11b.

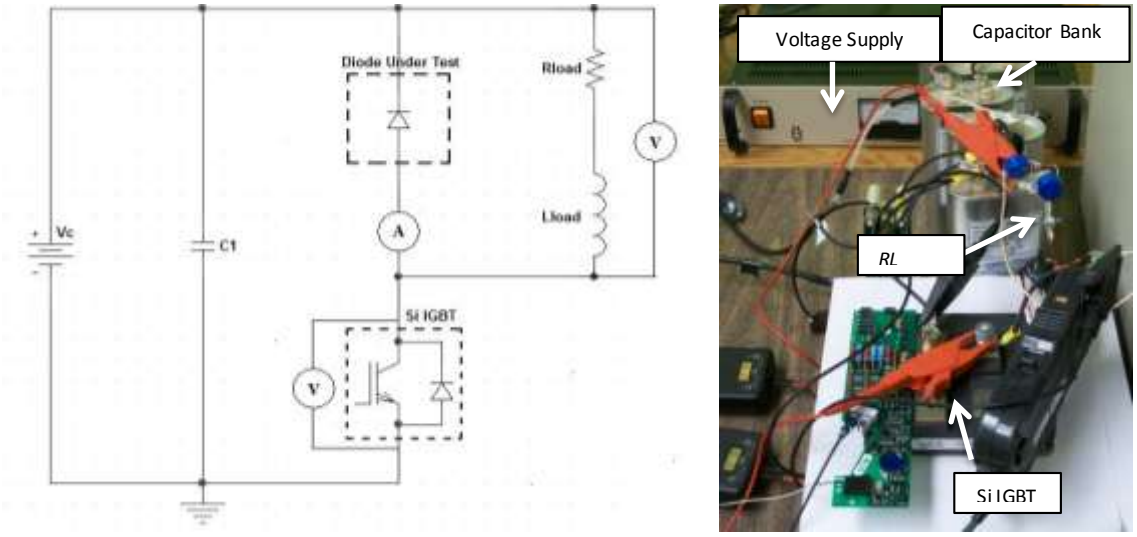


Figure 2-11. Circuit and setup used for medium current static characterization. a) Schematic representation of circuit. b) Physical setup of the circuit.

Component C_1 in Figure 2-12a represents a bank of five 10 µF Maxwell capacitors that is charged using a Glassman High Voltage Series EL DC power supply, represented by

component V_c. The series inductance of C_1 is approximately 450 nH. The total capacitance is chosen to be as large as possible (limited by the number of available capacitors) in order to ensure that the current does not change by more than 1% during a single 10 µs pulse. The trigger pulse is generated using a Berkeley Nucleonics Corporation (BNC) pulse generator, and fiber optically coupled to a Mitsubishi 1.7 kV Si IGBT. When the IGBT is triggered, it provides a discharge current path for the capacitor bank through the resistor-inductor (*RL*) load.

Component L_{load} is an air-core inductor with a value of 166 µH, and the load resistance, R_{load}, has a value of 2 Ω. The charge voltage V_1 is varied to control the load current. While the IGBT is conducting, current flowing through the circuit charges the load inductor. When the IGBT is subsequently turned off, the diode under test becomes forward biased by the induced voltage across L_{load} and acts as a freewheeling diode, providing a current path for the inductor to discharge. This allows a relatively steady current to be measured through the diode, and also makes it possible to control the diode forward current by charging the inductor over several pulses.

Current through the diode is measured using a Pearson coil current transducer. The diode voltage and voltage across the IGBT are measured using two 5 kV differential probes. Since the diode reverse voltage is much larger than the conduction voltage, the oscilloscope does not have enough bit precision to accurately measure the conduction voltage over the dynamic switching range of the voltage. The measurement is therefore taken across the *RL* load in parallel with the diode under test. Current and voltage measurement locations are indicated in Figure 2-11a.

A single pulse discharge test was conducted at -25 °C, 25 °C, 75 °C, and 125 °C. Diode current and voltage were measured at load currents, I_L, of 100 A, 200 A, 300 A, and 400 A, at each temperature. The diode under test is enclosed in the Sun Electronic Systems thermal chamber described in Section 2.2.1. As before, the chamber is programmed to maintain each

desired ambient temperature for 40 minutes so that the die temperature may stabilize before data is taken. Data is collected using a LeCroy Waverunner 104MXi-A 1 GHz Oscilloscope capable of taking up to 10 gigasamples per second (GS/s). The laboratory test setup is shown in Figure 2-12.

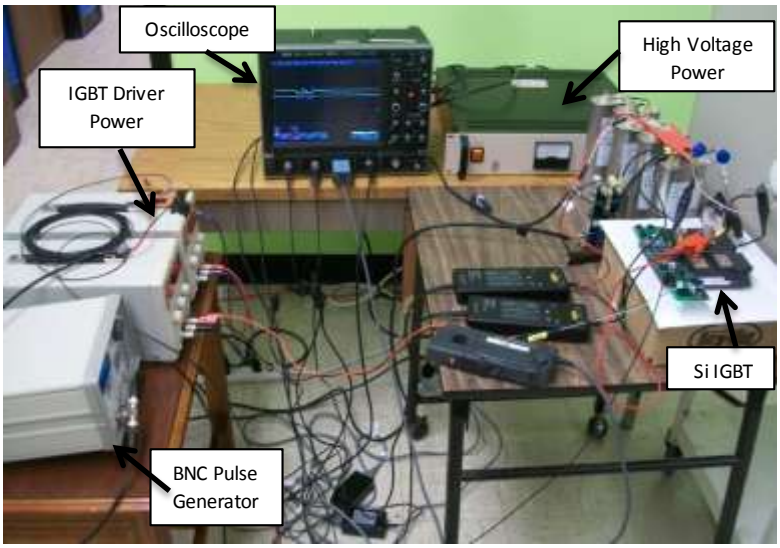


Figure 2-12. Photograph of medium current static characterization test laboratory setup.

Data collected for both the 5.5 kV Si fast diode and 5.8 kV SiC PiN diode are shown in Figure 2-13a and Figure 2-13b. A line-of-best-fit is added to the each set of data points at each temperature. These lines approximate the diode V-I characteristic curves and can theoretically be used to predict conduction losses at any forward current. As expected, both sets of data show a positive linear correlation between diode forward voltage drop and forward current at high current values (high current density). At high current densities, the injected excess carrier concentration is so large that the device tends to look resistive so that the carrier mobility dominates the forward conduction behavior.

As the temperature increases, the mobility drops thus causing an increase in the forward voltage drop. The data for the Si diode in Figure 2-12a follows this behavior as described in (2-1).

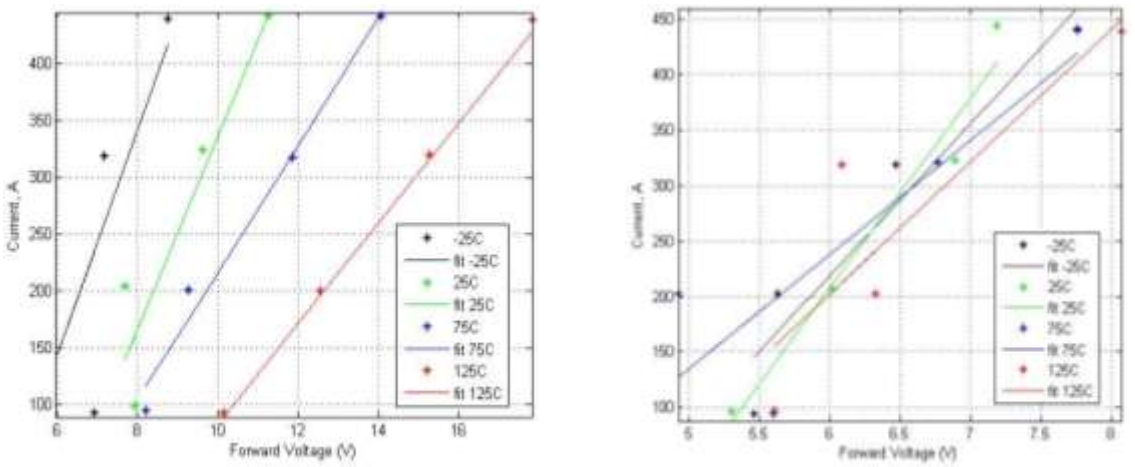


Figure 2-13. Medium current V-I characteristic data with trend lines for a) Si diode and b) SiC diode.

$$\mu_q = \frac{Dq}{k_B T} \tag{2-1}$$

where μ_q is the mobility of a charged particle, D is the diffusion constant, k_B is Boltzmann's constant, and T is the absolute temperature. Reduced mobility in term leads to higher drift layer resistivity and hence higher forward voltage drop.

While the temperature dependence and positive linear correlation between the Si diode forward voltage and current is as expected, it must be noted that, in each case, the observed forward voltage drop is higher than that predicted by the ABB 5SDF 02D6004 diode datasheet. Although the voltage measurements were taken after 100 □s into the conduction cycle, it is possible that under the experimental conditions, the diode voltage had not yet reached steady-state at the time of measurement. In addition the self-heating during the conduction cycle would have resulted in a higher junction temperature than the ambient and hence caused an additional increase in the forward voltage drop not accounted for in a direct comparison to voltage values expected from the datasheet.

While the medium-current V-I data for the SiC diode (Figure 2-14b) does show a positive correlation between the forward voltage and current, the temperature trend is not clearly defined. This can be attributed to material defects inherent from the relatively immature manufacturing processes of SiC devices [20, 21, 22]. This data suggests that these particular devices (prototype 5.5 kV SiC PiN diodes from Cree, Inc.) may not operate nominally at high currents (above 100 A). Since PIT switching applications require the devices to operate at peak current levels of several thousands of amps, it is hoped that current and future advances in SiC device manufacturing will improve material purity and make devices capable of efficient high current operation.

2.3 DYNAMIC CHARACTERIZATION

Dynamic characterization of the SiC devices is carried out using a double-pulse test circuit to observe the reverse recovery response of the diodes for varying ambient temperature and load current. These waveforms are compared with those for the Si fast diode and the total reverse recovery energy is tabulated for each case. The collected data allows for the prediction of reverse recovery losses at a variety of diode forward currents, as well as the extraction of diode parameters for use device modeling (beyond the scope of this work).

2.3.1 Experimental Setup

A schematic of the double-pulse test circuit is shown in Figure 2-14a. This circuit is used to look at the diode reverse recovery as follows: Two pulses, each of duration 10 μs and an equivalent period of 20μs (if operating in steady state), are applied to a Mitsubishi 1.7 kV Si IGBT via a fiber optic link. When the IGBT is conducting, current flows through the resistive-inductive (*RL*) load and charges the inductor. When the IGBT is subsequently turned off, the

current from the inductor must flow through the diode (DUT). The physical laboratory setup for the circuit is shown in Figure 2-14b. During the second pulse, the IGBT once again conducts, and the diode becomes reverse-biased. The diode experience a reverse recovery current as a result of the time it takes for the stored charge in the intrinsic region of the PiN power diode to be removed. The duration of this process depends both on the properties of the external circuit and the device material properties [23].

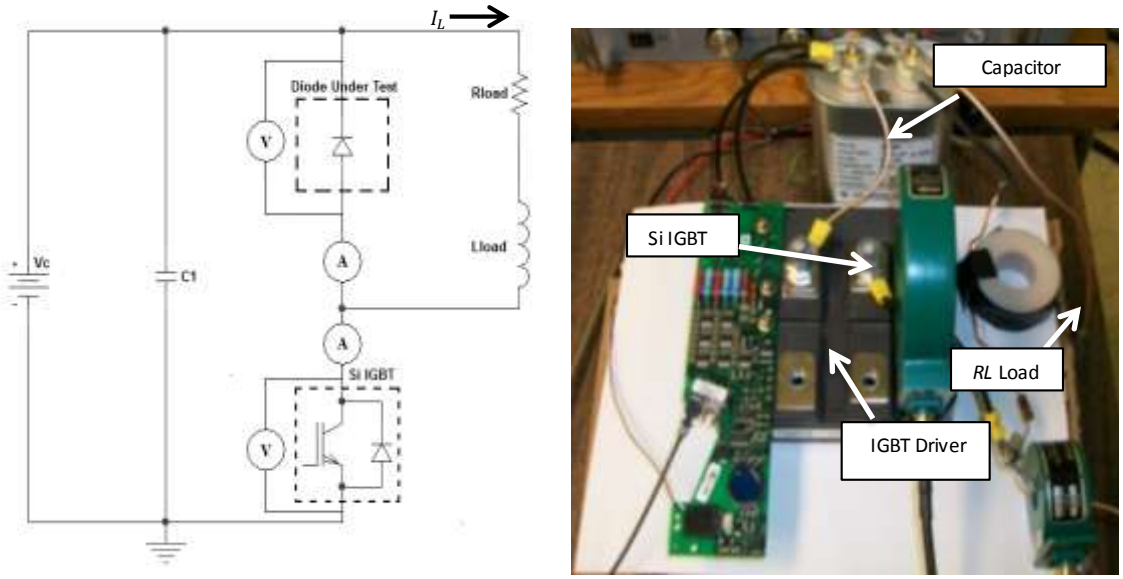


Figure 2-14. Diode dynamic characterization setup. a) Schematic representation of the double-pulse test circuit. b) Physical lab setup.

The reverse recovery response of the DUT is observed using a Model 1025 Pearson coil current transducer. A single 10 µF capacitor is used, with a series inductance of approximately 90 nH. The DUT is enclosed in the Sun Electronic Systems thermal chamber. The chamber is programmed to maintain a desired ambient temperature for 40 minutes so that the die temperature may stabilize before data is taken. The load current is controlled via the capacitor charge voltage, V_c, while the load resistance is fixed at 2 Ω. Stray inductance is minimized by keeping circuit connections as short as possible.

The relationship between the load current, I_L, and the diode forward current can be derived by looking at the behavior of the circuit in Figure 2-15a after the end of the first pulse. With the IGBT off, the circuit is reduced to a single loop containing the diode and load. The inductor attempts to counter the sudden change in load current by producing a voltage across its terminals in a direction that opposes the change. For this reason, the inductor can be represented at this point as a DC voltage source. The resulting circuit is shown in Figure 2-15.

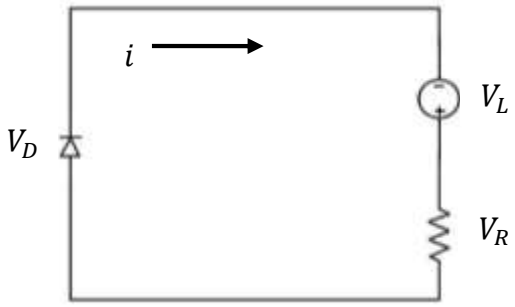


Figure 2-15. Circuit representing diode and load during switch off-state.

From Kirchhoff's Voltage Law (KVL), the loop equation is given by

$$-L\frac{d_{I_L}}{dt} = V_R + V_D \tag{2-2}$$

where the first term is the inductor voltage, V_R is the voltage across the load resistor, and V_D is the diode voltage. Solving this differential equation for the load current results in

$$I_L = I_{Lo}e^{\frac{-R}{L}t} \tag{2-3}$$

where I_{Lo} is the initial load current. Figure 2-16 shows Equation (2-3) plotted for several load currents. When the diode reverse recovery current is measured, the initial diode forward current, I_{Fo}, is equal to the load current at the time when the diode switches off, toward the tail end of the

exponential curve. Clearly, the measured initial diode forward current is dependent on initial load current.

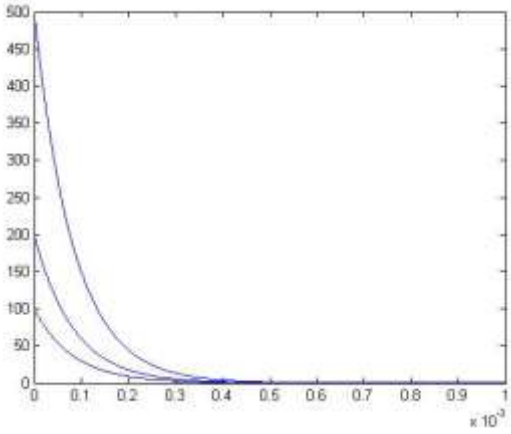


Figure 2-16. Load current curves for varying initial load current.

The separation between curves in Figure 2-16 suggests that the relationship between the initial load current and measured initial diode forward current is logarithmic. Figure 2-17 shows a logarithmic curve fit to three experimental data points of the form (I_{Lo}, I_{Fo}). The equation of the line is determined to be

$$I_F = \frac{1}{0.06915} \ln\left(\frac{I_L}{15.69}\right). \tag{2-4}$$

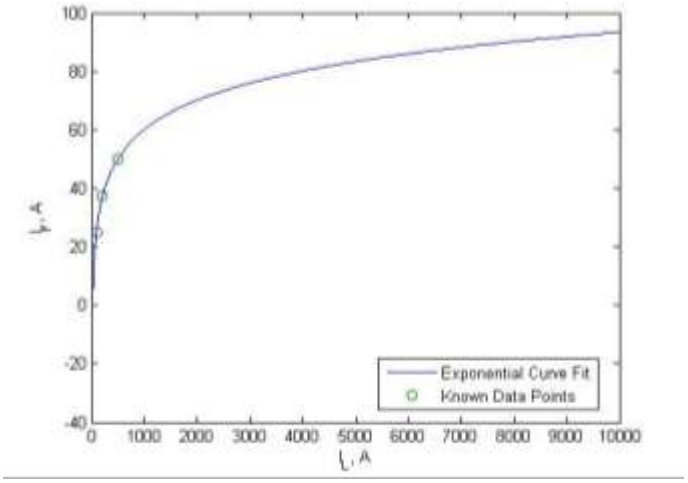


Figure 2-17. Exponential curve fit showing relationship between initial load current, I_{Lo}, and diode forward current, I_F.

The curve is plotted for load currents up to 10 kA as may be seen in low power IPPTs, and shows the three known data points as they fit on the curve. Using Equation 2-3, it is possible to estimate the initial diode current seen by the DUT for each given initial load current. In the following section, current values are expressed in terms of measured initial diode forward current, either using empirical data that relates the nominal initial load current to I_{Lo}, or using an estimate obtained from Equation 2-4.

2.3.2 Data and Results

A double-pulse test was conducted at -25 °C, 25 °C, 75 °C, and 125 °C to examine the reverse recovery response of the SiC PiN diode. Reverse recovery waveforms were collected at a nominal load current, I_L, of 100 A, 200 A, and 500 A at each temperature. Waveforms were also collected for the Si diode to allow for a comparison of reverse recovery characteristics. The temperature-dependent reverse recovery current waveforms for the Si and SiC diodes are shown in Figure 2-18.

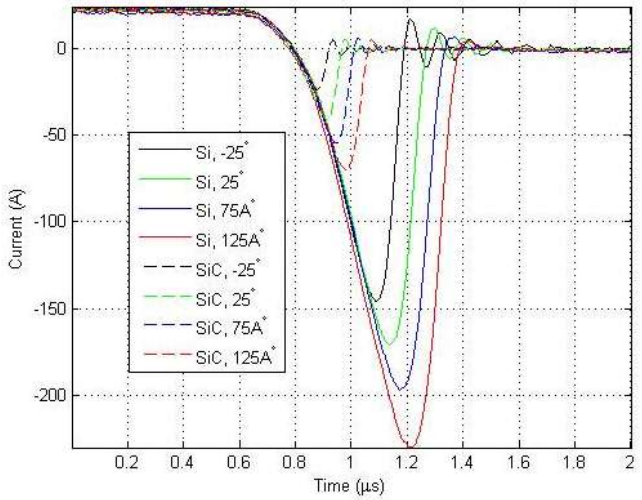


Figure 2-18. Comparison of reverse recovery waveforms for Si and SiC diodes at varying temperature and I_{Fo}= 25 A.

In each case, the nominal load current is equal to 100 A. The ringing in the waveforms is due to stray inductance in the test circuit, which is estimated to be on the order of 100 nH. As expected, the reverse recovery time, t_{rr}, reverse recovery charge, Q_{rr}, and peak reverse recovery current, I_{dRM}, of each diode corresponds directly to the temperature change. For each diode, this is primarily due to the increased carrier recombination lifetime as the temperature increases.

Upon comparing the reverse recovery current waveforms of the Si and SiC diodes, it can be seen that, at corresponding temperatures, the reverse recovery time, charge, and peak current are all significantly lower for the SiC diode than for the Si diode. This is explained by the lower carrier lifetime of SiC, as compared with Si [8].

Using a triangular approximation of the reverse recovery waveforms [24], the total diode reverse recovery energy, E_{rr} is given by

$$E_{rr} = Q_f V_{DC} \tag{2-5}$$

where Q_f is the portion of the charge, Q_{rr}, that contributes to the reverse recovery losses, measured from the time of peak reverse recovery current to the time at which the current again crosses zero. V_{DC} is the forward blocking voltage of the diode. The reverse recovery parameters for each diode at -25°C, 25°C, 75°C, and 125°C are listed in Table 2-4. Table 2-4 confirms that the reverse recovery parameters are significantly lower for the SiC diode than for the Si diode at each temperature. Notably, the peak reverse recovery current for SiC at -25°C is a factor of 6 lower than for Si at the same temperature, while the reverse recovery time, charge, and total reverse recovery energy are reduced by factors of approximately 3, 19, and 15, respectively.

The reverse recovery energy for each diode is plotted as a function of the ambient temperature in Figure 2-19. A line of best fit is shown for each set of points. From this figure, it is

Table 2-4. Calculated reverse recovery parameters for the Si and SiC diodes at varying temperatures and I_{Fo}=25 A.

Device Under Test	Ambient Temperature (°C)	I_{dRM}, A	t_{rr}, µs	Q_{rr}, µC	E_{rr}, mJ
Si	-25	145.8	0.397	28.9	7.5
	25	171.0	0.473	40.4	11.2
	75	196.6	0.557	54.8	16.1
	125	229.9	0.613	70.5	21.2
SiC	-25	24.1	0.128	1.5	.49
	25	40.7	0.183	3.7	1.1
	75	54.7	0.224	6.1	1.7
	125	70.0	0.269	9.4	2.8

clear that the value of the reverse recovery energy and the rate of increase of the reverse recovery energy per unit rise in temperature is greater in each case for the Si diode than for the SiC diode.

The equation for the linear fit of the Si data is $0.0921x + 9.3774$, while that for the SiC data is $0.0149 + 0.7752$- a factor of 6 difference in slope. The linear fit can be used to extrapolate the value of the reverse recovery energy to a variety of temperatures.

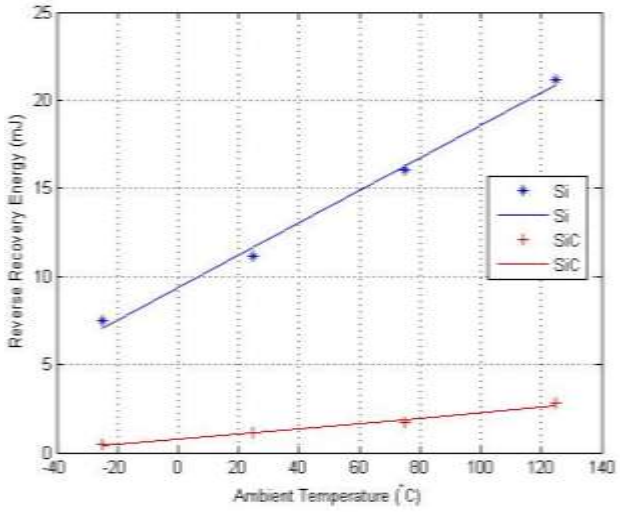


Figure 2-19. Data points and linear fit for reverse recovery energy, E_{rr}, at -25°C, 25°C, 75°C, and 125°C and I_{Fo} = 25 A for Si and SiC diodes.

In order to investigate the dependence of the diode E_{rr} on forward current, reverse recovery waveforms for each diode were measured at nominal load currents of 100 A, 200 A, and

500 A at an ambient temperature of 25°C. The current-dependent waveforms for the SiC diode are shown along with those for the Si diode in Figure 2-20. It is clear that, for each diode, the reverse recovery response increases with increasing I_{Fo}, and that, at each current, the reverse recovery response is significantly greater for the Si diode than for the SiC diode.

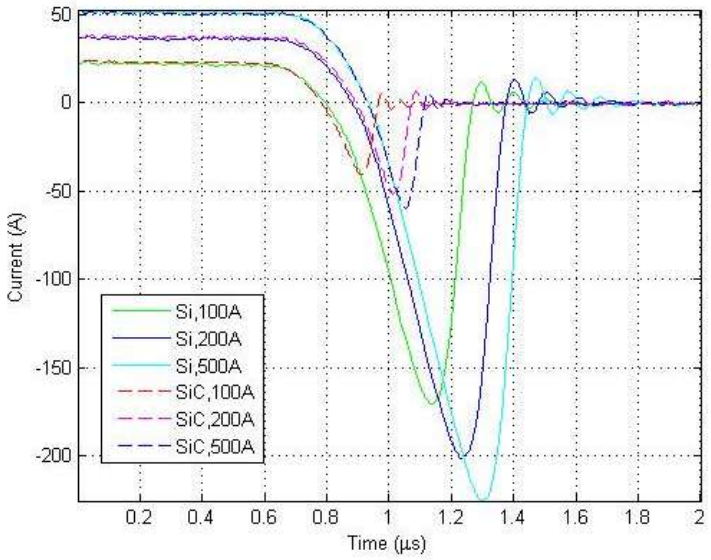


Figure 2-20. Comparison of reverse recovery waveforms for the Si and SiC diodes at varying diode forward current and 25°C.

Again using a triangular approximation of the reverse recovery waveforms, the reverse recovery parameters for each diode at an ambient temperature of 25°C and measure I_{Fo} of 25 A, 37.5 A, and 50 A are calculated and tabulated in Table 2-5. Table 2-5 confirms that the reverse recovery parameters are significantly lower for the SiC than for the Si diode under all conditions. The peak reverse recovery current for SiC at a diode forward current of 50 A is nearly 4 times lower than that for Si, while the reverse recovery time, charge, and total reverse recovery energy are reduced by factors of approximately 3, 10.5, and 9.5, respectively.

The reverse recovery energy for each diode is plotted as a function of the diode forward current in Figure 2-21. A line of best fit is shown for each set of points. From this figure, it is

clear that the value of the reverse recovery energy and the rate of increase of the reverse recovery energy per unit rise in I_{Fo} is greater in each case for the Si diode than for the SiC diode. The equations for the linear fit of the Si

Table 2-5. Calculated reverse recovery parameters for the Si and SiC diodes at 25°C and varying I_{Fo}.

Device Under Test	*Diode Current (A)*	I_{dRM} *(A)*	t_{rr} *(µs)*	Q_{rr} *(µC)*	E_{rr} *(mJ)*
Si	25	171.0	0.474	40.5	11.2
	37.5	201.7	0.496	50.0	14.4
	50	225.5	0.513	57.8	17.0
SiC	25	40.7	0.183	3.7	1.1
	37.5	51.7	0.181	4.7	1.6
	50	59.7	0.185	5.5	1.8

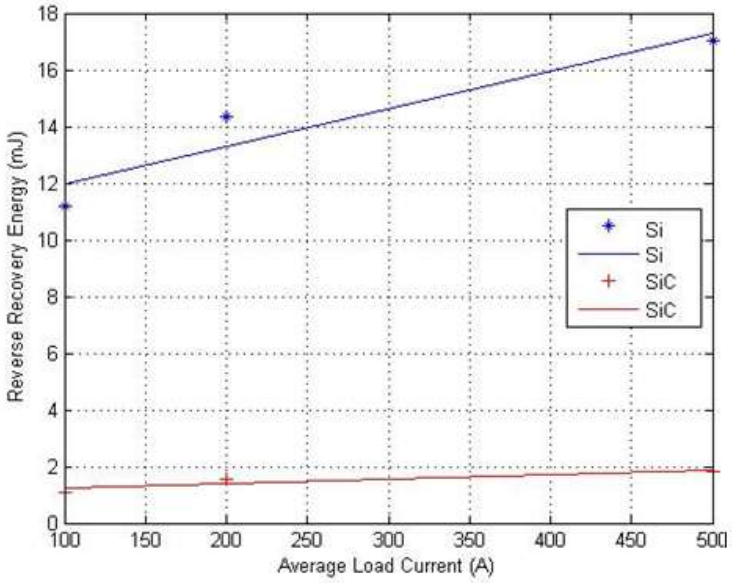


Figure 2-21. Data points and linear fit of reverse recovery energy, E_{rr}, at 25°C for I_{Fo} = 25 A , 37.5 A, and 50 A for Si and SiC.

data is $0.0132x + 10.653$, while that for the SiC data is $0.0016x + 130713$- a factor of 8.25 difference in slope. Upon comparing the values of the slopes with those of the best fit lines in Figure 2-15, it can be concluded that ambient temperature has a greater effect on the diode reverse recovery than diode current, for both Si and SiC diodes. Using the lines of best fit, a prediction can be made of reverse recovery energy for both diodes up to load currents of 10-20 kA, such as are used in IPPT drive circuit applications.

The significant reduction in reverse recovery current, time, charge, and energy for the SiC diode as compared to the Si diode will result in reduced switching losses for the SiC device. An additional benefit of the SiC diode's superior turn-off capability can be seen by looking at the corresponding portion of the current waveform for the Si IGBT used in the double pulse test circuit, as discussed in the following section.

2.3.3 Additional Considerations

In additional to directly reducing energy lost in the circuit due to diode switching losses, faster diode switching also serves to reduce stress on other circuit components. In particular, a sharp spike in the main switch current is observed to correspond to diode turn off, due to reversal of the diode current. The magnitude of the spike is directly proportional to the magnitude of the diode reverse current, $I_{dRM.}$ Figure 2-22a shows the IGBT current waveforms for both the Si and SiC double-pulse test at varying temperature and a diode current of 25 A, while Figure 2-22b shows the corresponding waveforms at a fixed temperature of 25°C and diode currents of 25 A, 37.5 A, and 50 A. For each case, the current spike caused by the SiC diode is significantly smaller than that caused by the Si diode, due to the lower reverse current seen by the SiC device. This translates to less stress on the switch, which may reduce the probability of switch failure and extend the component's lifetime.

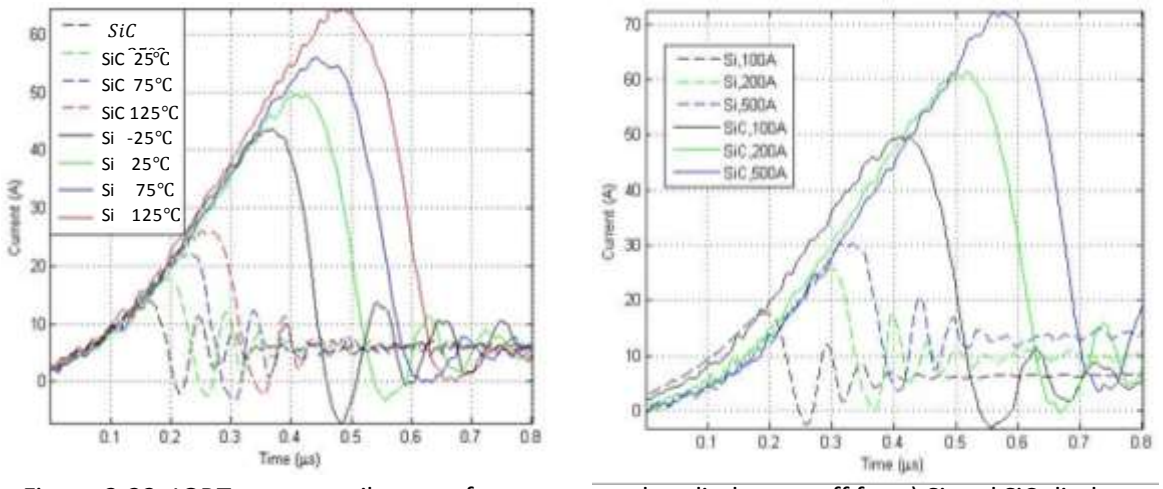


Figure 2-22. IGBT current spike waveform measured at diode turn off for a) Si and SiC diodes at $I_L = 100\,A$ and varying temperatures. b) Si and SiC diodes at 25°C and varying load current.

From the data presented in this section, it is concluded that the SiC diode tested has significantly lower reverse recovery losses than the Si diode for a variety of operating conditions. From this, it is reasonable to conclude that the use of a series SiC diode in the proposed drive circuit topology will lead to reduces switching losses, and less stress on the main switch as opposed to the use of a Si diode in the same configuration. It is noted, however, that conduction losses must also be taken into consideration when calculating the total diode losses. A discussion of total diode losses and circuit efficiency is presented in Chapter 3.

CHAPTER 3
IPPT ELECTRICAL CIRCUIT SIMULATION

Due to resistive dissipation of the ringing energy in a conventional, non-diode-clamped IPPT circuit, the recapture efficiency, η_r, of such a circuit is clearly zero. In order to estimate the maximum theoretical η_r that can be obtained through the use of the diode-latched topology, a simple circuit model of the thruster is developed. The circuit is then described mathematically and modeled in MATLAB/Simulink©. The model takes into account non-ideal circuit parameters such as stray resistance and stray inductance, however an ideal switch and diode are assumed.

3.1 SIMULINK MODEL OF IPPT

As discussed in Section 1-2, an IPPT can be model electrically as a switched series *RLC* circuit. The drive circuit provides the energy to the acceleration coil to ionize the neutral gaseous propellant. This circuit consists of a capacitor bank with an initial charge, V_{ci}, and some type of switch that connects the capacitor bank to the acceleration coil. In practice, the circuit will also have some stray series resistance, R_s, and stray series inductance, L_s (Figure 3-1).

As the plasma current sheet forms on the coil face and is axially accelerated away from the thruster, the two currents in the coil and plasma result in a magnetic coupling between the plasma and drive circuit. The mutual inductance, *M*, between the two is dependent on the axial distance of the plasma current sheet from the coil, and consequently is time-varying as the plasma moves away from the coil. Due to this affect, the measured self-inductance of the acceleration coil depend on the distance of the plasma current sheet. The effect of this mutual inductance will be addressed in more detail in Section 4.3, or alternatively the reader may refer to [2] for a detailed examination of the magnetic coupling.

For the purpose of estimating the circuit efficiency however, the inductance in the circuit model can be represented as a single inductor. Since the ringing of the current and voltage waveforms in the circuit occur on a relatively short time scale, (one cycle per 20 μs) it is assumed that the coil self-inductance as seen by the drive circuit during this time is near constant, and can be assumed to be the "shorted" inductance of the acceleration coil with the plasma current sheet at an axial distance of 0 cm [2].

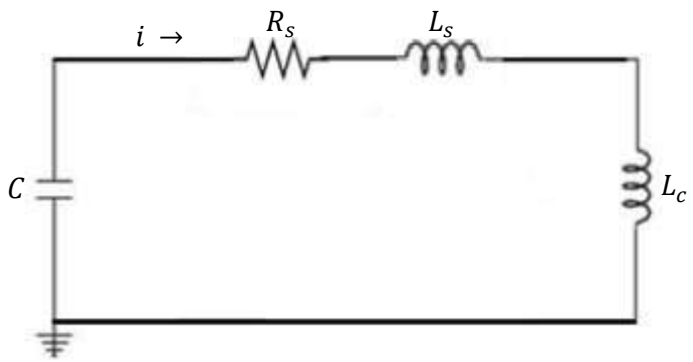


Figure 3-1. Basic RLC electrical circuit model for IPPT.

The circuit in Figure 3-1 can be described mathematically by a set of two coupled first-order Ordinary Differential Equations (ODEs). The first is readily derived from Kirchhoff's Voltage Law for the loop:

$$V_c = (L_s + L_c)\frac{di(t)}{dt} + iR_s \tag{3-1}$$

where V_c is the voltage across the initially charged capacitor, L_s is the circuit stray inductance, L_c is the acceleration coil inductance, R_s is the circuit stray resistance, and i is the current in the circuit. Solving for $\frac{di(t)}{dt}$ in Equation 3-1, the ODE becomes

$$\frac{di(t)}{dt} = \frac{V_c - iR_s}{L_s + L_c}, \tag{3-2}$$

with the associated initial condition

$$i(0) = 0\ A. \tag{3-3}$$

The second ODE is derived from the V-I characteristic of a capacitor, and is written

$$\frac{dV_c(t)}{dt} = \frac{-i(t)}{C}, \tag{3-4}$$

with initial condition

$$V_c(0) = V_{ci}. \tag{3-5}$$

This system of coupled ODEs is readily solved using MATLAB/Simulink©. The Simulink model is shown in Figure 3-2. The model solves for the current, $i(t)$, in the circuit and the capacitor voltage $V_c(t)$.

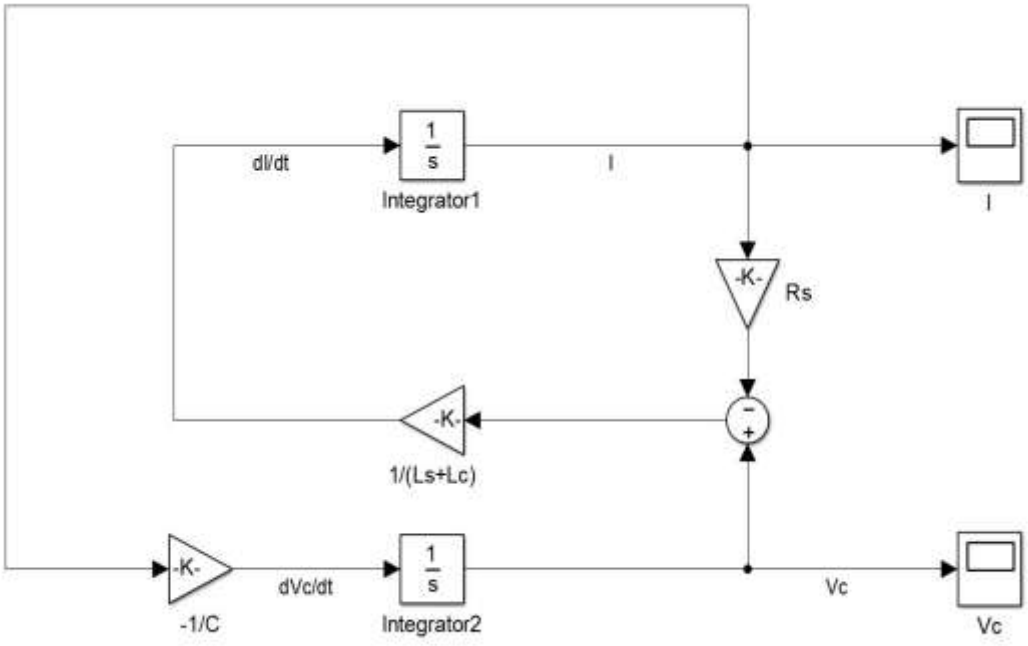


Figure 3-2. Simulink© model of RLC IPPT electric circuit model as coupled first order ODE.

Table 3-1. Simulink© model electrical components values.

Parameter	Value
Capacitance	10μF
Initial Capacitor Voltage	1000V
Coil Inductance	700nH
Stray Inductance	330nH
Stray Resistance	0.05Ω

The values of all components used in the model are listed in Table 3-1, while model configuration parameters are listed in Table 3-2. It should be noted that the circuit is modeled as a pair of coupled first-order ODEs rather than a single 2nd-order ODE for more robust simulation conversion.

Table 3-2. Simulink© model simulation parameters.

Parameter	Value
Simulation Time	2.30025e-04s
Solver	Ode15s (stiff/NDF)
Max Step Size	1e-5
Min Step Size	1e-27
Initial Step Size	Auto
Solver Reset method	Fast
Relative Tolerance	1e-3
Absolute Tolerance	1e-5
Shape Preservation	Disable All
Number of consecutive Min Steps	1
Solver Jacobian Method	Auto
Zero-Crossing Control	Use Local Settings
Algorithm	Adaptive
Time Tolerance	10*128*eps
Signal Threshold	Auto
Number of Consecutive Zero Crossings	1000

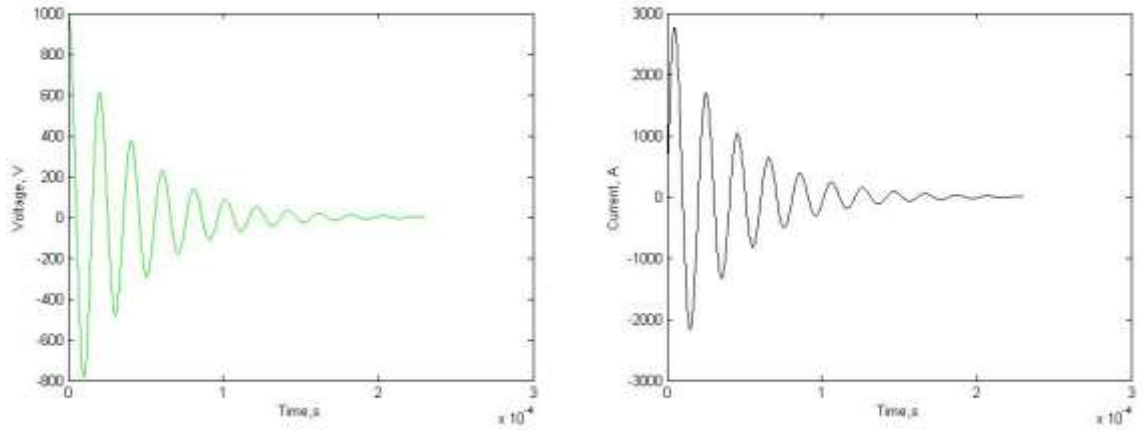


Figure 3-3. Simulated current and voltage waveforms for the circuit in Figure 3-1. The estimated ringing frequency is 50 kHz. a) Capacitor voltage. b) Loop current.

The simulated waveforms for the capacitor voltage and loop current are shown in Figure 3-3a and Figure 3-3b, respectively. The waveforms indicate an underdamped response at a frequency of approximately 50 kHz. As discussed in Section 1.2.1, the energy is the drive circuit no longer does work on the plasma current sheet after the plasma has decoupled from the acceleration coil, which occurs after the first half-cycle of the current waveform. After this, the remaining energy that oscillates in the circuit is dissipated as heat.

3.2 DRIVE CIRCUIT EFFICIENCY

In order to preclude energy-waste and excess heating, a series diode can be used to clip off current flow in the circuit at the first zero crossing, as shown in the proposed drive circuit topology of Figure 1-5. In practice, the reverse recovery time of the diode causes additional energy loss in the circuit, equal to the total diode reverse recovery energy.

While the energy total thrust efficiency, η_t, of an IPPT takes into account the losses incurred during energy coupling into the plasma, this work focuses solely on quantifying the thruster drive

circuit efficiency via a quantity that shall be defined as the capacitor bank *recapture efficiency*, η_{RC}. A simple way to obtain a relative measure of total circuit losses is to consider the capacitor bank energy, E_C, calculated as

$$E_C = {}^1\!/_2\, C V_c^{\,2}, \tag{3-6}$$

where C denotes the capacitance and V_c denotes the capacitor bank voltage, as before. The thruster drive circuit recapture efficiency, η_{RC}, is then defined as the percentage of energy that remains on the capacitor after one discharge cycle:

$$\eta_{RC} = \frac{E_{Cf}}{E_{Ci}} \times 100\% \tag{3-7}$$

where E_{Ci} and E_{Cf} represent the initial and final capacitor bank energies, respectively. The recapture efficiency conglomerates all circuit losses, including resistive losses in circuit connections, SCR and diode conduction losses, and SCR and diode switching losses. A drawback of this definition is that it is not possible to separate these effects. However, this technique is sufficient to demonstrate a relative gain or loss in drive circuit efficiency between different switch module configurations.

Equation 3-8 can be used to determine a baseline value for circuit efficiency for the ideal case where current in the circuit is cut off at the first zero crossing. An estimate of the capacitor bank energy loss between the time at which the drive circuit switch is closed ($t = 0$) and the time at which the first current zero crossing ($t = t_1$) occurs can be determined by finding the average power dissipated over a quarter cycle of the voltage waveform. For a sinusoidal waveform, average voltage drop over one quarter cycle is given by

$$V_{avg,(0-\pi/2)} = \frac{2V_{pk}}{\pi} \tag{3-8}$$

where V_{pk} is the peak value of the sinusoid. This value is then subtracted from the initial charge voltage, V_{ci}, to determine the capacitor bank voltage at time $t = t_1$. The value of E_{Cf} can then be calculated using Equation 3-6.

For a 10 μF capacitor charged to 1 kV, the initial energy at time $t = 0$ is found to be 50 J. The average voltage drop over the first quarter cycle is then approximately 636.62 V, for a final capacitor voltage magnitude of 363.38 V at time $t = t_1$. Using equation 3-6, E_{Cf} is found to be 0.66 J. Finally, Equation 3-7 is used to determine η_{RC} for this ideal case. The calculation indicates that 13.2% of the energy remains in the capacitor bank following a single discharge cycle. The calculation parameters are summarized is Table 3-3.

As discussed in Section 3.2, the non-ideal case involves a diode with some reverse recovery energy loss, which will reduce the circuit efficiency. Due to the direct relationship between the device forward current and reverse recovery energy, these losses are significant (on the order of joules as opposed to millijoules) for high-current, repetitively-pulsed IPPT drive circuit operation.

Table 3-3. Ideal IPPT drive circuit recapture efficiency calculation parameters.

Parameter	Value
$\boldsymbol{C, \mu F}$	10
$\boldsymbol{V_{c(t=0)}, V}$	1000
$\boldsymbol{E_{c(t=t_1)}, J}$	5
$\boldsymbol{\Delta V_{c,t=0-t_1}, V}$	636.62
$\boldsymbol{V_{c,t=t1}, V}$	363.38
$\boldsymbol{E_{c,t=t_1,}\, J}$	0.66
$\boldsymbol{\eta_{RC,Ideal}}$	13.2%

CHAPTER 4
FLAT-PLATE THRUSTER PROOF-OF-CONCEPT EXPERIMENT

The Flat-Plate Thruster (FPT) is a modular, small-scale IPPT has been designed at NASA Marshall Space Flight Center (MSFC) to serve as a flexible test-bed for solid state switching components and pulsed propellant injection technology. Use of these components will eventually allow for thruster testing in repetition-rate mode, as opposed to the single-shot testing that has been carried out to-date [2]. As a first step toward this goal, a Silicon Controlled Rectifier (SCR) switch and Fast Recovery Diode (FRD) are integrated into the thruster switch module for single-shot testing. This chapter describes important design specifications, fabrication of thruster subsystems, and the experiment setup employed to collect device switching waveforms and drive circuit efficiency data. Additional information on thruster components may be found in [2].

4.1 FPT DESIGN AND FABRICATION

The FPT was fabricated in-house at NASA-MSFC using both custom and commercial off-the-shelf (COTS) components. The thruster is designed to operate in vacuum, and special measures are taken throughout fabrication to ensure safe operation in such conditions. In particular, all surfaces exposed to high voltage are kept as clean as possible and carefully insulated. Of the five major subsystems, only three are assembled and integrated for the preliminary bench-top testing. These include the acceleration coil, the capacitor bank, and the switch module. A preionizer and pulsed propellant-injection valve are not necessary for the electrical switching test, and are temporarily omitted.

A Lexan frame provides the structure on which all thruster components are mounted (Figure 4-1). The frame dimensions are approximately 40 cm (16 in) wide, 40 cm (16 in) tall, and 38 cm (14.75 in) long. Four 35 cm (13.8 in) long, 1.6 cm (0.63 in) diameter fiberglass threaded rods

connect the two separate pieces of 1.3-cm (0.5 in)-thick Lexan that constitute the frame. Components are then mounted onto the rod. The primary materials used in the prototype FPT fabrication are Lexan, phenolic, and fiberglass rod, however a flight unit would require alternate materials for lighter overall weight and enhanced thermal management.

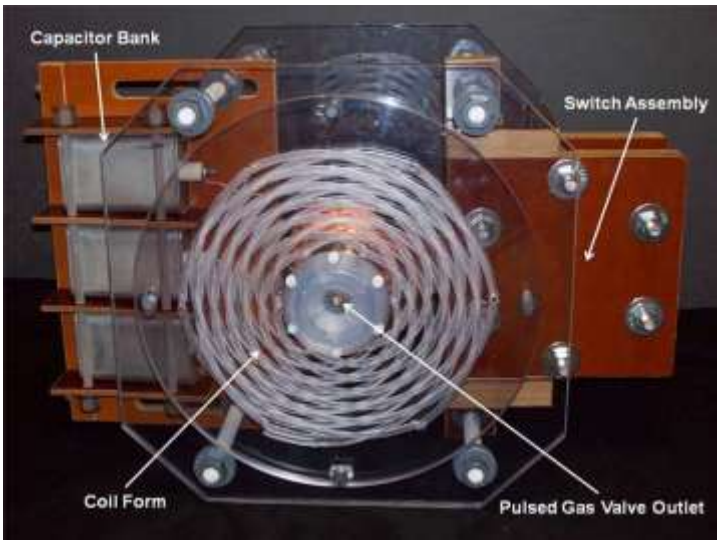


Figure 4-1. Photograph of Flat-Plate Thruster Lexan frame structure. The unfinished capacitor band, switch assembly block, and Lexan acceleration coil form are shown temporarily mounted on the frame to give the reader an idea of the thruster configuration.

4.1.1 Design Specifications

As previously discussed, the FPT is designed to serve as a testbed for technologies that ultimately allow for repletion-rate thruster operation, including solid state switching and pulsed gas injection. The thruster is therefore designed to be modular and easily modifiable. In its final configurations, a DC glow-discharge preionizer will be employed to partially ionize the neutral propellant gas, reducing the amount of energy subsequently required to ionize and accelerate the remainder of the propellant. Consequently, the thruster can be operated at a charge voltage of 4 kV on a 10 μF capacitor bank, for an energy per pulse of 80 J. The electrical parameters of the flat-plate thruster are summarized in Table 4-1.

Table 4-1. Summary of Flat-Plate Thruster electrical parameters.

Electrical Parameters	
Energy, J/pulse	80
Pulse Length, μs	~20
Coil Voltage, kV	4
Peak Coil Current, kA	>12
Capacitor Bank, μF	10
Nominal Coil Inductance, nH	650
Nominal Circuit Stray Inductance, nH	200
Predicted Circuit Stray Resistance, mΩ	10
Switch Type	Solid State

Target performance parameters for this thruster are a jet power, P_{Jet}, of 2-5 kW and an $\hat{I}_{sp}$ of 3,000-6,000 s, as would be required for a Lunar or Marian cargo mission [2].

4.1.2 Acceleration Coil

The FPT acceleration coil consists of six 10 gauge copper leads connected in parallel. The flat coil geometry was chosen because it is relatively simple to fabricate, and has been used for previous IPPTs, including the PIT and the FARAD thrusters [1, 2, 3, 4]. The copper coil leads are laid in grooves machined in a Lexan coil form, where each lead path is in the form of an Archimedes spiral. The inner radius of the coil is 5 cm, while the outer radius is 15 cm. Each lead starts on the front side of the Lexan coil form, spirals out toward the edge of the pattern, passes through a hole in the Lexan to the back side of the coil, and then spirals back in to a point directly opposite of its starting point. Additional details on coil design and can be found in [2].

The Lexan coil form is fabricated from a 1.3 cm (0.5 in) thick piece of Lexan with an inner diameter of 7 cm (2.75 in) and an outer diameter of 35.5 cm (14 in). Lexan was chosen for its

high voltage hold-off, mechanical strength, and machinability. To further prevent shorting between leads at high voltage (particularly in vacuum), insulation was applied to the Lexan grooves and copper leads. The inside of the grooves was coated with two layers of Viking varnish to seal any small fissures that may be present. The enamel-coated Copper magnet wire is additionally insulated with clear heat shrink tubing. Prior to running the thruster at high voltage in vacuum, the entire coil will be potted in RTV-560 silicon insulating compound.

The copper leads were hand-laid into the coil form groves, taking care to minimize unnecessary bending or strain. The coil form was secured on four 30.5 cm (12 in) tall posts to hold it in place as the leads were wound (Figure 4-2). Once all leads were in place, the pulsed gas valve holder assembly was placed in the coil form to help hold the leads in place on the front of the coil (not shown). On the back of the coil, the copper leads were extended with 10 gauge hookup wire rated for 30 kVDC (not shown). The fabricated coil (unpotted) is shown in Figure 4-3.

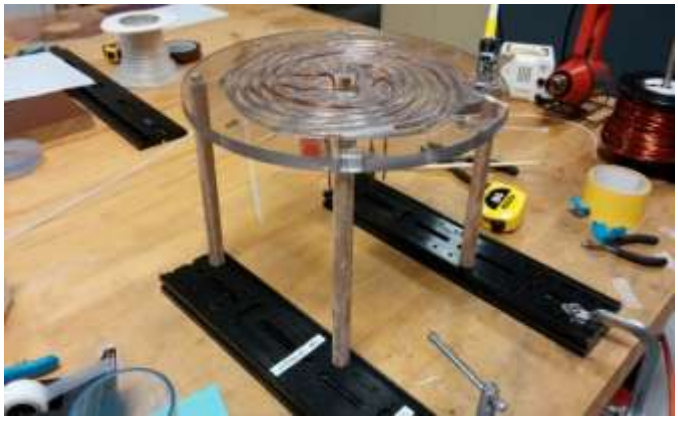


Figure 4-2. Setup for fabrication of the Flat-Plate Thruster acceleration coil. Phenolic post are used to elevate and secure the coil. The post are screwed in to optical rails which, in turn, are secured to the table using 'C' clamps.

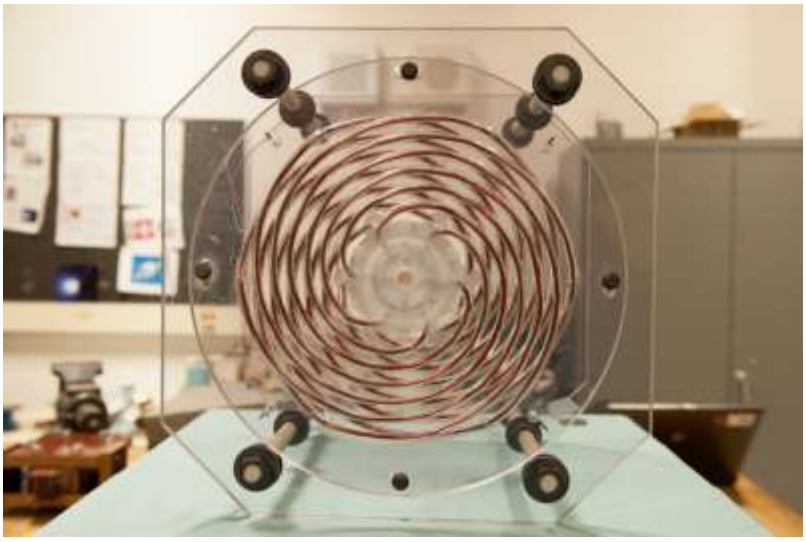


Figure 4-3. Flat-Plate Thruster Acceleration Coil (front view). The pulsed gas valve holder is attached in the center of the coil form, and aids in holding the leads in place.

The acceleration coil and plasma current sheet of an IPPT can be modeled as a pair of magnetically coupled inductors. The mutual inductance, M, changes as the plasma current sheet is accelerated away from the thruster coil. For this reason, the total effective coil inductance as measured at the coil terminals, denoted by L_{eff}, depends on the axial distance of the current sheet from the coil. If the stray inductance (such as from wires connecting the coil leads) is denoted by L_o, and the self-inductance of the acceleration coil by L_c, then the effect of the mutual inductance on L_{eff} is described by Equation 4-1.

$$L_{eff} = L_o + L_c - \frac{M}{L_c} \qquad (4-1)$$

Equation 4-1 implies that the effective inductance increases as the mutual inductance decreases, i.e., as the axial distance, z, between the coil and plasma current sheet increases. This occurs because, when the plasma is near the coil, it acts to exclude magnetic flux, thereby lowering the effective inductance. Beyond some distance z_o- known as the electromagnetic decoupling distance, or the electromagnetic stroke length- the coil inductance is no longer

affected by the plasma, and L_{eff} asymptotes toward some constant value, known as the "free-field inductance." Once this value is determined, the coil self-inductance can be calculated using Equation (4-2).

$$L_c = L_{eff} - L_o, \tag{4-2}$$

where the mutual inductance is assumed to be zero.

The coil self-inductance and electromagnetic decoupling distance were predicted using a two-dimensional QuickField™ simulation in AC Magnetics mode. A voltage oscillation frequency of 50 kHz was assumed, as this is the expected discharge frequency of the thruster. The plasma current sheet is modeled by a 5 mm thick annular disk with a resistivity similar to that of aluminum ($4x10^{-8}$ Ω-m).

The coupling coefficient, k_o, between the coil and disk is assumed to be 0.907. A perfect coupling of 1.000 would imply that the two elements have the same shape and initially occupied the same volume. This imperfect coupling introduces some residual effective inductance, which is estimated to be approximately 100 nH. Stray inductance (due to auxiliary connection, excess wire-lengths, and terminations, etc.) is neglected. Using this model, the predicted self-inductance of the coil was found to be 729 ± 2 nH, while z_o was estimated as 6.3 ± 0.1 cm.

In order to determine the actual self-inductance and electromagnetic decoupling distance of the manufactured FPT acceleration coil, inductance measurements were taken using the setup shown in Figure 4-4. Here, the plasma current sheet is simulated using a 0.16 cm ($1/8^{th}$ in) thick annular copper disk with resistivity of approximately $1.68x10^{-8}$ Ω-m. The copper disk is attached the end of a phenolic rod mounted on a phenolic stand. This allows the disk to move

along the z-axis of the coil by sliding on an optical rail securely fasted to the table. The copper disk is elevated a distance of several coil radii above the rail, in order to prevent the metal rail from affecting the inductance measurements.

Figure 4-4. Inductance Measurement setup. The copper disk simulates the plasma current sheet, and inductance measurements are taken to determine the coil self-inductance and electromagnetic decoupling length of the manufactured FPT acceleration coil.

Weights are added to counter-balance the horizontal rod and keep the disk as level as possible. The other thruster components are temporarily omitted in order to obtain an inductance measurement of the acceleration coil alone, as opposed to the entire circuit, and to avoid effects from any metal components or loose wires. A temporary single connection point is made to each set of six coil leads on either side of the coil form. This is done with jumper wires, connected to the leads with wire nuts. The jumper wires are bent at 90° angles into a "U" shape (Figure 4-5a and Figure 4-5b), in order to minimize potential stray inductance due to distance between the jumpers and coil face.

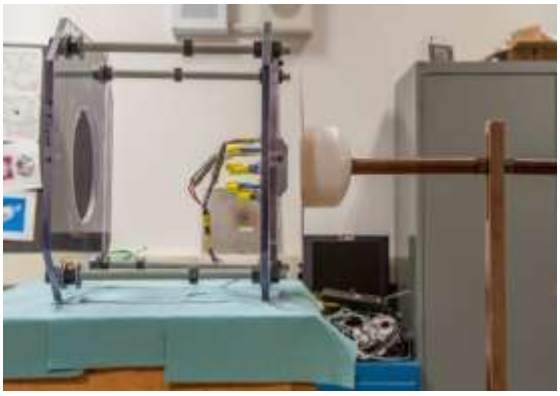


Figure 4-5. Acceleration coil connections. a) Back isometric view. b) Side view.

Initially, the copper disk was positioned as close to the coil face as possible. The remaining gap was estimated to be approximately 1 cm (0.4 in), with a slight drooping of the phenolic rod assembly causing the disk to be 2-3 mm (0.08-0.12 in) farther from the bottom of the coil than the top. The disk was then incrementally backed away from the coil along the optical rail, and the measured inductance was noted at each location. Since the inductance changes rapidly at first, measurements were taken at 0.2 cm (0.08 in) increments for the first 2 cm (0.8 in), 0.5 cm (0.2 in) increments for the next 5 cm (2 in), and 1 cm (0.4 in) increments thereafter. Measurements were acquired using an Agilent 4285A Precision RLC meter (Figure 4-6) with the measurement configuration parameters listed in Table 4-2.

Figure 4-6. Agilent RLC Meter. An Agilent 4285A Precision RLC meter was used to collect inductance measurements of the FPT acceleration coil.

Table 4-2. Agilent RLC meter configuration parameters.

RLC Meter Parameters	
Function	$L_s - R_s$
Frequency, kHz	100.0
Level, V	1.00
Range	Auto
Bias, V	0.00
Integration	Medium

Figure 4-7 shows the dependence of the measured effective inductance, L_{eff}, on axial distance of the copper disk. The effective coil inductance is observed to asymptote to a value of 1102 nH, which occurs beyond an electromagnetic decoupling distance of approximately 6 cm. The decoupling length is found to be within 3% of the predicted value. The initial parasitic inductance, L_o, due to the imperfect coupling between the coil and the copper disk, is approximated to be about 400 nH. Using Equation 4-2, the coil inductance, L_c, is calculated to be 702 nH. This is within 4% of the value predicted by the QuickField™ simulation. Stray inductance due to auxiliary connections, excess wire-lengths, and wire terminations is determined to be approximately 100 nH.

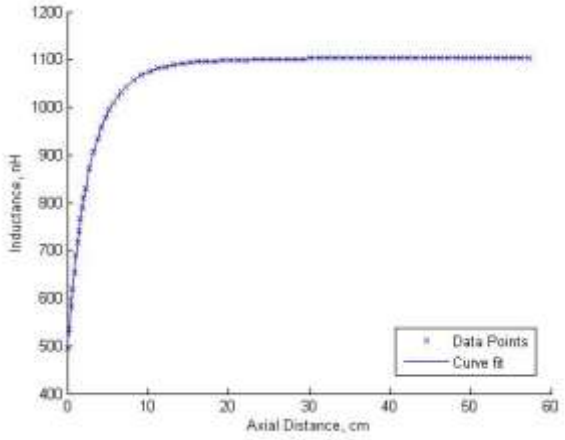


Figure 4-7. Inductance Measurement Data. The measured effective coil inductance is observed to asymptote to a value of approximately 1102 nH beyond a distance of approximately 6 cm.

It should be noted that the same value for coil self-inductance would not be obtained by measuring the inductance of each lead separately and then adding the values in parallel. While this approach works for a small number of leads, as the number of leads increases, the coil begins to look like a solid current sheet, and the inductance asymptotes to a fixed value [5]. For completeness, the inductance and series resistance of each the six copper windings was measured separately. The measurements obtained are given in Table 4-3.

Table 4-3. Individual coil lead measurements.

Coil Winding	**Measured Inductance, μH**	**Measured Series Resistance, Ω**
1	1.361	0.023
2	1.392	0.026
3	1.383	0.023
4	1.372	0.023
5	1.386	0.024
6	1.413	0.025
Average	1.3845	0.024

4.1.3 Capacitor Bank

A capacitor bank is used to store that energy that is then discharged through the acceleration coil. The capacitor bank of the FPT thruster consists of three oil-filled, vacuum-compatible capacitors, made by CSI Capacitors. The specifications for the capacitors are summarized in Table 4-4. The total capacitance of the bank can be 10, 20, or 30 µF, depending on how many of the capacitors are connected.

Table 4-4. CSI capacitor specifications.

Capacitor Specifications	
Nominal Capacitance, µF	10
Maximum Charge Voltage, kV	7.5
Series Inductance, nH	≤ 20

The capacitors are mounted on a phenolic frame, and are held in place using threaded rod (Figure 4-8). The entire module can then be mounted on the thruster frame as a unit.

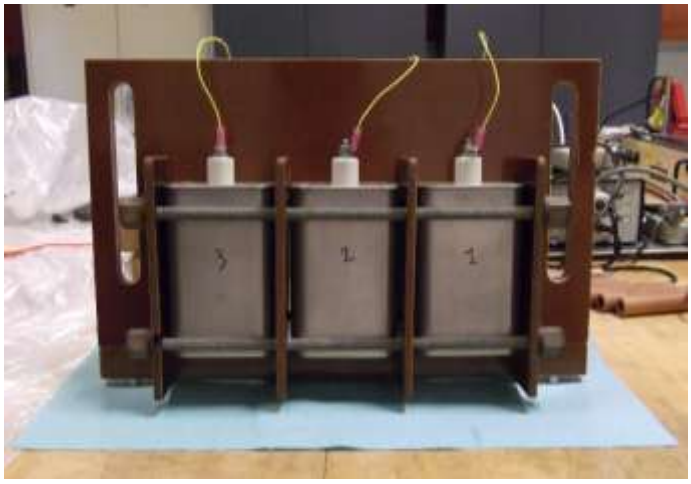


Figure 4-8. Flat-Plate Thruster capacitor bank.

The actual capacitance of each capacitor was measured using a Fluke 87-V Digital Multimeter. The capacitance measurements are given in Table 4-5.

Figure 4-5. Capacitance measurements.

Capacitor	Measured Capacitance, µF
1	9.85
2	9.88
3	9.89

4.1.4 Switch Module

In the present configuration, the switch module consists of a single SCR power thyristor in a ceramic compression ("hockey puck") package in series with a fast recovery power diode of the same packaging. The SCR is a Dynex™ PT85QWx45, optimized for use in pulsed power applications. For the experiment carried out in this work, the diode is the device under test (DUT) and is one of three devices: a Dynex *DSF21545SV* Si fast FRD, an ABB *5SDF 02D6004* Si FRD, or a prototype SiC PiN diode from Cree, Inc. A photograph of the Dynex diode (top) and SCR (bottom) is shown in Figure 4-9.

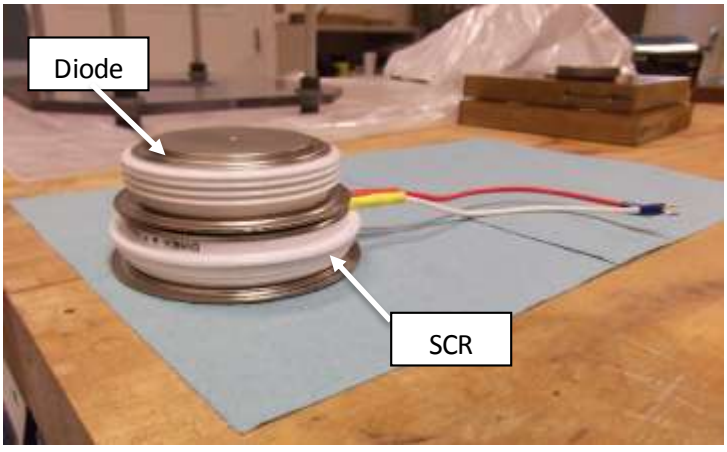


Figure 4-9. Dynex switching components. The Dynex FRD is shown in series with the Dynex SCR.

The ABB Si diode and Cree SiC diodes shown in Figure 4-10a and Figure 4-10b, respectively, will also be evaluated in the FTP circuit through bench-top testing. The ABB diode is pressure clamped using a Wakefield^{TM} clamp, with a mounting force, F_m of approximately 16 kN. G10 spacers are used to hold the device in the clamp, while also providing electrical isolation between the diode and the clamp's metal base. A phenolic stand is used to hold the diode in an upright position. Copper tabs are clamped on either side of the diode, and contain through-holes that are used to make connections to other circuit elements.

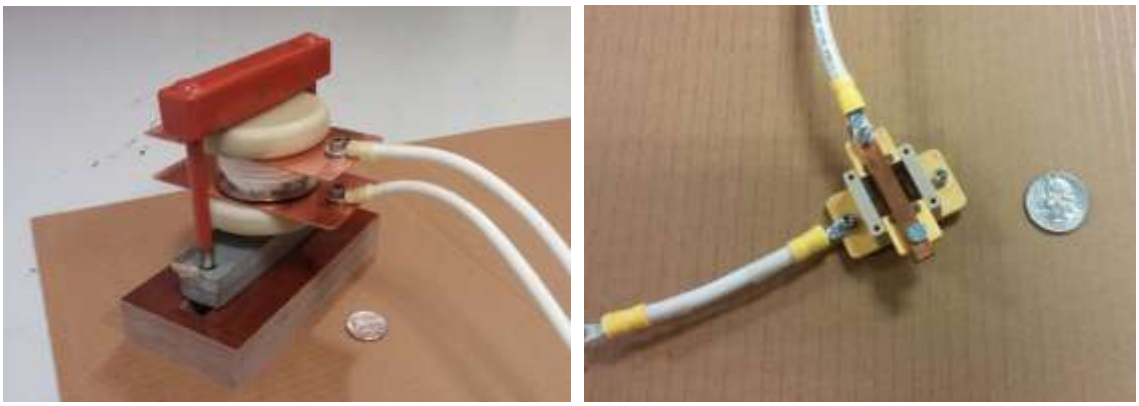


Figure 4-10. Diodes for FPT testing. a) 5.8 kV SiC PiN diode from Cree, Inc. b) 5.5 kV Si fast diode from ABB.

In the case of the SiC diode, connections are made to the copper bus bar that connects the top tabs (anode) and the bottom plate (cathode). Key performance specifications for all four solid state devices discussed above, including the SCR and three diodes, are listed in Table 4-6. As mentioned previously, no data sheet is available for the Cree SiC diode.

Figure 4-6. Solid state switching component performance specifications.

	Description	Dynex Si SCR	Dynex Si Diode	ABB Si Diode	Cree SiC Diode
V_{RRM}, V	Repetitive Peak Reverse Voltage	4500	4500	5500	5800
$I_{F(AV)}, A$	Mean Forward Current	1670	3230	175	Not available
I_{FSM}, A	Surge (non-repetitive) forward current	37000	16000	3000	Not available
$di/_{dt}, A/\mu s$	Current rise rate	22000	> 1000	> 1000	Not available
$t_{rr}, \mu s$	Reverse Recovery Time	Not available	7	2*	~1*

**Estimated from switching data presented in Chapter 2.*

The thruster circuit stray inductance and series diode topology server to limit the current and voltage rise rate through the SCR, eliminating the need for a protective snubber circuit. Connections to the switch and diode stack are made via pressure clamping at a force of 40 kN ± 10%. The mounting yoke, between which the devices are clamped, consists of two 2.54-cm-thick phenolic slabs held together by six 13.97-cm-long stainless steel bolts. Phenolic tubes fitted over the bolts are used to provide electrical insulation. To facilitate tightening of the bolts, sockets were welded to a metal plate to hold the module in place as the bolts were tightened to the necessary compressive force (Figure 4-11a and Figure 4-11b.)

Figure 4-11. Flat-Plate Thruster switch module construction. a) Isometric view. b) Front view.

Copper tabs (Figure 4-12) are clamped on either side of the SCR and diode stack, and are used to make connections to the external circuit (capacitor bank and acceleration coil). The tabs are treated with Cool-Amp paste to deposit a thin layer of elemental silver on the surface of the copper, increasing the surface conductivity. In the configuration that contains the Dynex diode, a circular gasket made of thin silver foil (0.25 mm thickness) is placed in between the SCR and Dynex diode in order to increase electrical conductivity between the two devices.

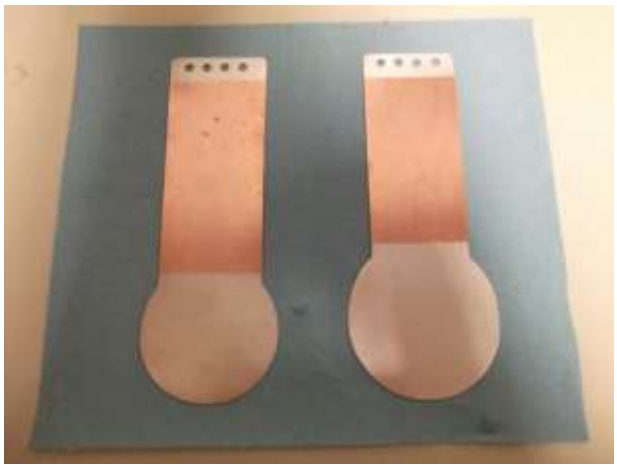


Figure 4-12. Switch module connector tabs. Silver areas were treated with Cool Amp Conducto-Lube.

In the switch configuration which includes the ABB Si diode and Cree SiC diode, the Dynex diode is removed from the switch stack and the copper tabs are clamped to either side of the SCR. Each alternative diode can then be connected to one of the SCR tabs using several parallel wires (to minimize stray inductance.) External circuit connections are made via wires from the SCR anode-side copper tab and the diode cathode-side copper tab. The complete switch module in the Dynex diode configuration is shown in Figure 4-13.

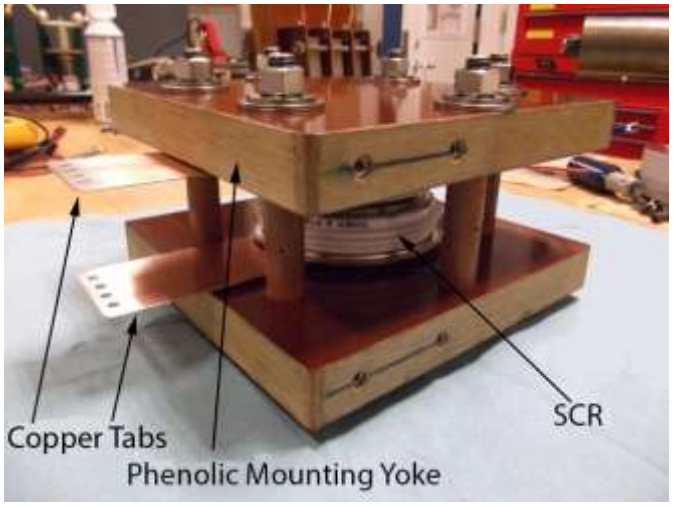


Figure 4-13. Flat-Plate Thruster Dynex configuration switch module.

The SCR gate is triggered with a 15 V pulse of duration of 20 us. The trigger signal also has a "backporch" of magnitude 4 V and adjustable duration. This prevents the SCR from switching off too soon, which may damage the device. A driver circuit was designed and fabricated on a custom printed circuit board. The driver is battery powered, providing isolation from the thruster circuit and preventing ground loops. The driver circuit is triggered via a fiber optic connection from a BNC pulse generator, and a coaxial cable connects the output pulse to the SCR gate and axillary cathode connection wires.

4.1.5 Additional Components

As previously discussed, the FPT is designed for repetition-rate operation at discharge energies lower than those required for the PIT. Operation at lower discharge energies is made possible through the use of a dedicated preionizer, which will be used to provide the initial ionization of the propellant gas. For pulsed operation, the use of a pulsed propellant injection valve reduces the risk of excessive background pressure in a vacuum environment (versus steady-state gas flow), reducing the risk of electrical arching at high voltage levels. While the preionizer

and pulsed gas valve for the propellant delivery system are not integrated into the FPT configuration used in the preliminary electric bench-top testing, significant design, fabrication, and testing has been carried out on each of these components to-date, and detailed information can be found in [2].

4.2 EXPERIMENTAL SETUP

The circuit topology chosen for the bench-top testing is shown schematically in Figure 4-14, along with measurement locations. The capacitor bank is charged via a Bertan Model 205B-20R high voltage power supply, which is connected through two normally-open Ross relays (Model E40-NO-40-1-0-BD). The charging circuit (not shown) is disconnected on both sides of the capacitor in order to prevent ground loops caused by the connection of the circuit common to the power supply earth ground. A dump resistor is connected in parallel with the capacitor through a normally-closed Ross relay (Model E40-NC-40-1-15-BD). The two charging relays are controlled by a single switch, while the dump resistor relay is controlled by a separate switch. When the charge relays are closed, the dump relay is open and the capacitor bank is charged. For safety reasons, the capacitor may be discharged through the dump resistor at any time by disconnecting the charge circuit and closing the dump resistor relay. A physical view of the charge and dump relay circuit is shown in Figure 4-15.

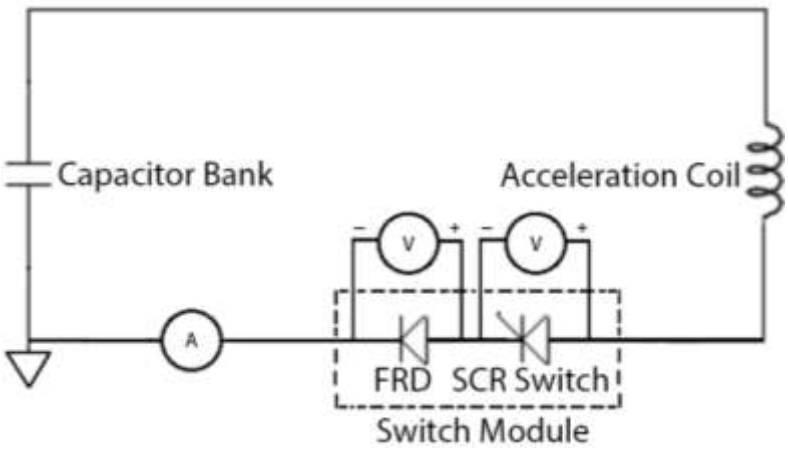


Figure 4-14. Bench-top testing circuit topology. The switch module configuration is varied.

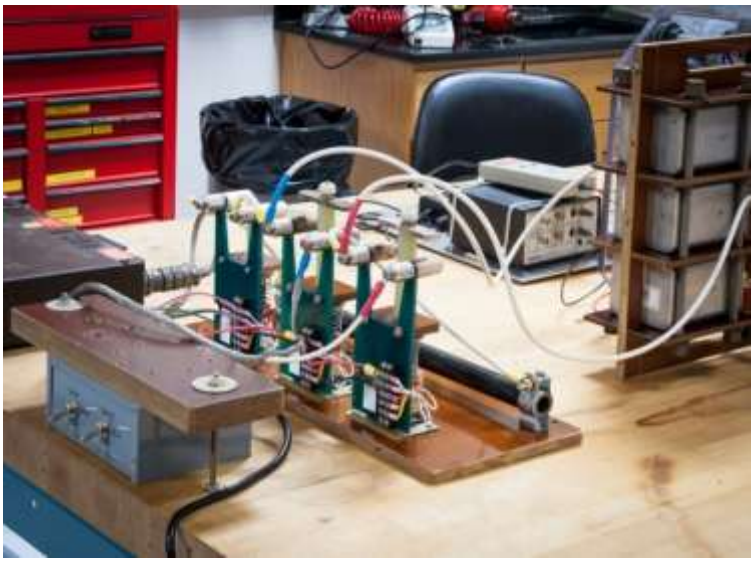


Figure 4-15. Charge/dump control circuit. The relays are opened and closed via manual switches mounted on the grey controller box. These are manipulated using a 45 cm long phenolic rod.

When the capacitor is charged, the anode terminals of the SCR and diode are at a positive potential with respect to their cathode terminals, so that both devices are forward biased. However, no current will flow through the circuit until a current pulse is applied to the SCR gate. One the SCR is triggered, the SCR turns 'ON' and current flows through the acceleration coil. As

discussed in Section 3.1, with no active circuit components, the capacitive and inductive reactance would cause the current to oscillate in the circuit.

However, in the given configuration, the SCR will become reversed biased once the polarity of the current waveform changes, i.e., at the first zero crossing of the current waveform. This causes the SCR to turn 'OFF' and interrupts the flow of current in the circuit. The remaining energy in the capacitor bank is then stored for a subsequent discharge cycle. While the SCR will theoretically switch 'OFF' at the first zero crossing, in practice there is a turn-off delay of 100s of μs introduced by the reverse recovery response of the device, dependent on the forward voltage and ambient operating temperature. For this reason, a Fast Recovery Diode (FRD) is placed in series with the SCR to cut off current as close to the zero-crossing as possible. The shorter the reverse recovery time, t_{rr}, of the diode, the faster turn-off occurs. The reverse recovery time of the Dynex FRD is < 10 μs.

The switch module is connected on the low side of the circuit, i.e., the side closest to circuit common (Figure 4-16a and Figure 4-16b). This topology has several advantages over one in which the switch module is connected on the high side. Primarily, less of the circuit is at low potential, which precludes electron emission that may lead to arching in a vacuum environment. Another advantage is that the switch module is connected directly to common, meaning that a common-referenced high voltage probe can be used to measure the voltage across it, rather than a differential probe being required. This is beneficial if only a limited number of differential probes are available.

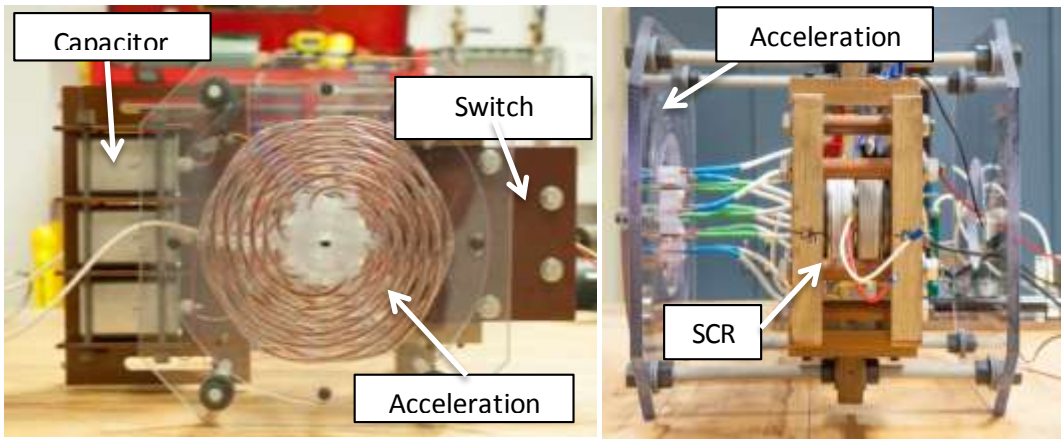
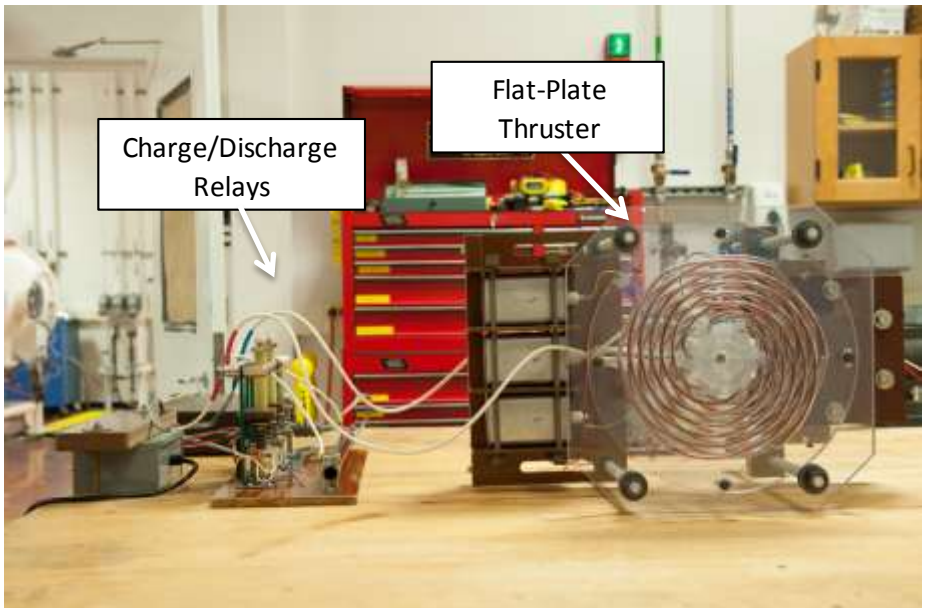


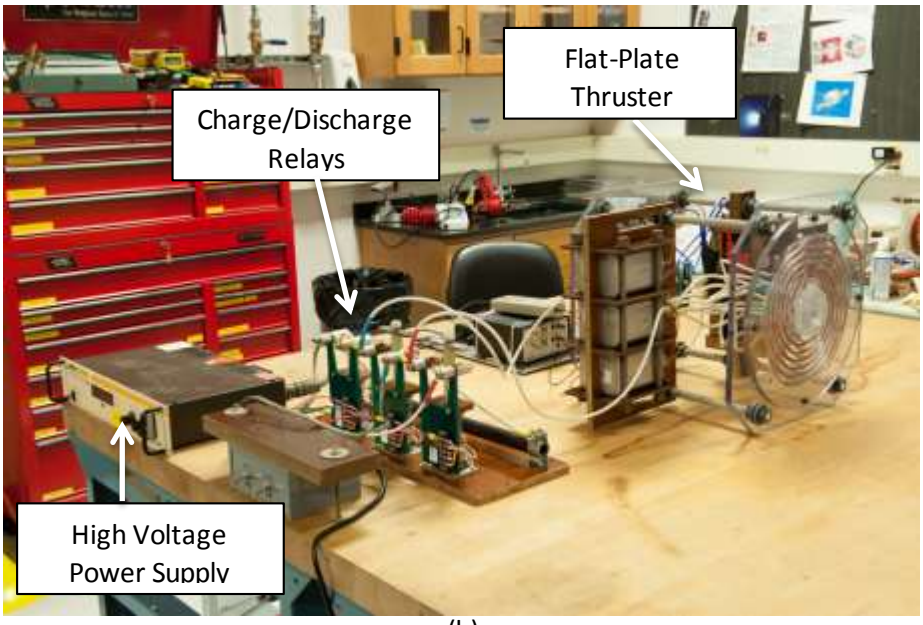
Figure 4-16. Switch module connection- physical view. a) Front view of assembled FPT. b) Side view of assembled thruster showing switch module position.

In addition to measuring the voltage across the switch module, the voltage waveform across the diode alone is measured using a Tektronix P5210 high voltage differential probe rated for a maximum differential voltage of 4400 V_{RMS}. The voltage across the capacitor bank is measured using a Tektronix P6015 high voltage probe (rated for 20 kV maximum continuous, 40 kV peak pulsed) and that across the switch module is measured using a Tektronix P5205 100MHz high voltage differential probe rated for a maximum differential voltage of 1300 V_{RMS}.

The remaining voltages in the circuit- that across the acceleration coil and that across the switch- can each be calculated from the know voltages and Kirchhoff's Voltage Law (KVL). The measurement of primary interest is the loop current, which is obtained using a Model 4418 Pearson coil (sensitivity of 0.001 ± 1% V/A, maximum peak current of 200 kA). This waveform shows the reverse recovery response of the diode, and allows for a comparison of diode switching characteristics. Several physical views of the test setup are shown in Figure 4-17a and Figure 4-17b.



(a)



(b)

Figure 4-17. Bench-top physical test setup. a) Front view. b) Isometric view.

CHAPTER 5
EXPERIMENTAL OBSERVATIONS AND MEASURMENTS

Benchtop testing of the FPT drive circuit was carried out using the Dynex model PT85QWx45 SCR and each of the series FRDs described in the previous chapter. For each configuration, loop current and voltage across several components were collected at a variety of capacitor bank charge voltages. The collected data allows for a comparison between diode reverse recovery characteristics, as well as a quantitative analysis of the circuit recapture efficiency, η_{RC}, as defined in Section 3.2. Moreover, the data allows one to make observations regarding the effect of FPT turn-off speed on other drive circuit components, and provides a general understanding of mechanics of using solid state switching in an IPPT.

5.1 FPT BENCHTOP SWITCHING DATA

This section discusses the data collection methodology, as well as presents the switching waveforms collected during preliminary FPT benchtop testing. For this preliminary testing, the capacitor charge voltage was capped at a maximum nominal voltage of 1 kV. This allows one to gain an understanding of the drive circuit while minimizing the chances of damaging the switch module components. Higher voltage benchtop switching tests will be carried out at a later time (see Forward Work).

5.1.1 Data Collection Methodology

A variety of factors were taken into account when designing the test setup and choosing the charge voltages for each switch module configuration. Primarily, the maximum current and voltage ratings for each switching device was considered in order to preclude damage or failure. In addition, dynamic ratings including maximum current and voltage rise rates, $(\mathrm{di/dt})_{\mathrm{max}}$

and $(dv/dt)_{max}$, were heeded. While the Dynex SCR is overall higher rated than the three FRDs, the charge voltage was limited by the parameters of the lowest rated device in the switch module. Due to the short duration of the applied pulse (10 μs) and the low duty cycle (single shot) the maximum surge current ratings given in the datasheet could be safely exceeded (see Section 2.1.2), and the I^2T rating used instead. The rate of current rise, as well as the peak current, in the circuit depend on the total circuit inductance, which is affected by the axial distance of the plasma current sheet as discussed in Section 4.1.2. Due to diode packaging and hookup cable locations, this changes slightly between configurations. Lower inductance configurations see higher di/dt and peak current that those with higher inductance. This is taken into account when selecting test charge voltages so as not to exceed component ratings.

While the charge voltage is capped at 1 kV to avoid damage to component over-current, it is also necessary to avoid switching the drive circuit at too low a voltage, due to the high slope resistance of the switch at lower currents. It was observed that the switch does not turn on completely as quickly at lower charge voltages (below approximately 500 V) so that there could potentially be higher internal heating of the device due to the increased resistance during this time. Due to the possibility of this leading to switch damage or failure, the charge voltage was kept above 200 V for all switching tests.

The time the switch remains closed during each discharge cycle is fixed by the ringing frequency of the circuit, since both the SCR and FRD will become reversed biased after the first current zero crossing. Due to the dependence of the ringing frequency on total inductance, this will vary slightly between switch module configurations. The total turn-off time is governed by the shorter reverse recovery time of the series components, which in each case is the FDR. A rough calculation of the highly underdamped circuit ringing frequency can be approximated using Equation 5-1.

$$\omega_o = \frac{1}{\sqrt{LC}} \qquad (5-1)$$

where L is the total circuit inductance and C is the capacitance of the capacitor bank. Based on the inductance measurements presented in Section 4.2.1, the total circuit inductance with the plasma current sheet at infinity can be estimated as 1 µH, where the coil inductance accounts for 700 nH and the remaining 300 nH is due to stray inductance caused by circuit connections. Using a measured capacitor bank capacitance of 9.88 µF, the ringing frequency is estimated to be approximately 50 kHz. Based on this, the first current zero crossing will occur approximately 10 µs after the switch is triggered.

The SCR switch will not latch, meaning that as soon as the gate pulse is removed, the switch should revert to reverse blocking mode. Normally, a snubber circuit consisting of a resistor and capacitor is connected across the SCR so as to protect the switch from high forward and reverse dv/dt, as well as high forward di/dt [25]. However, in the circuit configurations tested, the forward dv/dt is zero when the SCR becomes reverse biased at the first current zero crossing, and the diode serves to protect the switch from the reverse di/dt. If the diode is omitted- as in the case of the baseline measurement- the switch may retrigger as the current rings, even after the gate pulse has been removed. Although this should pose no danger to the SCR, the significantly longer turn-off time would adversely affect the circuit recapture efficiency. The stay inductance of the circuit is designed to limit the di/dt to an appropriate value.

It is important to ensure that the switch does not shut off abruptly prior to the current zero crossing. This would interrupt current in the circuit before the plasma has decoupled, and could potentially cause damage to the switch and series diode due to the resulting inductive voltage spike. For this reason, the gate pulse must be at least as long as the first current half cycle. The SCR driver circuit is designed to output a fixed-length current pulse of 20 µs into a 10 Ω load.

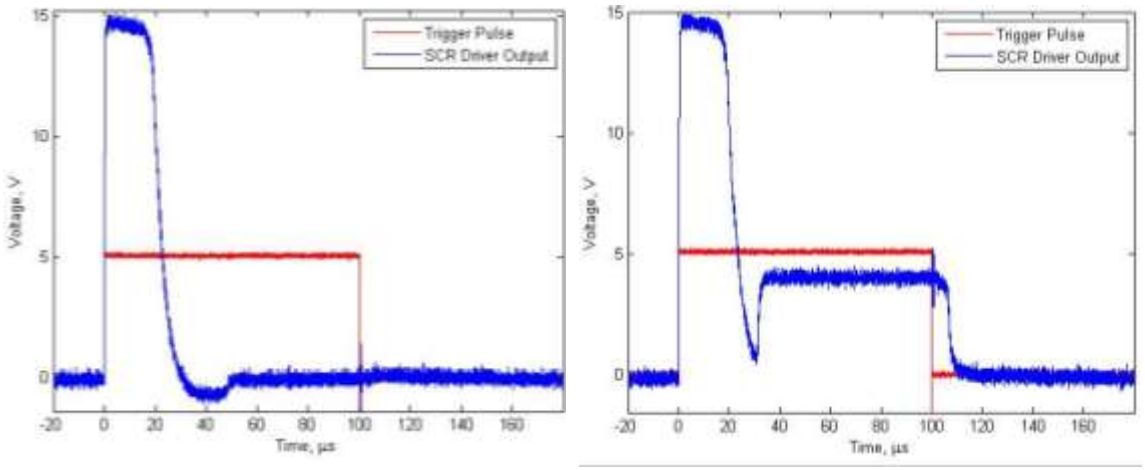


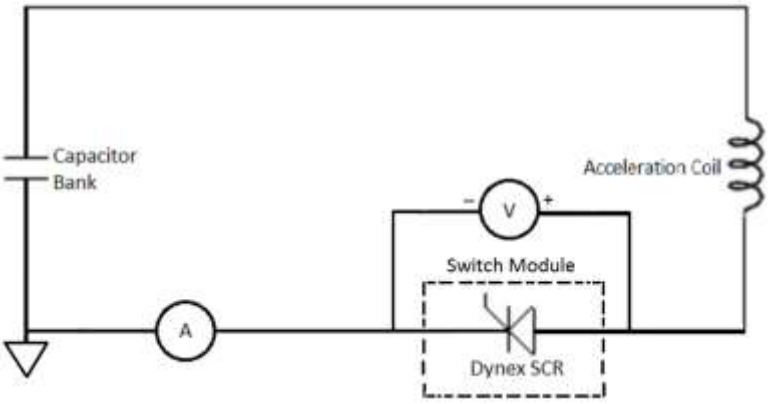
Figure 5-1. SCR driver output pulse. a) With no backporch, the pulse is approximately 20 us long, as fixed by the circuit. b) With the backporch on, the duration of the backporch is set by the length of the trigger. pulse.

This pulse serves to turn the SCR on when it is forward biased. A "backporch" of magnitude 4.2 V can also be added to the circuit in order to maintain carrier injection into the gate and keep the SCR on after the initial current pulse. The length of this backporch is controlled by the length of a pulse output from a BNC pulse generator and fiber optically coupled to the SCR driver. The driver waveforms with and without the backporch are shown in terms of voltage in Figures 5-1a and Figure 5-1b, respectively. The trigger pulse is also shown. As calculated previously, the switch module components are expected to become reverse biased after a period of approximately 10 µs following receipt of the initial trigger signal. It is therefore deemed unnecessary to extend the driver pulse beyond the fixed 20 µs, so that the backporch is omitted.

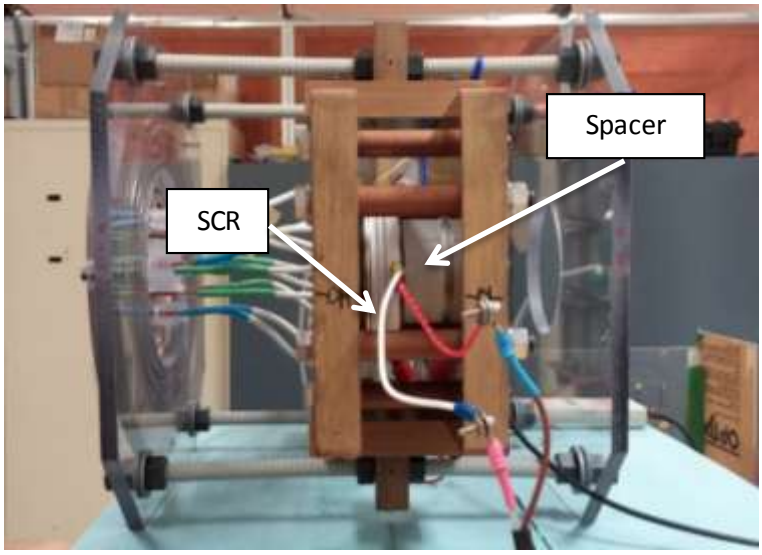
5.1.2 Baseline No-Diode Configuration

In order to provide a baseline against which to evaluate the performance of the Si and SiC diodes in the proposed circuit topology, current and voltage waveforms were collected for a switch module configuration containing only the Dynex SCR with no series FRD. The circuit is

shown schematically in Figure 5-2a, and a photograph of the switch module configuration is shown in Figure 5-2b. The loop current and switch voltage waveforms may then serve as a reference against which the diode latched waveforms are compared. With no diode in the circuit to protect the switch from reverse dv/dt, both shots were taken at relatively low charge voltage (250 V and 300 V) to minimize the risk of damaging the SCR.



a)



b)

Figure 5-2. Baseline No-Diode Configuration. a) The schematic circuit showing the no-diode circuit configuration and measurement points. b) A photograph showing the switch module with no series diode. A steel slug is used as a spacer in place of the diode.

The collected loop current and switch voltage waveforms for a nominal charge voltage of 250 V are shown in Figure 5-3a, while the capacitor voltage, $V_c(t)$, is shown in Figure 5-3b. $V_c(t)$ is calculated from the measured loop current $i(t)$ as

$$V_c(t) = \frac{-1}{C}\int_0^t i(t)dt + V_c(0) \qquad (5-2)$$

where C is the capacitance and $V_c(0)$ is the initial capacitor charge voltage.

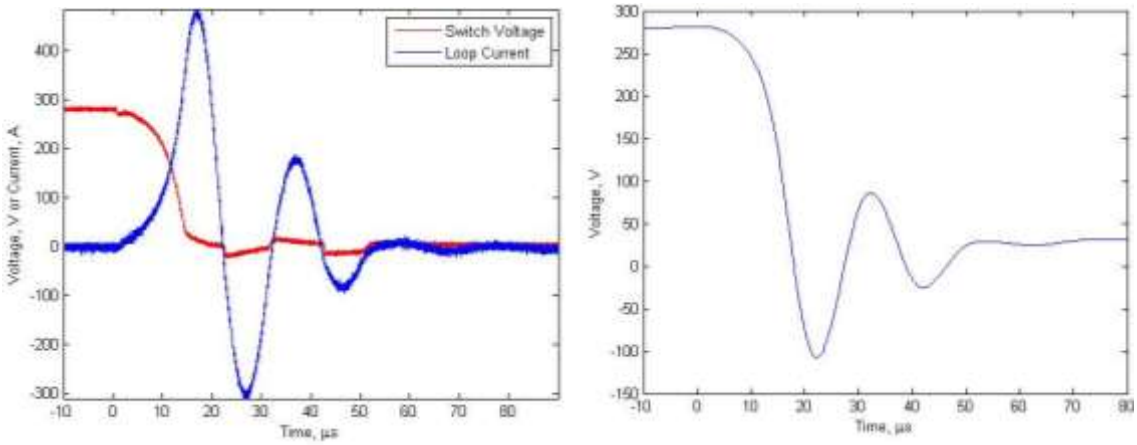


Figure 5-3. Baseline switching waveform. a) The measured switch voltage and loop current waveforms for the no-diode configuration. b) The capacitor voltage calculated from Equation 5-2. The SCR is observed to self-trigger after the gate pulse has been removed.

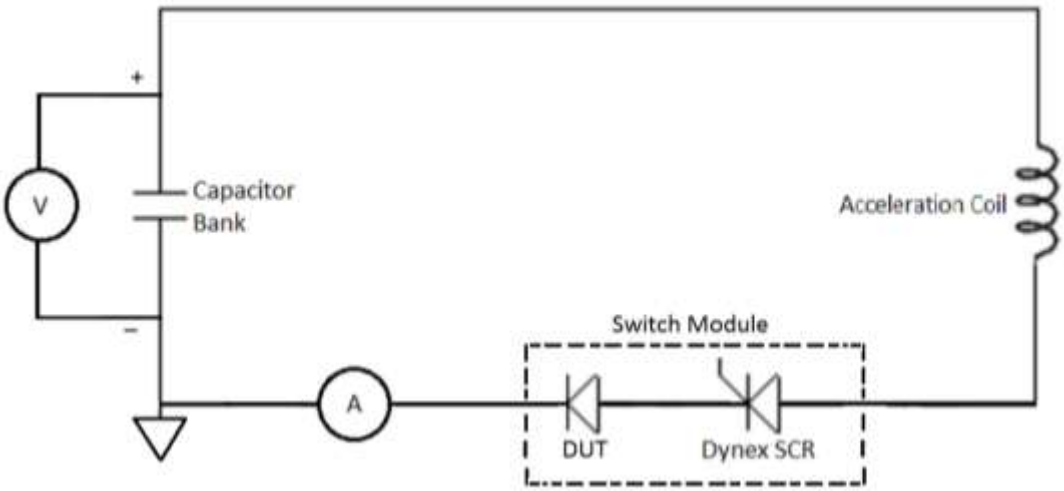
The SCR is observed to conduct even after the initial zero current crossing, and does not permanently return to a blocking state after the 20 µs trigger pulse is removed. This implies self-triggering of the SCR, likely caused by high values of reverse voltage rise rate in the absence of the series FRD. A curve fit of the loop current waveform indicates a total circuit inductance and resistance of approximately 1.24 µH and 58.6 mΩ, respectively. The frequency of the waveform is found to be slightly greater than 45 kHz. For an unclamped configuration with no series FRD, all or nearly all voltage is assumed to be removed from the capacitor bank following a single ringing discharge cycle. In this case, η_r will be very small or zero.

5.1.3 Dynex Si Diode Configuration

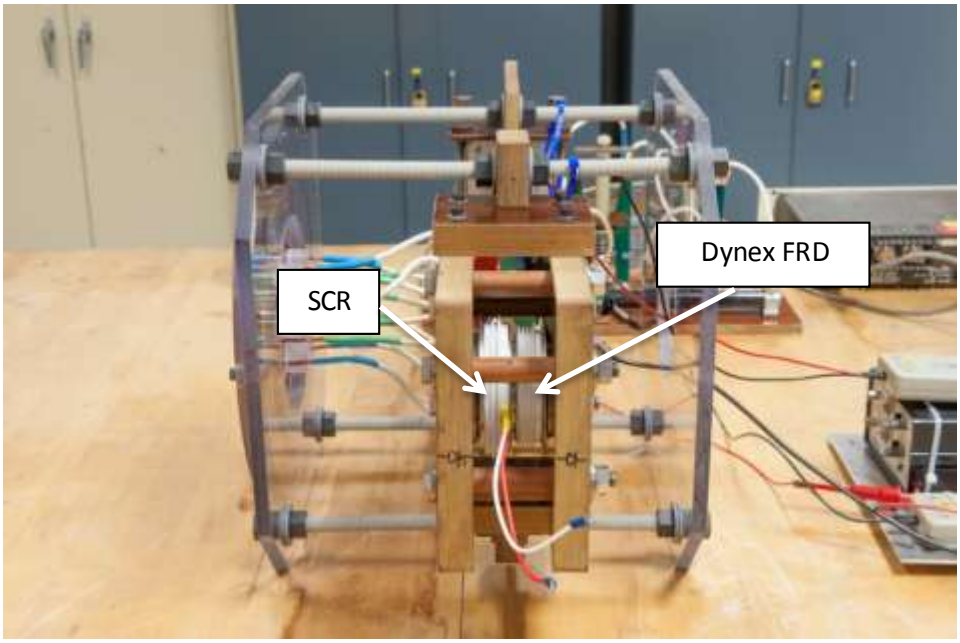
The Dynex Model DSF21545SV diode was purchased specifically to operate as the series diode in the FPT switch module. It is designed for fast turn-on to complement Gate Turn-off Thyristors (GTOs) in inverter circuits, and has an average forward current rating, $I_{F(AV)}$, of 3230 A, which is significantly higher than that of the FRD to be tested. The test setup and several representative waveforms are included here to introduce the operation of the current-cutoff drive circuit topology; however, performance of this diode is not compared with that of the ABB and Cree FRDs.

Current and voltage waveforms were collected at nominal capacitor charge voltages of 250 V, 500 V, and 1 kV. The data allows one to observe the relationship between the reverse recovery response and forward current for the Dynex diode, as well as turn-on characteristics of the SCR. The circuit schematic and physical test setup are shown in Figure 5-4a and Figure 5-4b, respectively.

A representative capacitor voltage and current waveform collected at a nominal charge voltage of 250 V is shown in Figure 5-5. The actual charge voltage is somewhat higher than the nominal (approximately 290 V). The difference between the nominal and actual charge voltage in all cases is due to the low resolution and accuracy of the power supply dial and display, which makes it difficult to obtain an exact voltage value. Comparing Figure 5-5 to Figure 5-3, it is clear that the series diode has the effect of blocking current flow in the circuit following the first zero crossing. A reversal of the current occurs due to the reverse recovery of the diode.



a)



b)

Figure 5-4. Dynex diode configuration. a) The schematic circuit showing the Dynex SCR and Dynex diode circuit configuration and measurement points. b) A photograph showing the switch module with the Dynex series diode.

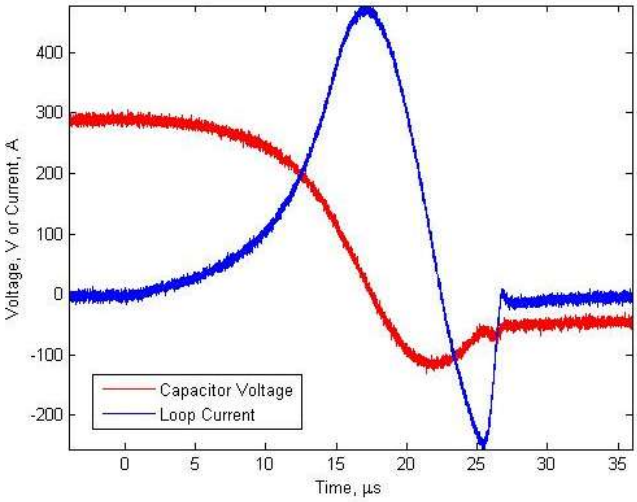
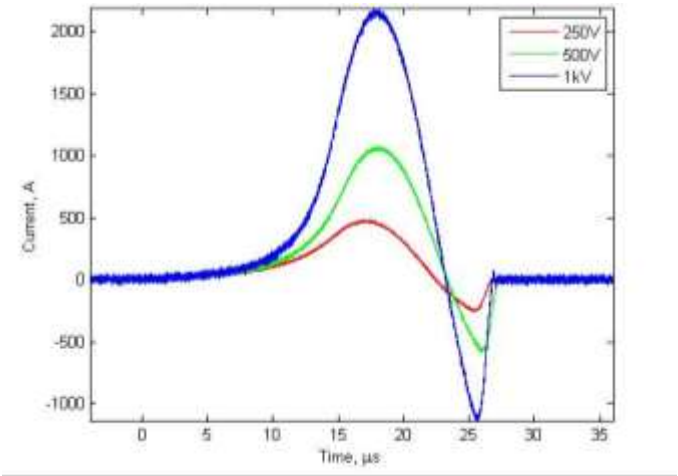


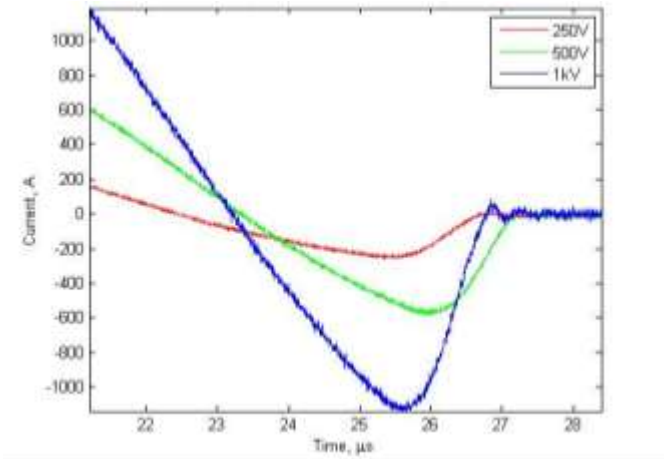
Figure 5-5. Dynex Diode Switching Waveforms. The capacitor bank voltage and loop current are shown on the same figure to demonstrate the effect of the diode reverse recovery on capacitor voltage reversal. The nominal charge voltage is 250 V.

As with the baseline capacitor voltage waveform discussed in Section 5.1.1, a charge voltage remains on the capacitor bank following a discharge cycle. In the case of a diode-containing topology, the remaining charge has negative polarity. The magnitude of the remaining charge for the waveforms show in Figure 5-5 is approximately -45 V, which translates to a recapture efficiency of approximately 2.4%. While this is an improvement relative to the recapture efficiency of the baseline configuration, the large reverse recovery time of the Dynex diode contributes to a significant energy loss in the circuit.

The magnitude of the reverse recovery response- as quantified by peak reverse recovery current, I_{dRM}, (See Section 3.2.2) - is directly proportional to the forward current through the diode prior to turn-off. This can be clearly seen in Figure 5-6a, which shows the loop current waveforms at nominal charge voltages of 250 V, 500 V, and 1 kV. This relationship is due to the higher population of charge carriers in the intrinsic region at higher currents, which means that more carriers must reverse direction and be swept out of the drift region before the device can turn off. Figure 5-6b shows a close-up view of the diode reverse recovery response.



a)



b)

Figure 5-6. Dynex Diode Current Waveforms. a) Higher peak forward current leads to a greater peak reverse recovery current. b) Close-up of reverse recovery curves.

The reverse recovery time does not follow a clear trend for the three charge voltages, which suggests that higher current fall rates compensate for greater peak reverse recovery voltages, essentially switching the diode "harder." This is supported by the steepness of the three reverse recovery waveforms collected.

5.1.4 ABB and Cree Diode Configurations

The circuit schematic and measurement locations for the comparison of the Si ABB diode and Cree SiC diode reverse recovery parameters and their effect on the circuit recapture efficiency are shown in Figure 5-7. The setup differs from the previous setup of the Dynex diode in that the voltage across both the diode and the main SCR switch is measured. As before, the current waveform is captured using a Pearson current transducer, and the capacitor voltage waveform is calculated by integrating this current. A physical view of the ABB Si diode connection is shown in Figure 5-8a, while that for the Cree SiC diode is shown in Figure 5-8b.

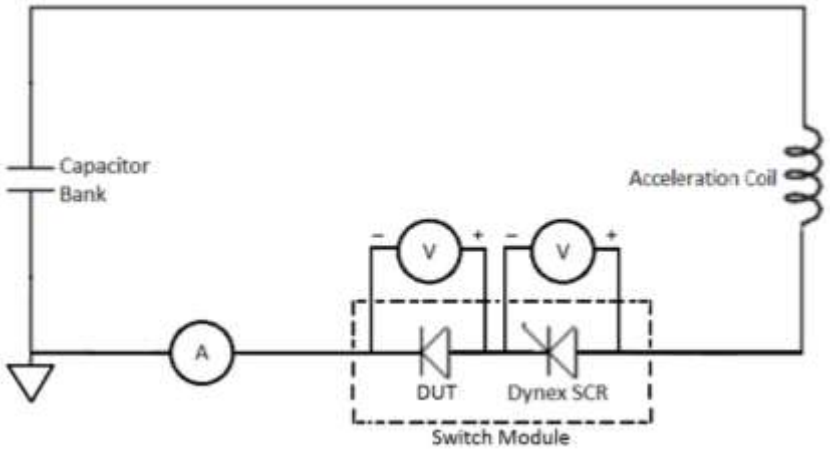
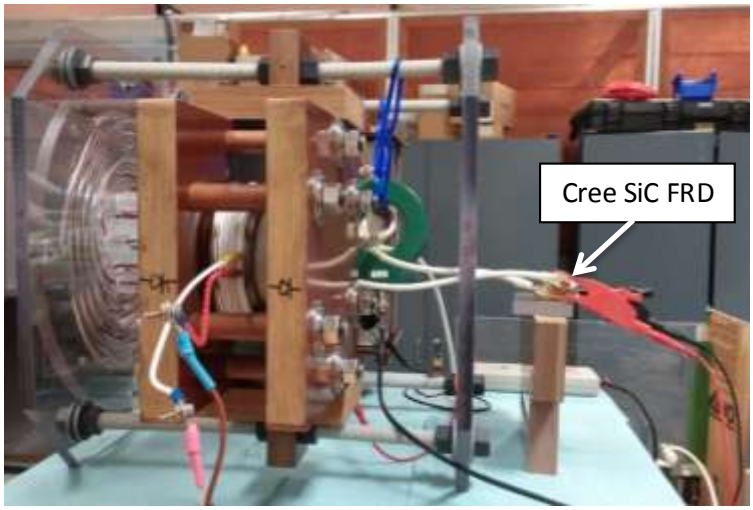
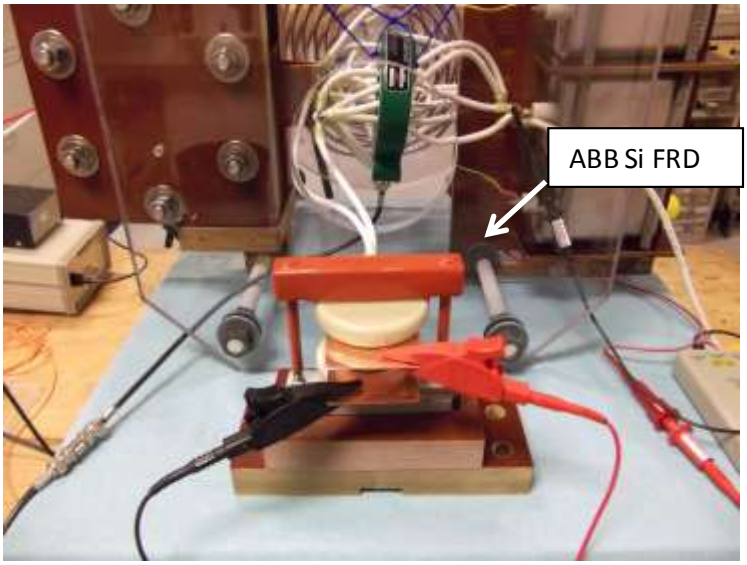


Figure 5-7. Circuit setup for ABB and Cree diode FPT testing.

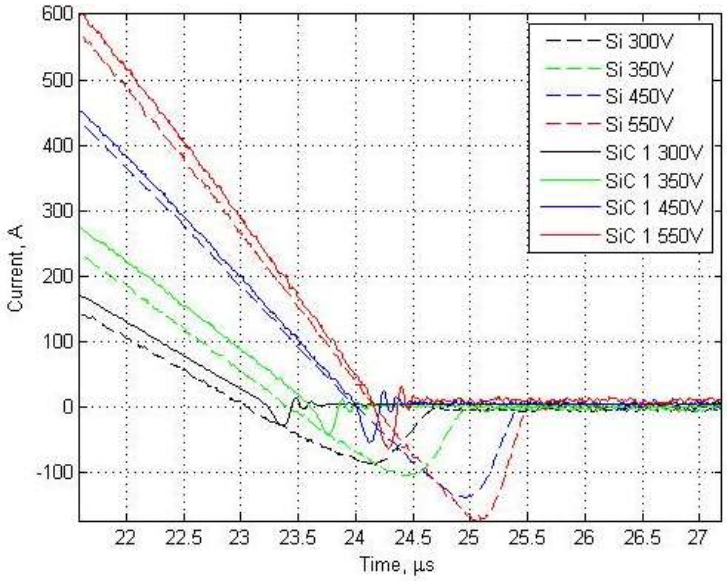


a)



b)

Figure 5-8. Physical views of test diodes in FPT bench top test setup. a) Cree SiC diode. b) ABB Si diode.



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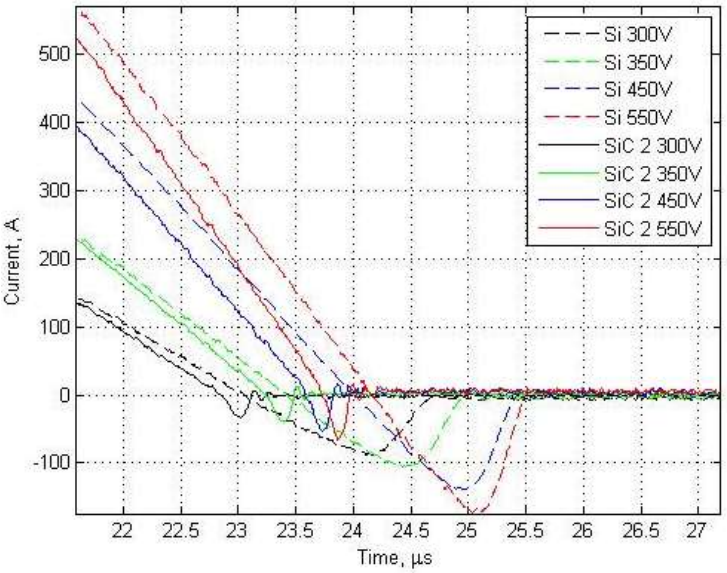


b)

Figure 5-9. Current-dependence of diode reverse recovery. a) ABB Si diode with SiC diode 1. b) ABB Si diode with SiC diode 2.

The current dependence of the diode reverse recovery is shown in Figure 5-9a and Figure 5-9b. As expected, the reverse recovery of the SiC diode is significantly smaller (i.e. shorter reverse recovery time and lower magnitude reverse recovery current) than that of the ABB Si diode for each charge voltage. This result holds for both of the SiC diodes. The slightly greater ringing in

the second SiC diode waveforms following turnoff is likely due to slightly higher stray inductance introduced by the circuit connections. The reverse recovery parameters for all three diodes are tabulated in Table 5-1. The reverse recovery energy, E_{rr}, is once again calculated using a triangular approximation, as discussed in Section 3.2.2.

Table 5-1. Reverse recovery parameters for the ABB Si diode and two units of the Cree SiC diode.

Device Under Test	*Nominal Charge Voltage (V)*	$\mathbf{I_{dRM}, A}$	$\mathbf{t_{rr}, \mu s}$	$\mathbf{Q_{rr}}, \mu C$	$\mathbf{E_{rr}, mJ}$
ABB Si	*300*	88.22	1.66	73.22	7.29
	350	105.5	1.55	81.76	9.87
	450	139.0	1.41	98.00	14.70
	550	172.0	1.32	113.52	21.19
Cree SiC 1	*300*	29.7	0.20	2.97	0.29
	350	42.5	0.25	5.31	0.66
	450	56.0	0.21	5.88	1.18
	550	64.0	0.21	6.56	1.56
Cree SiC 1	*300*	34.2	0.27	4.62	0.45
	350	39.8	0.24	4.77	0.57
	450	52.4	0.24	6.29	0.99
	550	65.8	0.24	7.89	1.83

A clearer picture of the relationship between reverse recovery energy and charge voltage (directly proportional to peak current) for each diode is provided in by Figure 5-10. The reverse recovery energy is significantly higher at all peak currents for the Si diode than for either of the SiC diodes. The two SiC diodes produced very similar results. In addition, the slope of the line of best fit for the Si diode, as opposed to that for the SiC diodes (whose lines of best fit overlap), is higher by an order of magnitude, indicating that the energy loss due to the reverse recovery of the

diode will increase 10 times faster for a given increase in peak forward current for the Si diode than the SiC diodes. The line of best fit for the Si diode is described by the equation $y = 0.026x - 4.2$, while that for the two SiC diodes is described by $y = 0.0023x - 0.64$. The norm of the residuals for the least-squares regression fit are 1.38 and 0.08, respectively.

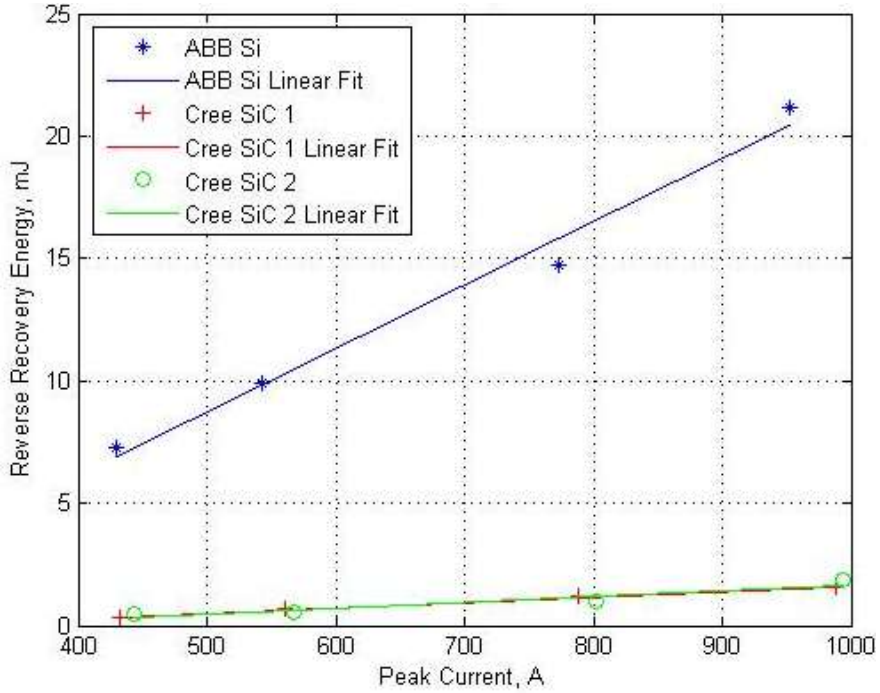
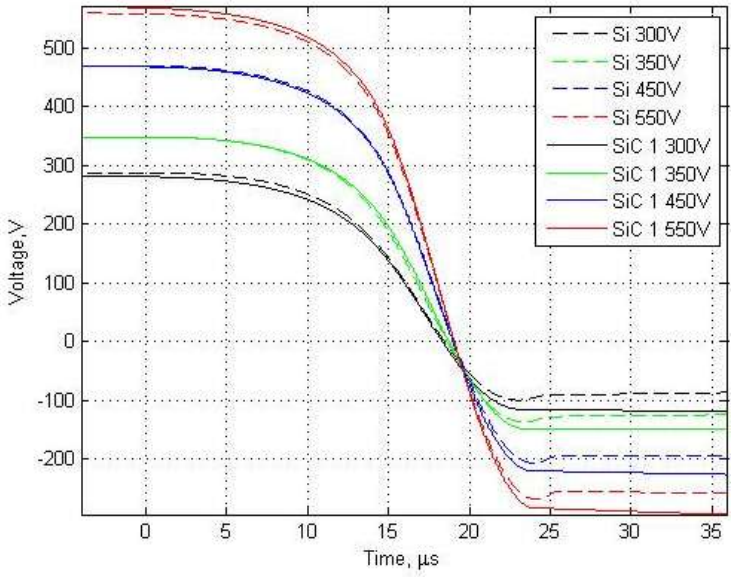


Figure 5-10. Reverse recovery energy loss as a function of peak current for the three diodes tested.

5.2 RECAPTURE EFFICIENCY CALCULATIONS

The recapture efficiency, η_{RC}, was calculated for each of the twelve datasets discussed in Section 5.1.3 using the calculated capacitor waveforms in Figure 5-11, as well as Equations 3-6 and 3-7. The waveforms in Figure 5-11a and Figure 5-11b correspond to the current waveforms in Figure 5-9a and 5-9b, respectively.



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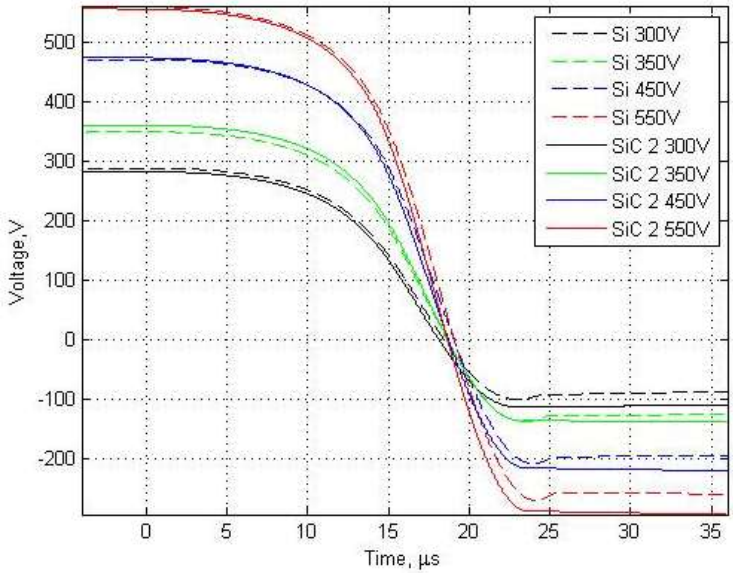

b)

Figure 5-11. Calculated capacitor voltage waveforms. a) ABB Si diode and SiC 1 diode for varying charge voltage. b) ABB Si diode and SiC 2 diode for varying charge voltage.

For each waveform in Figure 5-11, the initial and final capacitor energies, along with the calculated recapture efficiency, are tabulated in Table 5-2. It should be noted that the initial capacitor charge voltage used in the initial energy calculation is the *actual* measured voltage, as opposed to the nominal voltage listed.

Table 5-2. Recapture efficiency parameters for ABB Si diode and two units of the Cree SiC diode.

Device Under Test	*Nominal Charge Voltage (V)*	*Initial Capacitor Energy, mJ*	*Final Capacitor Energy, mJ*	*Recapture Efficiency, %*
ABB Si	*300*	415.45	37.43	9.01%
	350	640.22	77.19	12.06%
	450	1091.25	188.23	17.25%
	550	1549.18	329.85	21.29%
Cree SiC 1	*300*	392.85	70.78	18.02%
	350	598.25	110.41	18.46%
	450	1091.25	253.66	23.24%
	550	1616.29	429.61	26.58%
Cree SiC 1	*300*	387.30	59.67	15.41%
	350	640.22	92.31	14.42%
	450	1105.22	237.36	21.48%
	550	1527.13	423.23	27.71%

Figure 5-12 shows a plot of the percent recapture efficiency as a function of initial capacitor voltage for all three diodes, along with lines of best fit. Some variation was observed between the two SiC diodes, which can likely be attributed the sensitivity of the calculation on the exact initial and final charge voltages, which had to be estimated due to noise present in the measured waveforms. All waveforms were smoothed using a 10^{th}-order moving average filter. The data points clearly demonstrate that the recapture energy was higher at all charge voltages for the SiC diodes as compared to the Si diode.

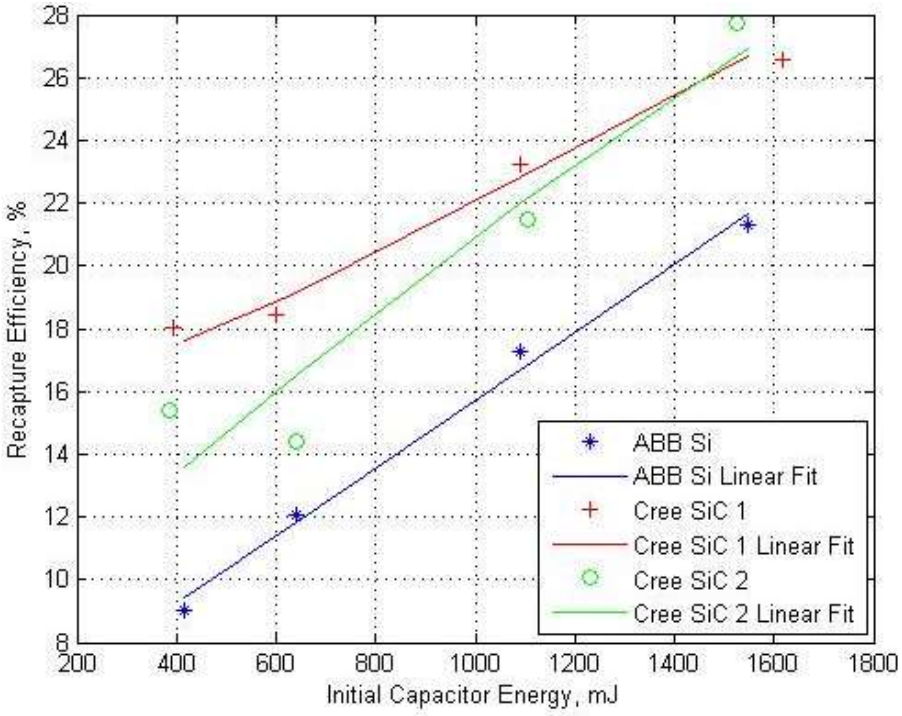

Figure 5-12. Percent energy recapture efficiency as a function of initial capacitor voltage for Si and SiC diodes.

CHAPTER 6
CONCLUSION AND FORWARD WORK

The analysis and data presented in this work point to several important conclusions that have significant implications for IPPT technology, as well as a variety of other fields in which high power semiconductor switching is employed. This, the final chapter, addresses the effects of the findings on IPPT drive circuit design, efficiency, and component lifetime, as well as identified limitations of the proposed drive circuit topology and semiconductor devices. In addition, implications of the results and forward work on the topic are discussed.

6.1 IPPT DRIVE CIRCUIT EFFICIENCY AND OPERATION

The data presented in Chapter 5 supports the assertion that the proposed IPPT drive circuit topology results in less energy wasted as heat in the circuit due to ringing (as opposed to the baseline configuration with no series diode), and consequently more efficient energy utilization and improved thermal management. Both of these are significant advantages in a space environment, where the production of electricity can be costly from both a financial and mass allocation standpoint, and where the lack of convective cooling makes thermal management a serious concern. In addition, the comparison of the Si and SiC FRDs points to a significant advantage in using fast-switching SiC devices for this application. This point is quantified by the data in Table 6-1, which shows a comparison of recapture efficiencies for the baseline configuration, ABB Si diode, and both Cree SiC diodes, as calculated in the previous chapter.

The use of a series Si FRD in the drive circuit results in a maximum recapture efficiency of over 20% for the conditions tested, while SiC diode results in a maximum recapture efficiency approaching 30%.

Table 6-1. Summary of drive circuit recapture efficiencies.

Device Under Test	*Nominal Charge Voltage (V)*	*Recapture Efficiency, %*
No Diode	n/a	~0%
ABB Si	550	22.58%
Cree SiC 1	550	28.93%
Cree SiC 2	550	27.74%

As demonstrated thorough previous analysis and data, this difference is largely due to the superior reverse recovery response of the SiC devices, which stems from the unique material properties of the wide bandgap material used. Although the recapture efficiency definition used does not allow for the distinction between switching and conduction losses, both are inherently captured for each configuration, demonstrating that the *total* losses incurred are lowest for the SiC series FRD topology.

An additional advantage demonstrated through the data present in the preceding chapters is the lower stress experienced by drive circuit components in the proposed circuit topology, versus the baseline configuration. The series diode serves to protect the SCR from high reverse dv/dt, eliminating the need for a separate snubber circuit. The snubber capacitance and resistance in and of itself would lead to longer switching times and additional losses, so there is a compound advantage to excluding one. Fewer components also generally implies reduced complexity and, hence, increased reliability.

Clamping off current in the circuit also prevents stress on the main switch that would be caused by repeated self-triggering and heating that results from the additional on-state and switching losses. Additionally, the lower magnitude of the reverse recovery current observed with the SiC diodes leads to a smaller spike in the main switch current at turn-off, as demonstrated in

Section 3.2.3. The topology minimizes current reversal on the capacitor used, which also reduces stress on these components. Reduce stress may result in improved reliability and extended component lifetimes, reducing the need for redundant systems that are both costly and heavy.

6.2 LIMITATIONS

While there are clearly several significant advantages to the circuit topology and wide bandgap devices proposed, it is important to note several limitations that became apparent over the course of this work. These must be considered when applying the findings to higher power setups or practical spacecraft thruster design.

Primarily, the negative polarity of the final capacitor bank charge voltage in the proposed topology means that the remaining charge is not usable for a subsequent discharge cycle. The remaining charge must first be dumped- potentially used for some useful alternative purpose- and the capacitor bank fully recharged before the next discharge cycle can take place. This issue can be mitigated by either allowing the circuit to ring through one complete current cycle before turning off- which would leave a positive charge on the capacitor bank- or by using a symmetric switching topology such as the Bernardes and Merryman circuit. The former solution would lead to slightly lower recapture efficiency, while the latter would bring an increase in the number of components used, the mass of the system, added complexity, and potentially reduced reliability.

As is, the use of solid state switching components in IPPT circuits as opposed to the spark gap switches used previously has the potential to increase the cost and complexity of the system. Power switches such as IGBTs and thyristors require specialized driver circuits to operate, which may be expensive and to design and build, depending on the availability of COTS drivers. Additionally, wide bandgap semiconductor devices are currently quite expensive [8] as compared to conventional Si devices.

A significant disadvantage of current SiC devices for IPPT switching applications is their relatively low current handling ability. This was demonstrated in Section 2.2.2, where the SiC diodes exhibited unpredictable behavior at current levels greater than 100 A. As discussed, this is likely due to material defects in the devices resulting from immature SiC wafer manufacturing processes, and is expected to improve as the these processes become more developed. It should also be noted that the SiC diodes were found to operate nominally in the FPT circuit up to peak current levels exceeding 1 kA, and may survived up to higher currents. The investigation of the SiC diode current limit is forward work.

Nevertheless, the nominal peak current levels required for IPPT drive circuit applications would currently require SiC devices of this type to paralleled, which would increase complexity and cost. A significant increase in current handling capability would surely be achieved through the use of double-sided cooled compression packaging. Ideally, a high-current rated FRD diode module could be produced for this application containing an array of SiC dies in packaging optimized for thermal management.

6.3 IMPLICATIONS OF RESULTS

As mentioned previously, the increased power utilization efficiency demonstrated through the analysis and experimental results of this work can lead to lower-cost, lighter spacecraft systems that are more reliable and capable of longer-duration spaceflight missions. The reduction in mass that results from smaller electrical power generations systems can free up mass and volume for additional payload and even passengers.

In addition to IPPTs, the technology demonstrated may have implication for other fields that utilize high-power solid state switching, including automotive, rail, and wind power. The demonstrated faster switching and reduction in component stress that comes from the use of a

wide bandgap semiconductor device is universally applicable, and can lead to higher efficiency operation of a variety of switching circuits. Moreover, the concept of clamping off ringing current in a circuit can be applied to a variety of practical resonant *RLC* circuits, such as those employed in inductive energy transfer to a moving load- for example, wireless energy transfer to vehicles passing over a coil imbedded in a road, where current is cut off once the vehicle moves out of range.

6.4 FORWARD WORK

The work described herein was only a first step towards the design of practical, efficient, and reliable solid state drive circuits for in-space propulsion engines. For such a scheme to be a viable option for a flight unit spacecraft, a variety of issues must first be examined and questions answered. These deal primarily with operating power level, the effect of the dummy plasma location on drive circuit operation, integration and testing of the remaining thruster components, testing of the fully assembled thruster in vacuum, and taking repetitive-rate measurements to demonstrate the pulsed operation of the thruster for a large number of pulses.

A logical next step in the process of investigating this type of IPPT drive circuit is to repeat the benchtop testing of the current configuration at high power levels. Now that a basic understanding of the drive circuit operation has been attained, as well as a basic idea of the component limitations, the FPT may be tested at charge voltages up to 4 kV. The testing of a SiC series FRD at these power levels would require paralleling of devices, as well as repackaging for improved thermal management. Higher power benchtop testing will also provide an opportunity to pinpoint and fix any weak spots in the acceleration coil or elsewhere that may breakdown and cause arching. Since vacuum operation would increase the probability of arching, these should be identified prior to vacuum testing.

Integration of the pulsed gas injection valve and preionizer assembly into the FPT and testing of the fully assembled system is a significant step that must be completed before the thruster can be operated in repetitive-rate mode for any number of consecutive pulses. In addition, pulsed operation, particularly in vacuum, could potentially introduce thermal management issues, especially within the switch module components. These would need to be investigated through both analysis and preliminary benchtop testing, and appropriate measures taken to preclude catastrophic component failure.

While a substantial amount of work lies ahead, the results presented and discussed in the preceding chapters are an important stepping stone toward the development of the advanced propulsion systems of tomorrow. Each small step closes the gap between the present and the awesome mystery of alien worlds. After all, as the Italian poet Antonio Porchia said "Set out from any point. They are all alike. They all lead to a point of departure."

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