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Investigation of state retention in metal–ferroelectric–insulator–semiconductor structures based on Langmuir–Blodgett copolymer films

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Among the ferroelectric thin films considered for use in nonvolatile memory devices, the ferroelectric copolymer of polyvinylidene fluoride, PVDF ($C_2H_2F_2$), with trifluoroethylene, TrFE (C_2HF_3), has distinct advantages, including low dielectric constant, low processing temperature, relative low cost compared with epitaxial ferroelectric oxides, and compatibility with organic semiconductors. We report the operation and polarization retention properties of a metal–ferroelectric–insulator–semiconductor bistable capacitor memory element consisting of an aluminum gate, a P(VDF-TrFE) Langmuir–Blodgett film, a 30 nm cerium oxide buffer layer, and a moderately doped silicon wafer. The device exhibited a 1.9 V wide hysteresis window obtained with a ±7 V operating range with a state retention time of 10 min. The mechanisms contributing to loss of state retention are discussed. © *2010 American Institute of Physics*. [doi:10.1063/1.3452331]

I. INTRODUCTION

Demand for nonvolatile memory devices has been growing as many electronic products become more portable and yet more connected by wireless communications.[1] Ferroelectric thin films are promising for nonvolatile memory applications, such as one transistor-one capacitor ferroelectric random access memory (FRAM) (Refs. 2 and 3) and ferroelectric field effect transistors (Fe-FETs).[4–7] Memory elements based on these ferroelectric films have attracted much attention recently because of their lower operating voltages and faster switching speeds than those of flash memory.[8,9] The FET type memory has a number of specific advantages over flash and FRAM, including nondestructive readout and a scalable single device structure.[10] It has been noted that the Fe-FET structure is more promising for applications to high density (gigabit) nonvolatile RAM.[11]

A promising material class for use in nonvolatile memories is ferroelectric polymers, such as polyvinylidene fluoride (PVDF, consisting of $C_2H_2F_2$ monomers) and its copolymers with trifluoroethylene (TrFE, C_2HF_3).[12,13] The VDF copolymers have a large spontaneous polarization, approximately 0.1 C/m^2, excellent polarization stability, and switching times as short as 20 ns.[14] The high resistivity of PVDF and its copolymers, up to 10 Ω cm (Ref. 15), means low leakage, making them suitable for nondestructive readout devices. Further, they require relatively low processing temperatures, less than 200 °C, have outstanding chemical stability, are amenable to low-cost fabrication methods, and are chemically inert and nontoxic.[15] Memory devices based on copolymers of P(VDF-TrFE) provide different opportunities, and face different challenges than those based on ferroelectric perovskites. There have been encouraging demonstrations of nonvolatile memory elements made by adding PVDF copolymer spun films to both silicon[16–18] and organic based devices.[19–22] These copolymer films can be annealed at much lower temperatures and have lower dielectric constants, but their coercive fields can be several orders of magnitude higher than those of the perovskite ferroelectrics. This means that ferroelectric polymer films must be even thinner to enable switching at moderate voltage. We have had much success making high quality ferroelectric films as thin as 1 nm by Langmuir–Blodgett (LB) deposition.[23–26] As the thickness of the ferroelectric layer of the copolymer is reduced in order to decrease operating voltage, careful attention should be applied to the leakage current, which may limit retention times. This study addresses the retention characteristics of silicon based metal–ferroelectric–insulator–semiconductor (MFIS) memory structures[5,16] that incorporate ultrathin ferroelectric copolymer films made by the LB technique.[31]

One proposed form of ferroelectric memory structure is the Fe-FET,[5] which is based on a metal-oxide-semiconductor FET (or MOSFET), with the gate dielectric replaced by a ferroelectric layer (and possibly also a dielectric buffer layer to limit interdiffusion and leakage).[32] The application of a voltage pulse to the gate electrode sets (writes) the direction of the ferroelectric polarization. The surface charge of the ferroelectric film connected with remnant polarization controls the electrical conductance of the semiconductor channel in the same way as the charge on the gate electrode in an ordinary MOSFET. The key difference is that the switchability of the ferroelectric polarization makes the Fe-FET a bistable device with two logic states that are programmable by a voltage pulse of the appropriate sign, while the device state can be sensed (read) without disturbing the ferroelectric polarization, i.e., the readout is nondestructive.

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The main challenge in realizing an Fe-FET memory is to obtain a reliable interface between the ferroelectric and semiconductor layers to limit atomic diffusion through the interface, which can increase the number of interface traps, and consequently degrade device performance.[33] An additional insulating layer can reduce leakage and prevent interdiffusion or reaction of the ferroelectric layer with the semiconductor, but this extra layer should have a large dielectric constant so that its capacitance remains high and it does not drop much of the gate voltage.[10] Although the Fe-FET concept was first introduced over 50 years ago[4] it has not proven suitable for use in nonvolatile memories mainly because the state retention times of prototype devices are generally reported at a few days at best, much less than the 10 year requirement for nonvolatile memory. The 2002 paper by Ma and Han[27] summarizes the challenges and attributes short retention times to two main causes: (1) the tendency of the ferroelectric film to depolarize by breaking up into opposing domains and (2) charge leakage and trapping that tends to screen the polarization charge. The tendency of a ferroelectric film to depolarize is because of the large internal electric field generated by uncompensated polarization.[28–30] In a capacitor the electrodes can provide enough charge to compensate the polarization and thus stabilize it. If one side of the film is bounded by an insulator or semiconductor, then there may be insufficient compensation.[35] It is expected, however, that the self depolarization is not a significant limitation as long as the depolarization field is less than the coercive field, and so relatively little compensation charge may be necessary.[36]

A potentially more serious limitation on state retention is leakage or injection followed by trapping of charges in the gate dielectric or the ferroelectric film. Although the trapped charges can help stabilize the remanent polarization, they screen the semiconductor, which diminishes the effect of the ferroelectric polarization on the FET channel conductance, thus reducing state contrast.[10,27] The leakage time t for a device that has a remanent polarization P_r, leakage current I and trapping probability α, may be estimated from the following relation:[27]

$$t = \frac{P_r}{I\alpha}. \tag{1}$$

This relation suggests that the leakage current should be made very low ($\ll 1$ nA/cm^2), so that typical polarization values in the range from 5 to 50 μC/cm^2 would lead to retention times of many years. It has been proposed that a suitable insulating layer placed between the ferroelectric and gate electrode (as in a metal-insulator-ferroelectric-insulator-semiconductor capacitor) can prevent charge injection from the gate electrode and greatly improve retention characteristics[36] but this will further exacerbate the tendency of the ferroelectric film to depolarize and will also increase the operating voltage.

II. EXPERIMENTAL METHODS

The MFIS samples used in this study each consisted of, in order of preparation, a doped silicon substrate, an oxide insulating layer, a ferroelectric copolymer film, and an aluminum gate electrode. The substrates consisted of moderately doped (<1 Ω cm) silicon wafers, on which was grown either a 100 nm thick silicon oxide insulating layer (on n-type Si) or a 12 nm thick cerium oxide layer grown by reactive rf-sputtering on p-type Si. The ferroelectric Langmuir layer was formed on an ultrapure water subphase using a 0.05% concentration of P(VDF-TrFE) (70:30) in dimethyl sulfoxide. The ferroelectric layer was then compressed to a surface pressure of 5 mN/m at a temperature of 25 °C and deposited onto the substrate using the horizontal (Schaefer variation) in LB deposition, with the film thickness determined by the number of transfers, or nominal monolayers (ML), ranging from 0 to 100 ML for the present study. The LB deposition procedure was described in greater detail previously.[31] Last of all, an aluminum gate electrode was deposited by vacuum thermal evaporation at a chamber pressure of 5×10^{-5} mbar using a Bal-Tec MED 020 coating system. The gate electrodes, which are 0.24 cm^2 in area, were deposited at a rate between 1 and 2 Å/s to a thickness of 100 nm, as determined using a Sycon quartz thickness monitor. The complete MFIS samples were annealed at 120 °C for 1 h in order to improve crystallinity.[31] Electrical contact was made to the silicon substrates with a gallium–indium eutectic applied to a fresh scratch on the back of the wafer.[32] The gate bias voltage cycled in 0.1 V steps at a rate of 0.05 V/s. Sample capacitance was measured with an impedance analyzer (HP 4192A) operating at 1 kHz with amplitude 0.1 V rms. All measurements were made at 25 °C.

III. RESULTS

The total charge trapped in the ferroelectric and insulating layers was determined from the flat-band voltage V_{fb}, the gate bias voltage at which the semiconductor crosses over from depletion to accumulation, using the following expression:

$$V_{fb} = \Phi_{ms} + q_t/C_i, \tag{2}$$

where $\Phi_{ms}=-0.35$ V is the work function difference between the aluminum gate and silicon semiconductor, q_t is the trapped charge, and C_i is the combined capacitance of the ferroelectric and oxide layers and is equal to the capacitance in accumulation. The flat-band voltages for the MFIS samples made with SiO_2 were obtained from the capacitance-voltage (C-V) data like shown in Fig. 1 by locating the elbow of the capacitance curve, where the sloped portion and the accumulation portion tend to meet.[33] The flat-band voltages are summarized in Table I. For example, the 0 ML sample (basically an MOS device) has a shift $V_{fb}=-4.0$ V, and an accumulation capacitance $C_i=6.36$ nF, corresponding to a positive charge with density of 0.10 μC/cm^2 trapped by the oxide layer, most likely caused by dangling bonds at the silicon surface, which is common with unpassivated Si/SiO_2 substrates.[34] The MFIS with 30, 50, and 100 ML LB films had slightly more trapped charge than the 0 ML sample, with the exception of the 50 ML sample, which had less trapped charge. The predominately negative net charge contribution from injection through the

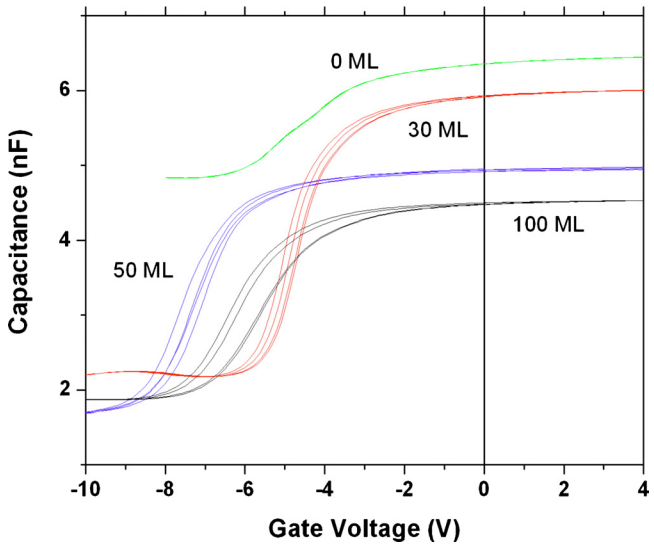

FIG. 1. (Color online) *C-V* data for MFIS devices containing a 100 nm SiO_2 insulating layer on an n-type silicon wafer and a ferroelectric layers with thickness 0 ML, 30 ML, 50 ML, and 100 ML.

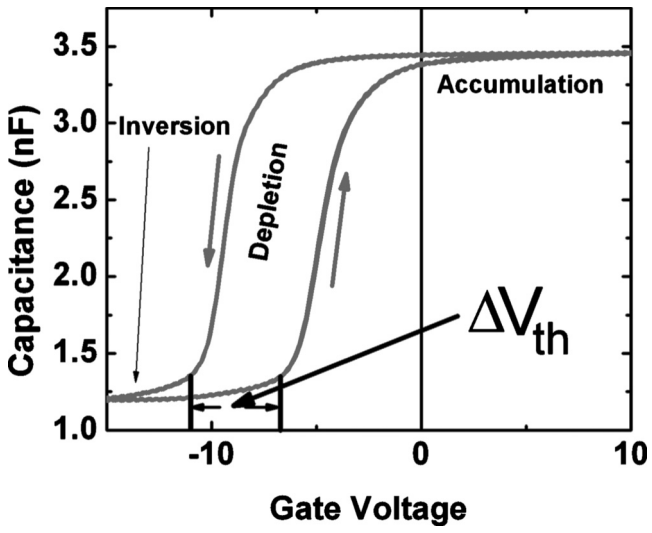

FIG. 2. *C-V* data for an MFIS device containing a 100 nm SiO_2 insulating layer on an n-type silicon wafer and a 100 ML ferroelectric layer. The amplitude of the gate voltage cycle was ±35 V.

ferroelectric layer agrees with previous reported values in the literature.[17,31]

The capacitance of the MFIS device should exhibit counterclockwise hysteresis as the gate bias voltage is cycled, provided that the electric field in the ferroelectric layers is large enough to switch the polarization.[5,16] This hysteresis is evident in the MFIS samples made with silicon oxide insulating layers, as shown in Fig. 1. The 0 ML sample, which lacks a ferroelectric layer and is therefore a conventional MOS structure, has the highest capacitance because it is thinner, and also exhibits no hysteresis. The MFIS structures containing ferroelectric LB films exhibit a memory window on cycling the gate bias with a sufficiently large amplitude to switch the remanent polarization, since the opposite surface charges of the two polarization states cause the threshold voltage to shift in opposite directions. This hysteresis was not observed with the 0 ML MOS sample, indicating that the window is truly due to the spontaneous polarization of the ferroelectric layer. The bias voltage was cycled twice for each sample to demonstrate repeatability.

To better understand the mechanisms limiting state retention, we next focus on the modes of operation of an MFIS device consisting of a second 100 ML LB 70:30 film (approximately 180 nm thick)[35] made on a 100 nm SiO_2 insulating layer and n-doped silicon wafer. The hysteresis loop for a bipolar gate bias voltage sweep amplitude of 35 V is shown in Fig. 2. (The plot shows the region where the depletion layer thickness changes significantly as the semiconductor surface changes from accumulation to depletion and vise versa. Outside this region, on either side, the capacitance is nearly constant, high in full accumulation at positive gate bias voltage and low strong inversion at negative voltage. Although the dc device capacitance should be high in either accumulation or strong inversion, the minority carrier response is too slow to respond to the 1 kHz measurement frequency, so the measured capacitance remains low even in strong inversion, for gate bias voltage below −10 V.) A sufficiently large positive gate bias voltage switches the ferroelectric film to a polarization state that induces majority carrier (negative for n-type doping) charge accumulation at the silicon surface. Therefore, this polarization state favors the accumulation mode and a larger negative gate voltage is required to reach the threshold V_{th}, the voltage at which the depletion layer reaches maximum thickness and the device capacitance is at a minimum. Conversely, when the large negative gate voltage is applied to the sample, the ferroelectric polarization switches to the state that induces minority carrier charge at the interface (inversion), and threshold occurs at a less negative gate voltage. The counterclockwise sense of the hysteresis loop in Fig. 2 is, therefore, consistent with ferroelectric switching. If the hysteresis was due to charge injection from the gate, it would have a clockwise

TABLE I. Device characteristics used to determine the trapped charge density for the SiO_2 MFIS samples.

Polymer film thickness (ML)	Capacitance in accumulation C_i (nF)	Flat band capacitance C_{fb} (nF)	Flat band voltage V_{fb} (±0.05 V)	Total trapped charge density q_t/A ($\mu C/cm^2$)	Net trapped charge density vs 0 ML sample ($\mu C/cm^2$)
0	6.4	5.78	−4.0	+0.10	
30	5.9	5.42	−3.5	+0.08	−0.020
50	5.0	4.60	−5.5	+0.11	+0.010
100	4.5	4.19	−4.1	+0.08	−0.023

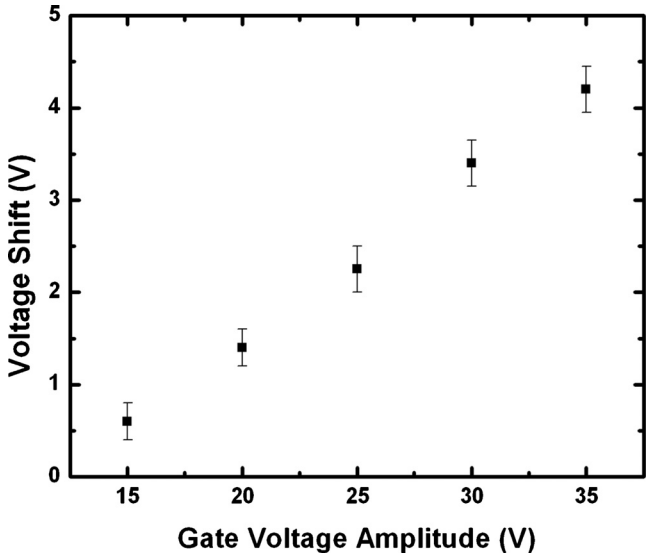

FIG. 3. Dependence of memory window voltage shift on gate voltage amplitude for an MFIS device containing a 100 nm SiO_2 insulating layer on an n-type silicon wafer and a 100 ML ferroelectric layer.

sense (for an n-type semiconductor).[34] As noted above, the MFIS devices with SiO_2 had a fixed positive trapped charge density. As further test, we heated the sample above the ferroelectric–paraelectric phase transition temperature where the hysteresis vanished as it should in the nonpolar paraelectric phase.[33]

A convenient way by which to determine the width of the memory window is to measure the voltage separation between intersecting points in the slope dC/dV of the capacitance curve.[33] In this case, the measured width of the memory window width was 4.2 V. The maximum width of the memory window should be twice the coercive voltage of the ferroelectric layer,[36] or about 21 V for a 100-ML LB film of this polymer,[37] much larger than that shown in Fig. 3. This suggests that the polarization of the ferroelectric layer was not saturated and that significantly larger operating voltage is required. Increasing the range of the operating voltage did indeed increase the width of the memory window, as shown in Fig. 3 but even cycling between ± 35 V did not appear to achieve saturation. The device capacitance data described in Sec. II demonstrated that the two different polarization states of the ferroelectric produced a large change in the surface potential and flat band voltage of the n-type semiconductor even when the polarization states were not saturated. The stability of those states, however, needs to be addressed especially because of the lack of saturation. The method for investigating state retention in 100 ML MFIS devices was accomplished in the following manner. First, a +35 V dc gate bias voltage was applied to the MFIS for 15 s to set the arbitrarily designated "OFF" device state. Then, after the gate was set to a suitable holding voltage, the capacitance was monitored over time for approximately an hour. Then the process was repeated with a -35 V bias voltage for 15 s to set the complementary "ON" state. In the figure, the higher capacitance (accumulation) state induced after applying +35 V is referred to as the OFF state, because within the Fe-FET structure, this state would induce higher resistance in the channel than the lower capacitance (strong inversion) ON state obtained after application of -35 V would. In the case of the -3 V holding voltage, the states quickly converge at the accumulation capacitance, the OFF state.

For truly nonvolatile memory, retention studies should be made at zero gate bias voltage. But, because of the large negative shift in the flat-band voltage due to charge trapping (see also Fig. 1 and Table I), for state retention studies the capacitance was monitored at negative holding voltages, where the hysteresis was significant. Figure 4 shows the retention data for a 100 ML film for different values of the holding voltage: (a) -3 V, (b) -6 V, and (c) -9 V. The small holding voltage of -3 V is to the right of the flat band voltage and does not completely compensate for the trapped charge and the external field across the ferroelectric is positive, which maintains the OFF state and switches to the ON state over time. The opposite situation occurs at the -9 V holding voltage, which overcompensates for the trapped charge and leaves a negative field in the ferroelectric film. Both states quickly converge to the ON state in this case. Since the -6 V holding voltage is closer to the center of the hysteresis loop and therefore to exact compensation to the trapped charge, the two capacitance states are discernible for the longest amount of time at this holding voltage—the retention is best. In this case, the capacitance difference between the two states drops to 56% of its initial value after approximately 1 h. Therefore, the device has a state retention time of approximately 1 h, but only at a holding voltage of -6 V.

The MFIS leakage current density (Fig. 5) was low throughout the operating range, less than 10 nA/cm^2, which is comparable to the leakage of the MFIS structures based on perovskite ferroelectrics.[38] We can estimate a lower limit on the time it takes to compensate the polarization charge, and, therefore, the minimum retention time if leakage alone is responsible for loss of state contrast. This minimum retention time due to leakage would be equal to the remanent polarization (>1 $\mu C/m^2$) divided by the product of the leakage current (<2 nA/cm^2 at -10 V) and the trapping probability. The retention time would range from more than 500 s for unity trapping probability to over 50 days for a more reasonable probability of 10^{-4}. The measured retention of approximately 1 h is closer to the lower end of this range, where trapping probability is close to one, an unlikely situation, which suggests leakage is not the limiting factor. Therefore, either the trapping probability in the LB film is large or the remanent polarization is much lower than estimated, or both.

Since it is more difficult to saturate the polarization of the thick LB films, which have larger coercive voltages,[39] on a thick silicon oxide layer, which will drop a large proportion of the gate bias voltage, the next logical step is to reduce the thicknesses of both layers while increasing the dielectric constant of the insulating layer. This should ensure that the operating voltage is reduced while supplying a larger percentage voltage drop across the ferroelectric layer and provide a better blocking barrier to charge injection from the silicon. For this reason, we made MFIS structures on moderately doped p-type silicon wafers (1–10 Ω cm) and high-k insulating layers, cerium oxide ($\varepsilon_{ins} \approx 26$). In general, high-$k$

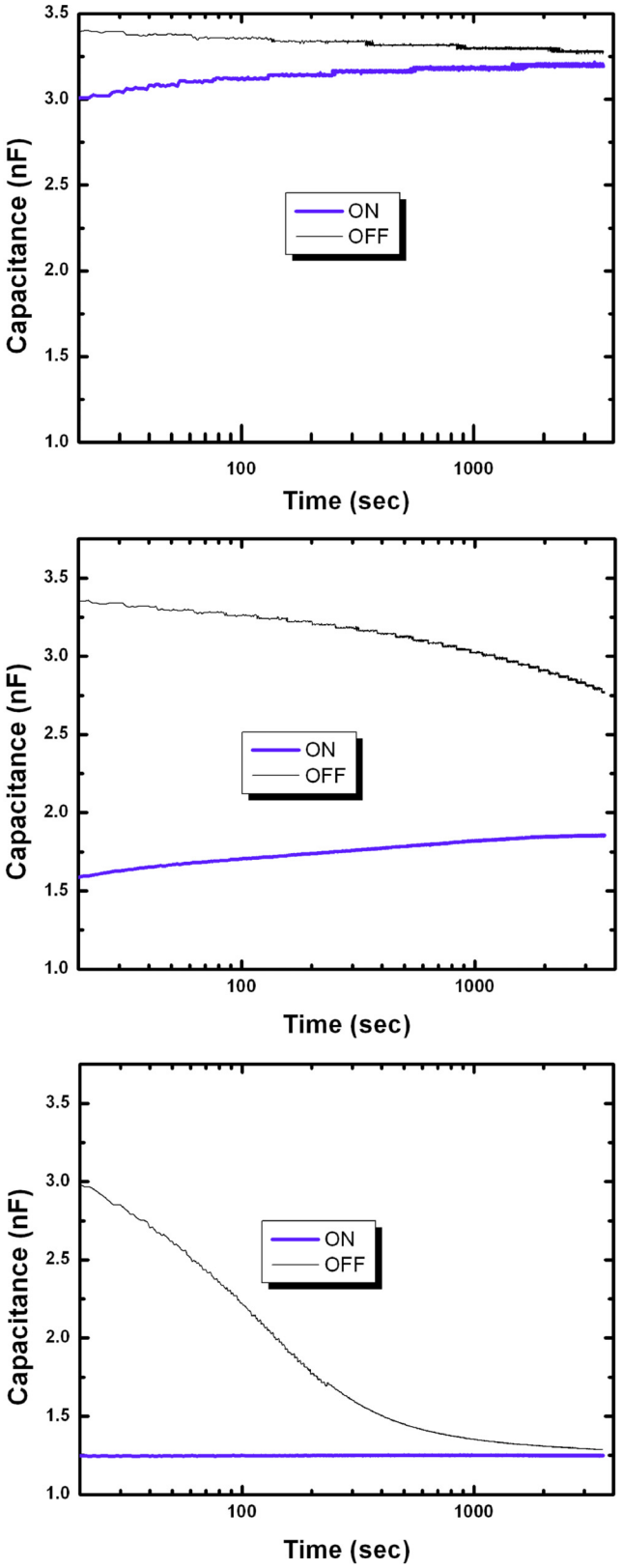

FIG. 4. (Color online) Retention measurements at holding voltages of −3 V (top), −6 V (middle), and −9 V (bottom) for an MFIS device containing a 100 nm SiO_2 insulating layer on an n-type silicon wafer and a 100 ML ferroelectric layer.

MFIS structures fabricated under the same conditions as the thick silicon oxide structures using these substrates resulted in large capacitance memory windows even at gate voltages lower than 5 V and lower shifts in the flat band voltage due

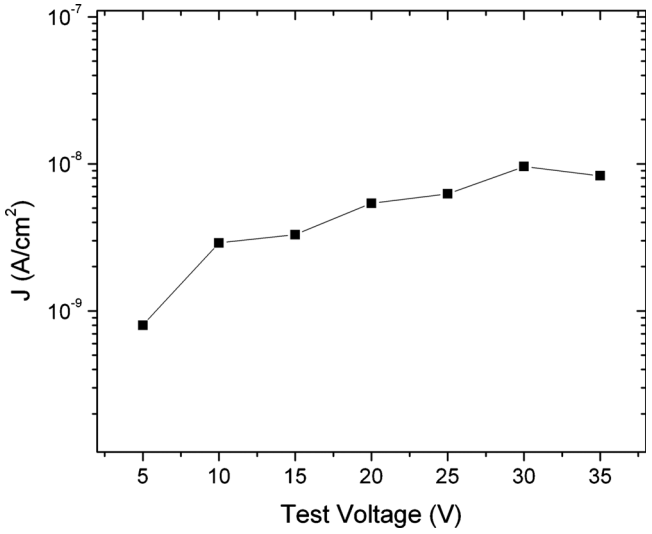

FIG. 5. Current density characteristics through an MFIS device containing a 100 nm SiO_2 insulating layer on an n-type silicon wafer and a 100 ML ferroelectric layer.

to reduced effective trapped charge in the insulating layer. The leakage current densities measured through these capacitors were, however, considerably higher ($>10^{-6}$ A/cm^2) than for silicon oxide barriers and significant charge injection occurred before gate voltages large enough to saturate the ferroelectric could be reached.

Figure 6 shows the capacitance hysteresis for two cycles of a 15 ML 65:35 LB copolymer film deposited on 30 nm of cerium oxide and a p-type silicon wafer. The bistability of the ferroelectric layer now causes clockwise hysteresis and shows accumulation at negative gate bias. Further, there is little horizontal offset as indicated by the centered hysteresis loop, indicating the low density of dangling bonds for trapping sites. The gate bias voltage sweep range in this case was only ±5 V, yet the memory window was 1.1 V, already 1/3 of the expected value of 3.9 V (twice the coercive voltage of a reference 15 ML metal-ferroelectric-metal structure[37]). Fig-

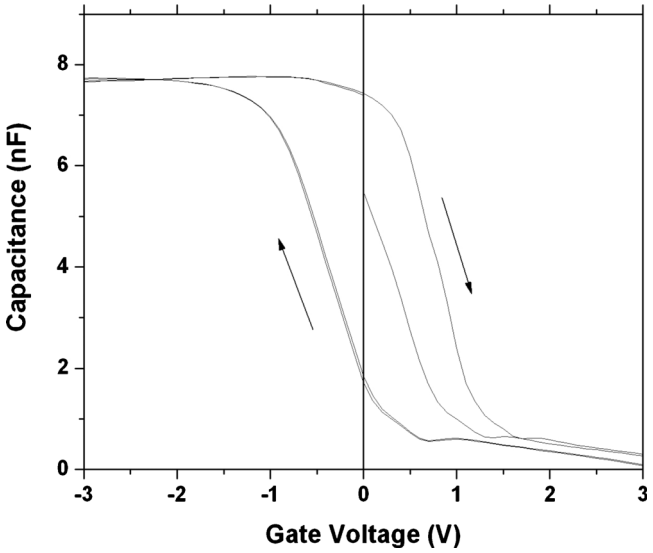

FIG. 6. *C-V* loop for an MFIS device containing a 30 nm CeO_2 insulating layer on a p-type silicon wafer and a 15 ML ferroelectric layer.

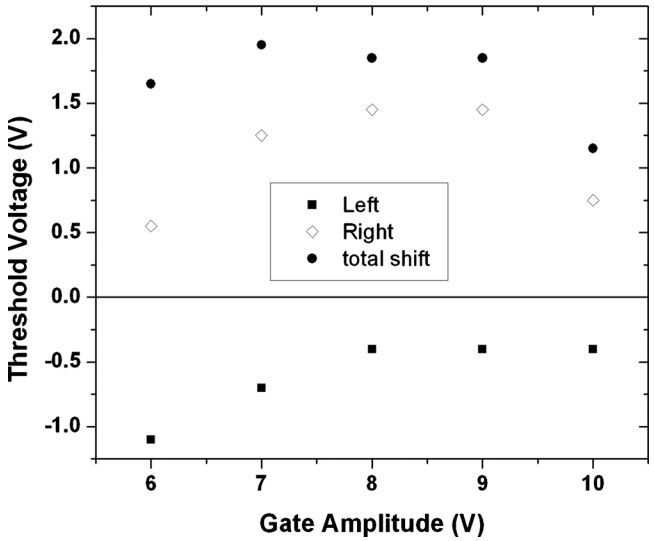

FIG. 7. Threshold voltages and memory window for an MFIS device containing a 30 nm CeO_2 insulating layer on a p-type silicon wafer and a 15 ML ferroelectric layer.

ure 7 shows, however, that when the gate amplitude was increased, the hysteresis window achieved its maximum value of 1.9 V (more than half of the theoretical saturated value) at a gate amplitude of ±7 V, while after cycling to higher gate voltages, the size of the window began to decrease. Furthermore, both of the threshold voltages show a trend of shifting toward positive gate bias, an indication that negative charge is being trapped in the oxide layer during cycling.

The stability of the polarization states was monitored in the same manner described above. Since the ON/OFF ratio was large at zero bias, in this case the capacitance was monitored over time with the gate under short circuit boundary conditions, a more appropriate condition for nonvolatile memories. Figure 8 shows the OFF or accumulation capacitance state and its dependence on time after two applications of −6 V pulses with different time durations. The process was also performed for the ON state, but for simplicity that data is not shown since in this case the ON state was stable for at least 3 h, due to the small offset at zero gate voltage. Although the large memory window of the capacitance loop shown in Fig. 6 indicates that the ferroelectric film was brought closer to saturation when compared to the earlier studies on thick MFIS structures, there is little improvement in the retention time compared to the devices with an SiO_2 insulating layer. Even so, there is evidence that incompletely polarized ferroelectric polymer LB films continue to relax on a logarithmic time scale.[40] This means that there is much yet to learn about polarization relaxation processes.

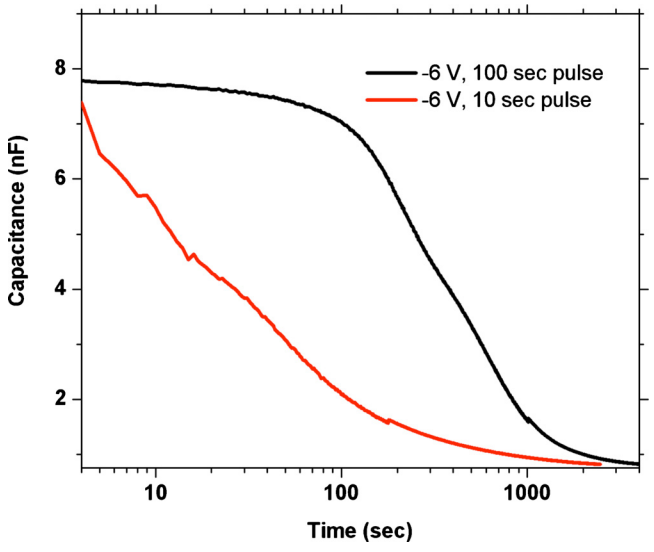

FIG. 8. (Color online) Retention of the accumulation state at zero gate bias voltage following −6 V poling pulses of 10 and 100 s duration for an MFIS device containing a 30 nm CeO_2 insulating layer on a p-type silicon wafer and a 15 ML ferroelectric layer.

In order to test the insignificance of the depolarization field, a comparison study was made between two different ferroelectric capacitors, both with aluminum electrodes and a 40 ML (72 nm) thick copolymer LB film. One of the samples had, in addition, a 5 ML thick (12 nm) stearic acid LB film deposited on top of the copolymer layer. The stearic acid layer was included to produce a nonzero depolarization field, comparable to that produced by the oxide layer in the MFIS. The pyroelectric signals of both samples were monitored after a 10 s saturation pulse at 1.5 times the coercive voltage was applied. 8 h after the pulse application, both samples retained high polarization, the sample with a stearic acid layer had reduced to 92% of its initial value and the other sample was at 95% of its initial value. Other studies have also observed that the depolarization field is not an important factor for polarization retention of devices based on the ferroelectric copolymer.[41]

These results demonstrate that in order to reduce operating voltages and to better saturate the ferroelectric, much thinner LB films were deposited on silicon substrates that had thin buffer layers with high dielectric constants. These structures resulted in repeatable hysteresis at lower voltages and better ON/OFF ratios at zero bias, which is necessary for a nonvolatile memory. State retention, however, was limited by the relatively large leakage currents produced in these configurations. In order to decrease operating voltages and maintain acceptable current densities, it may be necessary to deposit a second high-*k* buffer layer between the ferroelectric and gate metal while investigating methods to improve overall crystallinity in the LB polymer films.

IV. CONCLUSIONS

The device characteristics of MFIS structures incorporating thick LB copolymer films on thick silicon oxide show that the polarization of the thick ferroelectric MFIS was not well saturated, even when operating voltages as high as ±35 V were applied. The limited retention time of the copolymer based devices suggested that the trapping probability is high but it remains to be seen if retention is limited by leakage or if it is caused by an unsaturated state of the ferroelectric.

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