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Real-Time Internal Temperature Estimation and Health Monitoring for IGBT Modules

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REAL-TIME INTERNAL TEMPERATURE ESTIMATION AND HEALTH MONITORING FOR IGBT MODULES

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REAL-TIME INTERNAL TEMPERATURE ESTIMATION AND HEALTH MONITORING FOR IGBT MODULES

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Field experiences have demonstrated that power semiconductor devices, such as insulated-gate bipolar transistors (IGBTs), are among the most fragile components of power electronic converters. Thermomechanical stresses produced by temperature variations during operational and environmental loads are the major causes of IGBT degradation. As the devices are often operated under complex working conditions, temperature variations and the associated damage are difficult to predict during the converter design stage. A promising approach—online health monitoring and prognosis for power semiconductor devices—that can avoid device failure and effectively schedule maintenance has attracted much interest.

This dissertation research focused on real-time accurate internal temperature estimation and health condition monitoring for IGBT modules, where real-time means negligible latency. The objectives of this dissertation research were to: 1) develop low-computational-cost thermal models to accurately estimate important internal

temperatures, e.g., junction temperature, in real time for better device overtemperature protection and lifetime prediction; and 2) invent a practical technique to monitor the major aging processes of IGBT modules for effective maintenance scheduling.

To achieve the first objective, this research developed a cost-effective, physics-based thermal equivalent circuit model and a low-order digital filter-based thermal model for IGBT modules. Further, a thermal model adaptive to the solder crack of an IGBT module was developed. This model allows accurate junction temperature monitoring over a device's lifespan. Additionally, an accurate, frequency domain, transient temperature estimation method for weak points of IGBT modules was developed. The method can be used to determine the bottleneck weak point(s) of IGBT modules. The accurately estimated internal temperatures can be used for more effective operation management of power electronic converters and a more accurate estimation of a device's remaining useful lifetime (RUL).

To achieve the second objective, a new method of using two-dimensional (2D) case temperatures for real-time monitoring of typical weak points, i.e., bond wire and solder interface, of IGBT modules was invented. This method is based on the physics of failure of IGBT modules and can easily be implemented without complex circuitry. Compared with existing methods, the proposed method is simple to use and does not interrupt the operation of power electronic converters.

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Table of Contents

List of Figures

List of Tables

List of Acronyms/Initialisms/Nomenclature

A. Acronyms/Initialisms

1D	one-dimensional
2D	two-dimensional
3D	three-dimensional
AlN	aluminum nitride
CTE	coefficient of thermal expansion
DBC	direct bonded copper
DC	direct current
DFT	discrete Fourier transform
EHPP	effective heat propagation path
FEA	finite element analysis
FIR	finite impulse response
FFT	faster Fourier transform
FWD	free-wheeling diode
HEV	hybrid electric vehicle
IC	integrated circuit
IGBT	insulated-gate bipolar transistors
IHCP	inverse heat conduction problem
IIR	infinite impulse response
LESIT	Leistungselektronik, Systemtechnik und Informationstechnologie

LTI	linear time invariant
MOSFET	metal-oxide semiconductor field-effect transistor
NI	National Instruments
PRBS	pseudo random binary sequence
PF	power factor
PSU	power supply unit
RC	resistor-capacitor
RUL	remaining useful lifetime
TEC	thermal equivalent circuit
TO	transistor outline
TSEP	temperature-sensitive electrical parameter

B. *Nomenclature*

α	thermal diffusivity
α_{adj}	heat spreading angle in the substrate copper layer needs to be adjusted during substrate solder cracks
$\Delta\alpha_{CTE}$	the difference between the CTEs of two different materials
α_f	a constant in lifetime model (1.4)
α_P	the ratio between actual power loss $P_{loss}(T_J)$ and estimated power loss $\hat{P}_{loss}(\hat{T}_J)$
θ	heat spreading angle in degree
$\varepsilon_{mismatch}$	the strain at the interface between two different materials
ε_p	plastic strain
ε'_f	fatigue ductility coefficient
ε_e	elastic strain
σ_a	alternating stress
σ'_f	fatigue strength coefficient
τ_{iF}	time constant of the i_{Foster}th RC pair
$A(z)$	horizontal cross-section area at the distance z
A_c	area of the EHPP through the bottom surface of the ceramic layer
A_f	a constant in lifetime model (1.4)
A_{hot}	baseplate hot area
$A_{IIR}(z)$	coefficient in an IIR filter

A_r	remained non-cracking area in the substrate solder layer
b_f	fatigue strength exponent
$B_{IIR}(z)$	coefficient in an IIR filter
CE_{lc}	lumped–capacitance approximation error
$CE_{lc,i,sub}$	lumped-capacitance approximation error of each sublayer
c_f	fatigue ductility exponent
C_f	normalized total damage in one operation cycle
C_{th}	thermal capacitance
$C_{th}(z)$	distributed heat capacitance at vertical distance z
$C_{th,i}$	lumped thermal capacitance of the ith layer
$C_{th,iF}$	thermal capacitance of the i_{Foster}th RC pair
$C_{th,tot}$	total thermal capacitance of the IGBT module
c_v	volumetric heat capacity
c_{vbp}	volumetric specific heat of the copper baseplate
d_{bp}	thickness of the baseplate
d_i	thickness of the ith layer
d_l	thickness of a layer
$d_{pattern}$	thickness of the substrate copper pattern layer
E	Young's modulus
E_a	activation energy
f_{sw}	switching frequency
F^{-1}	inverse Fourier transform

$H(z)$	transfer function of an IIR filter
H_{nm}	frequency response of the temperature rise from the nth junction to case excited by the mth source power loss P_m
$H_{nn}(z)$	IIR filter charactering the self-heating of the nth chip
$H_{nm}(z)$	IIR filter charactering the relationship between junction temperature of the nth chip, T_{jn}, and power loss of the mth chip
$h_{pj}(t)$	high-order LTI system characterizing relationship between junction-to-case temperature difference $\Delta T_{jc}(t)$ and power loss $P_{loss}(t)$
$h_{pj}[k]$	discrete-time form of $h_{pj}(t)$
$H_{pj}(e^{j\omega})$	frequency response of $h_{pj}(t)$
$H_{pj}(\Omega)$	frequency response of $h_{pj}[k]$
$h_{QD}(t)$	time derivatives of thermal impedance $Z_{thjcQD}(t)$
$h_{QQ}(t)$	time derivatives of thermal impedance $Z_{thjcQQ}(t)$
i	index for the layers from top to bottom in IGBT modules
I_c	collector current
i_{Cf}	index for different junction temperature swing ΔT_j in one operation cycle
i_F	index of RC pairs in a Foster-type TEC
$\mathbf{J}$	matrix of ones
k	thermal conductivity

k_B	Boltzmann constant
k_{bp}	thermal conductivity of the copper baseplate
k_{cs}	ratio between equivalent thermal resistance $R_{eqCchip}$ and equivalent thermal resistance $R_{eqCside}$
k_{dt}	index for discrete-time sequence
k_{hc}	the ratio between equivalent thermal resistance R_{eqCc} and equivalent thermal resistance R_{eqCc}
K_{sp}	number of the time-domain data samples of the power losses
$n_{f,i}$	cycle occurrence of the i_{Cf}th ΔT_j
N_{cf}	number of different junction temperature cycle amplitudes
N_f	number of cycles to failure
$N_{f,i}$	number of cycles to failure for the i_{Cf}th ΔT_j
N_l	order of a LTI system
N_{rc}	order of an RC TEC
N_{sub}	number of sublayers
P_{ce}	point at the free edge of the chip solder layer
P_{Closs}	conduction loss
P_{flux}	heat flux
P_{loss}	total power loss
$P_{loss}[k]$	discrete time power loss
$P_{loss}(\Omega)$	discrete Fourier transform (DFT) of $P_{loss}[k]$

$\hat{P}_{loss}(\hat{T}_j)$	calculated power loss at estimated junction temperature $\hat{T}_j$ using healthy device parameters
P_{jm}	point at the middle of junction
P_n	power loss of the nth chip
P_{se}	point at the free edge of the substrate solder
P_{SWloss}	switching loss
$q(z)$	heat flow
Q_i	amount of heat stored in the ith layer
$\mathbf{R}_{eqC}$	matrix of the equivalent thermal resistances from the points of interest on the 2D bottom surface of the baseplate to ambient
R_{eqCc}	an element in the matrix $\mathbf{R}_{eqC}$ for a cold spot
R_{eqCh}	an element in the matrix $\mathbf{R}_{eqC}$ for a hot spot
R_{eqcp}	equivalent thermal resistance characterizing the temperature rise from ambient to any point p
$R_{eqCchip}$	equivalent thermal resistances between the selected point right underneath chip and ambient
$R_{eqCside}$	equivalent thermal resistances between the selected point away from the hot spot and ambient
$\hat{R}_{eqCchip}$	calculated equivalent thermal resistances between the selected point right underneath chip and ambient

$\hat{R}_{eqCside}$	calculated equivalent thermal resistances between the selected point away from the hot spot and ambient
R_{th}	thermal resistance
$R_{th}(z)$	distributed thermal resistance at vertical distance z
$R_{th,iF}$	thermal resistance of the i_{Foster}th RC pair
R_{thca}	thermal resistance from case to ambient
R_{thja}	thermal resistance from junction to ambient
R_{thjc}	thermal resistance from junction to case
$R_{thja,side}$	thermal resistance from side chip junction to ambient
s	Laplace variable
t	continuous time
τ_{iF}	corresponding time constant
T_C	case temperature
$T(z)$	temperature at z
ΔT_{ε}	the temperature change from the temperature where the strain is zero
T_a	ambient temperature
$\mathbf{T}_C$	steady-state 2D case temperatures
T_{cchip}	case temperature at the location right beneath IGBT chip
T_{cool}	coolant temperature
T_{cside}	case temperature near the edge of the A_{hot}
T_j	junction temperature

$\hat{T}_j$	estimated junction temperature
ΔT_j	junction temperature swing
ΔT_{jc}	junction-to-case temperature difference
$T_{jmax,side}$	maximum junction temperature of the side chip
T_{jn}	junction temperature of the *n*th chip
T_m	average junction temperature
T_s	sampling period
$u(t)$	input of a target system
V_{CEon}	ON-state collector-emitter voltage
$y(t)$	output of a target system
z	vertical distance from the top surface of the layer to the point of interest
$Z_{nm}(t)$	equivalent transient thermal impedance from the *n*th junction to case when only the *m*th source is powered
$Z_{th,bp}$	transient thermal impedance of the baseplate
$Z_{thjaQQ}(t)$	the self-heating thermal impedance from the IGBT junction to ambient
$Z_{thjaQD}(t)$	cross-heating thermal impedance from the IGBT junction to ambient
Z_{thjc}	transient thermal impedance from junction to case
$Z_{thjcQQ}(t)$	transient thermal impedances from the junction of the IGBT chip to case when the IGBT chip is powered alone

$Z_{thjcQD}(t)$	transient thermal impedances from the junction of the IGBT chip to case when the parallel FWD is powered alone

Chapter 1. Introduction

1.1 Background

The reliability of power electronic converters (or more simply called power converters) in many applications, such as high-power traction and renewable energy generation, has attracted considerable attention in recent years. Power converters tend to experience a higher failure rate than other subsystems in these applications. For example, it was reported that the power electronic converter is the top-ranked subsystem contributing to the overall failure rates and downtime of wind turbines [1], [2]. As most power converters are not designed with redundancy, any faults occurring at the component or subsystem level would cause the shutdown of the whole power converter system. The unexpected interruptions cause safety concerns and result in high operation and maintenance costs, especially for critical applications, such as automobile, backup power source, aircraft power system, etc.

Power semiconductor devices, such as insulated-gate bipolar transistors (IGBTs) and metal-oxide semiconductor field-effect transistors (MOSFETs), were rated as the most fragile components of a power converter in a recent industrial survey [3]. The reliability research in power electronics is now switching from an empirical approach based on previously observed data to a physics-of-failure approach which is more focused on the root causes behind the failures [4], [5]. The physics-of-failure approach can model potential failure mechanisms and integrate investigative results into the design process to improve the robustness of a device. During operation, the physics-of-failure-

based online monitoring systems of power converters can collect useful information, such as junction temperatures for the remaining useful lifetime (RUL) prediction, or directly detect the aging conditions of the devices. The operation of power converters can be more properly managed, and predictive maintenance can be automatically scheduled before components wear out.

1.2 Causes of IGBT Module Failures

Failures of IGBT modules can be roughly classified into two categories: random failures and wear-out failures [9]. Random failures are usually caused by external accidental events, such as particle radiation, voltage transients, and damage by service actions leading to momentary overstress [6]. These failures are not related to the length of service or the age of the device. The wear-out failures are attributed to the accumulation of incremental physical damage under the operating load (stress) conditions, altering the device properties beyond the functional limit [6].

Mitsubishi Electric Corporation, a major IGBT manufacturer, has summarized the causes of IGBT module failures based on an analysis of the failed devices that are returned to their factory. According to the manufacturer's report [6], although problems may be inherent to the device itself or the manner in which it was used, the operational lifetime of the device, however, is dependent on the internal wire bonding and thermal fatigue between the insulation baseplate and the module baseplate.

This dissertation focuses on the major wear-out failures of the bond wire and solder interface caused by thermal fatigue.

1.3 Power Module Package

As the wear-out failures are related to the IGBT package, the power module will be introduced in this section. Power modules are the prevalent types of packages in power electronic applications, dominating in the range of more than 10 A for blocking voltages of 1200 V and above [17]. Power modules may also be integrated with several single functions, e.g., dual-switch, half-bridge leg, often with paralleling of chips for each switch. Fig. 1.1 shows a Mitsubishi IGBT module with two switches in a half-bridge configuration. This module has three main terminals (electrodes) which connect to a voltage source and a load. Each switch is controlled by an external signal that is applied to a pair of gate/emitter auxiliary pins. The structure of this module is illustrated in Fig. 1.2. Silicon chips are placed on a ceramic substrate. The terminals are connected to silicon chips via aluminum wires and the upper copper foil. Silicone gel provides encapsulation and can absorb some damaging vibration.

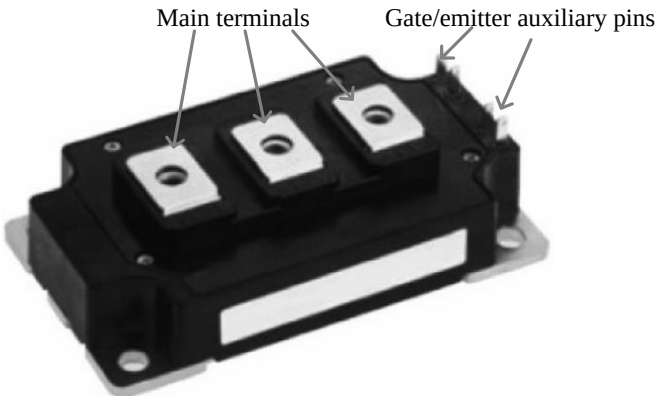


Fig. 1.1: A Mitsubishi IGBT module [7].

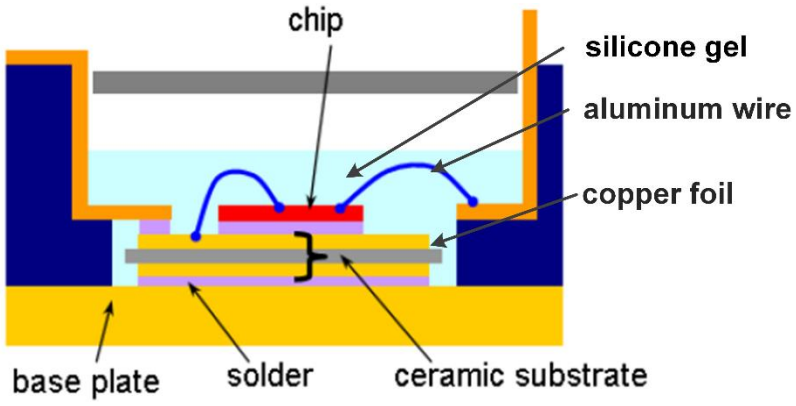


Fig. 1.2: Cross-sectional view of the structure of a Mitsubishi IGBT module [7].

1.4 Physics of Failure of IGBT Modules

In this section, the architecture of IGBT modules will be discussed in detail to explain the physics of failure. Typically, an IGBT module has a complex multilayered architecture, as illustrated in Fig. 1.3. The transistor chip is soldered to the upper copper surface of a ceramic "direct bonded copper" (DBC) substrate. The top side contacts of the silicon chips are connected via wire bonds. Trenches of the upper copper pattern layer of the DBC substrate form current tracks. The substrate is attached to a baseplate by solder. The baseplate is usually mounted onto a heat sink or cold plate with thermal interfacial materials applied on the contact surface. It should be noted that Fig. 1.3 is only for illustration purposes and does not reflect the real geometry of the IGBT module.

The failure of IGBTs can be the result of external accidental events, e.g., an abnormal control signal or bus voltage rise, or the wearing out or aging of the packaging. The lifetime of the device is considered to be limited by aging of the device [6], which is mainly caused by the cyclic thermomechanical stresses generated during temperature excursions due to the mismatch in coefficients of thermal expansion (CTE) between the

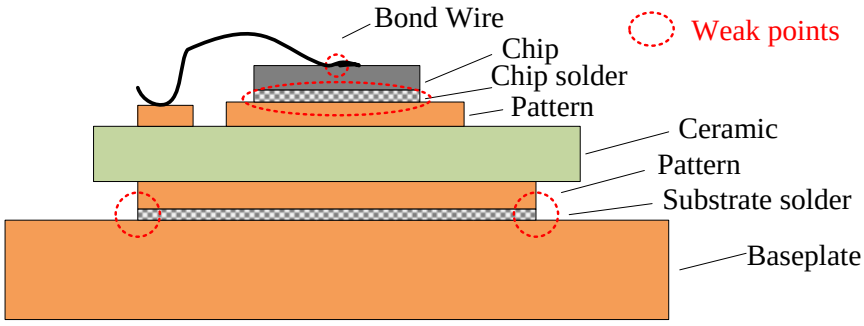


Fig. 1.3: Architecture of an IGBT module with the weak points circled by dashed lines.

materials used in the packaging. The major aging mechanisms frequently observed in IGBT modules are bond-wire liftoff, reconstruction of metallization, and solder aging [10], . Because the CTEs of copper and aluminum are much larger than those of silicon and ceramic, the solder interfaces and the interface between bond wire and chip are more severely stressed when the module undergoes temperature fluctuations. The weak points are shown in Fig. 1.3.

The reliability of power converters can be improved by choosing IGBT modules with more rugged packaging designs, including wire connection optimization [13] and sintered silver for die attachment [14]. However, the trade-off between robustness and cost is always a concern; and the expected lifetime of IGBTs can hardly be guaranteed, especially when the power converters operate under complex work conditions.

1.5 Junction Temperature Estimation and Lifetime Prediction

Information on junction temperature T_j is crucial for operational management of IGBT modules in real-world applications. Accurate junction temperature estimation can be used to prevent overtemperature [15] and predict the RUL [17] for an IGBT module. In practice, junction temperature cannot be directly measured. Typically, it is estimated

by using an electrothermal model, which consists of power loss estimation, a power module thermal model, a cooling system thermal model, and a reference temperature, such as ambient temperature T_a or coolant temperature T_{cool}.

The total power loss P_{loss} of the device includes conduction loss P_{Closs} and switching loss P_{SWloss}:

$$P_{loss} = P_{Closs} + P_{SWloss} \tag{1.1}$$

P_{Closs} and P_{SWlos} can be calculated using the equations in [20] and the device datasheet parameters, which may have temperature dependence.

Two important concepts for thermal modeling of IGBT modules are the thermal resistance from junction to case R_{thjc} and transient thermal impedance from junction to case Z_{thjc}. R_{thjc} is a steady-state value given by:

$$R_{thjc} = \frac{T_j - T_c}{P_{loss}} \tag{1.2}$$

where T_c is the case temperature of the module measured at a specified point on the outside surface of the package. The transient thermal impedance from junction to case Z_{thjc} is calculated based on the measured time-varying T_j (t) and T_c (t) in the device heating phase when a constant IGBT power loss applies.

$$Z_{thjc} = \frac{T_j(t) - T_c(t)}{P_{loss}} \tag{1.3}$$

According to (1.2), if the average junction temperature is of concern, it can be calculated by using R_{thjc}, the calculated average power loss, and the average case temperature. However, to calculate transient T_j (t), a dynamic thermal model should be used. The most commonly used real-time thermal models are thermal equivalent circuits (TECs), such as the Foster- or Cauer-type TEC. The TECs, however, cannot provide an accurate junction temperature estimation in fast-varying loading conditions due to their unsatisfactory

transient responses. More details of the TEC models and other thermal models will be presented in Chapter 2.

The advent of failure of IGBT modules can be predicted by calculating the RUL, which typically uses a lifetime model and information such as IGBT junction temperature. The lifetime of a power IGBT module in the number of cycles to failure can be calculated by using the Leistungselektronik, Systemtechnik und Informationstechnologie (LESIT) model:

$$N_f = A_f \cdot \Delta T_j^{\alpha_f} \cdot \exp(\frac{E_a}{k_B \cdot T_m}) \tag{1.4}$$

where ΔT_j is the temperature swing of junction, T_m is the average junction temperature, k_B is the Boltzmann constant, E_a is the activation energy, and the constants A_f and α_f are determined by experiments. For example, the constants in the model (1.4) for a specific device can be obtained by fitting the device's power cycling curve. An example of a power cycling curve is give in Fig. 1.4. The horizontal axis is the amplitude of ΔT_j in

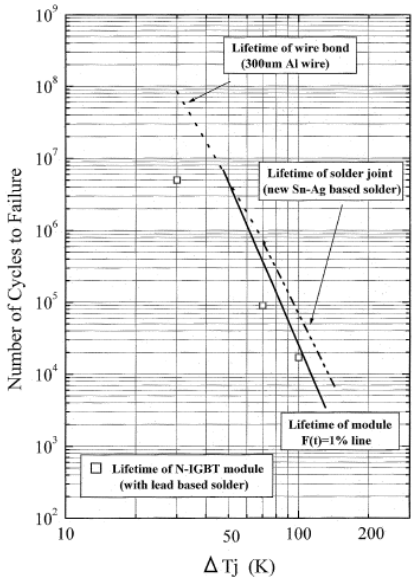


Fig. 1.4: An example of a power cycling curve [16].

each power cycle, and the vertical axis is the number of cycles that the devices fail at an accumulated failure rate, which is typically 20%.

If the typical operation cycles of applications are known, it is possible to calculate the expectation for the lifetime of an IGBT module under these conditions. In real-world applications, many ΔT_j with different amplitudes usually exist in an operation cycle of a power converter. Cycle counting is used to summarize lengthy, irregular T_j-versus-time histories by providing the number of cycles of various ΔT_j amplitudes occurred. Then, the lifetime of the device is typically calculated by using the Palmgren-Miner's rule, which assumes damage accumulation is independent of stress level. If there are N_{cf} different ΔT_j amplitudes, the normalized total damage in one operation cycle is:

$$C_f = \sum_{i_{cf}=1}^{N_{cf}} \frac{n_{f,i_{Cf}}}{N_{f,i_{Cf}}} \tag{1.5}$$

where i_{Cf} is the index of different ΔT_j amplitudes, $N_{f,iCf}$ is the number of cycles to failure for the i_{Cf}th ΔT_j amplitude, and $n_{f,iCf}$ is the number of the cycles occurred with the i_{Cf}th ΔT_j amplitude. The device is considered a failure after $1/C_f$ operation cycles.

However, an RUL prediction for IGBT modules is still not accurate in practice. One cause is that the accuracy of the conventional TEC model is often unsatisfied and degrades during the aging process (such as solder cracking), which results in an inaccurate estimation of T_j, especially for power converters working under complex conditions.

1.6 Real-time Health Monitoring and Prognostic Techniques

Real-time monitoring and prognosis of IGBT modules is considered to be a promising approach to avoid the failure of IGBTs and improve the long-term reliability

of power converters. The aging of bond wires and metallization in an IGBT module results in an increase of the ON-state collector-emitter voltage V_{CEon}; while fatigue of solder interfaces increases R_{thjc}. The commonly used criteria indicating the dangerous health status of IGBT modules are: (1) V_{CEon} has increased by 10~20%, or (2) R_{thjc} has increased by more than 20%. Various techniques for measuring V_{CEon} and T_j (for R_{thjc} calculation) were proposed and tested in a lab environment. However, the changes in V_{CEon} and R_{thjc} are difficult to measure in practice. The existing aging precursors [18] and aging detection techniques [19] for IGBT modules are still premature and/or impractical for real-world applications. These precursors and techniques will be discussed in detail in Chapter 2.

1.7 Problem Statement

As stated in the previous sections, the long-term reliability of power converters can be more cost-effectively improved by real-time overtemperature protection, online RUL prediction, and real-time health monitoring of IGBT modules. However, the existing thermal models for IGBTs are not accurate enough to estimate transient junction temperature for overtemperature protection and RUL prediction. And, there is a gap between the existing aging precursors and real-time monitoring techniques and practical implementation in real-world applications.

The objectives of this research were to: 1) develop cost-effective thermal models to accurately estimate important internal temperatures, e.g., junction temperature, of IGBT modules in real time for better device overtemperature protection and RUL prediction; and 2) invent a practical technique to monitor the major aging processes of IGBT modules in real time for effective maintenance scheduling.

1.8 Dissertation Outline

This dissertation is organized as follows.

Chapter 2 provides a literature review of electrothermal models and condition monitoring techniques for IGBT modules.

Chapter 3 presents a method for designing a physics-based improved Cauer-type TEC thermal model. This model greatly improves the accuracy of the conventional Cauer-type TEC model for the real-time transient junction temperature estimation of IGBT modules with a slightly increased order only.

Chapter 4 describes the characterization of the thermal behavior of an IGBT module using low-order infinite impulse response (IIR) digital filters. The order of the IIR filter thermal model is low because it takes advantage of using the junction temperature as a feedback. Another advantage is that the IIR filter thermal model can be easily implemented in a digital processing system.

Chapter 5 presents a new concept for an effective heat propagation path (EHPP) to interpret the effect of the substrate solder crack on the heat propagation inside an IGBT module. Based on EHPP, a thermal model adaptive to the solder health status can be built; and its parameters can be updated online. This allows accurate real-time junction temperature monitoring over a device's lifespan and a more accurate online prediction of a device's RUL.

Chapter 6 presents a two-dimensional case temperature-based, real-time aging monitoring method for multiple aging processes of IGBT modules in power converters. This approach is based on the physics of failure of IGBT modules and interprets complex aging processes via the changes in the device thermal behaviors. Compared to existing

methods, the proposed method does not interrupt the operation of power converters and can be easily implemented without complex circuitry.

Chapter 7 presents a frequency-domain thermal analysis method to efficiently estimate the temperature swings at the weak points of IGBT modules. By examining the frequency spectra of the power losses of an IGBT module at a loading condition and the frequency responses of the temperatures at weak points, the information on bottleneck weak points under the specific operating conditions can be obtained.

Chapter 8 summarizes the contributions of this doctoral dissertation research. Recommendations for future research are also presented.

Chapter 2. Literature Review

This chapter provides a comprehensive review of existing thermal models as well as the state-of-the-art aging monitoring techniques for IGBT modules.

2.1 Thermal Models for IGBT Modules

The junction temperature of an IGBT module is usually estimated online by using a thermal model, which characterizes the dynamical thermal behavior of the IGBT module. These thermal models mainly include the conventional thermal equivalent circuit (TEC) models, analytical models, numerical models obtained by methods such as Finite Element Analysis (FEA), and digital filter models.

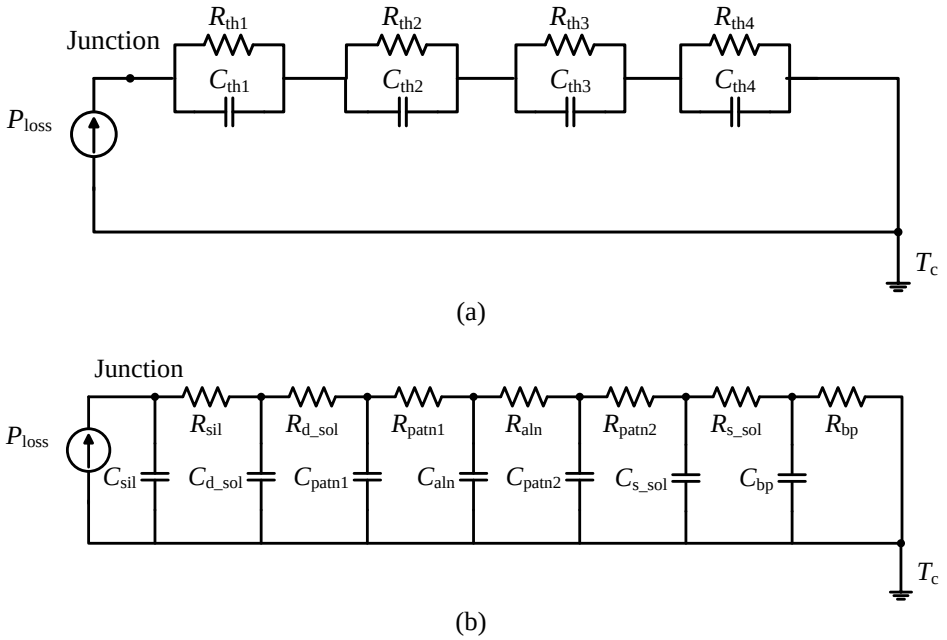


Fig. 2.1: TEC thermal models: (a) Foster-type and (b) Cauer-type.

2.1.1 TEC Models

TECs are the most commonly used models for thermal modeling of IGBT modules, for example [21]-[24]. The TECs have two basic topologies: the Foster-type TECs and the Cauer-type TECs, as shown in Fig. 2.1.

The Foster-type TEC is represented by a certain number of thermal resistor-capacitor (RC) pairs. The values of the thermal RC pairs are typically determined by fitting the sum of the first-order transfer functions of all the thermal RC pairs of the Foster-type TEC to the $Z_{thjc}(t)$ of an IGBT module as follows.

$$Z_{thjc}(t) = \sum_{i_F=1}^{N_{rc}} R_{th,i_F}(1 - e^{-\frac{t}{\tau_{i_F}}}) \tag{2.1}$$

where t is time, N_{rc} is the order of the RC circuit (i.e., the number of thermal RC pairs), i_F is the index of thermal RC pairs, and R_{th,i_F}, C_{th,i_F}, and τ_{i_F} ($=R_{th,i_F} \cdot C_{th,i_F}$) are the thermal resistance, thermal capacitance, and time constant of the i_Fth thermal RC pair, respectively. The Foster-type TEC has limitations in estimating fast transient temperature changes of the IGBT module [25]. When $t/\tau_{i_F} \rightarrow 0$,

$$Z_{thjc}(t) = \sum_{i_F=1}^{N_{rc}} R_{th,i_F}(1 - e^{-\frac{t}{\tau_{i_F}}}) \approx (\sum_{i=1}^{N} \frac{R_{th,i_F}}{\tau_{i_F}}) \cdot t \tag{2.2}$$

Equation (2.2) indicates that the Foster-type TEC can only accurately model the special case in which $Z_{thjc}(t)$ has a slope of one in the log-log coordinates because the power of t is about one. Otherwise, a relatively large error will occur, which makes accurate junction temperature estimation impossible under fast-changing power loss conditions.

There is an analogy between the heat diffusion equation and the differential equation for a transmission line with distributed line resistance and shunt capacitance [26]. The analogy between thermal and electric variables is shown in Table 2.1. A Cauer-type TEC of an IGBT module is constructed based on the analogy and the geometry of the module, where the nodes, thermal resistances, and thermal capacitances have physical meanings.

The parameters of the Cauer-type TEC can be adjusted by considering the temperature dependence of the materials' properties [27], [28], leading to an adaptive thermal model. To accurately characterize the thermal behavior of an IGBT module, a high-order Cauer-type TEC with distributed thermal resistance and capacitance is typically required. On the other hand, a low-order, high-accuracy, Cauer-type TEC model is always desired for online or real-time applications.

For a power semiconductor device with relatively simple packaging, e.g., the "transistor outline" (TO) package, a low-order Cauer-type TEC can be obtained based on the time constant spectra calculated from the thermal step response of the device [29], [30]. However, that method assumes that the thermal behavior of the packaging can be represented by the sum of a few first-order systems; and their time constants are widely

Table 2.1: Analogy between thermal and electrical variables.

	Variables	
	Thermal	**Electrical**
Through variable	heat flow rate, q	current, I
Across variable	temperature, T	voltage, V
Resistance	thermal resistance, R_{th}	resistance, R
Storage	thermal capacity, C_{th}	capacitance, C

separated [31]. Therefore, that method may not work for the IGBT modules with a relatively complex architecture.

The authors in [32] introduced the Elmore delay formula to model the propagation delay times of the heat flux in the layers of an IGBT module. Then, the time constants and thermal capacitances of the layers can be calculated using the calculated delay times and the measured thermal resistances of the layers. However, the application of the Elmore delay formula to the parameter calculation of the Cauer-type TEC is questionable because the Elmore delay formula is typically used for calculating the RC interconnect delays between voltage drivers and ideal (infinite impedance) loads.

The conventional Cauer-type TEC model neglects the temperature difference in each layer of the IGBT module and models each layer by a thermal resistance and a lumped thermal capacitance [30], [33]. The lumped thermal capacitance modeling is oversimplified for bulky layers, e.g., the ceramic layer and baseplate layer, which reduces the transient performance of the conventional Cauer-type TEC. Therefore, the accuracy of the dynamic junction temperature of the IGBT module estimated by using the conventional Cauer-type TECs is unsatisfactory.

2.1.2 Analytical Models

Analytical models, such as [34], [35], are usually obtained based on series approximation techniques to solve heat transfer equations, which are mathematically complex even if the boundary conditions are simplified. Moreover, these models are often subject to problems such as series truncation and convergence [36].

For example, an exact solution to heat conduction in a simple planar plate with power law and polynomial heat flux input was presented in [37]. Green’s functions were

used and resulted in slowly converging summation, which had to be replaced with closed-form polynomial expressions. The final solution was very complex. In [38], for heat conduction in a two-layer composite slab, a semi-analytical procedure was developed to obtain a relatively "simple" solution. The problem was simplified by analyzing the different transition times of the two layers of the slab. However, that method had to deal with the irregularly spaced eigenvalues of an eigenproblem with coefficients having the step change at an interior point. The temperature profile of the homogeneous layer of a two-layer material was found very sensitive to eigenvalue errors when the eigenvalues were derived from the other layer.

An alternative Fourier-technique-based junction temperature estimation method was reported in [39], where the time-domain power loss of the IGBT module was represented by a set of Fourier series, and the thermal impedance of the IGBT module was characterized in the frequency domain from the frequency response of a classical transient TEC. Then, the junction temperature of the IGBT was estimated in the frequency domain. However, that method still relied on the accuracy of the classical TEC.

2.1.3 Numerical Models

Three-dimensional (3D) thermal models generated by commercial software, such as ANSYS, or numerical methods, such as convolution integrals over 3D geometry [40], can handle complex geometry and simulate realistic conditions of an IGBT module. They can provide accurate transient junction temperature estimation, if used with care. However, they are computationally intensive and are, therefore, impractical for online implementation.

2.1.4 Digital Filter Models

As systems can be considered as filters, the thermal behavior of an IGBT module can be characterized by digital filters. In [41], a digital filter was obtained by discretizing a Foster-type TEC for efficient junction temperature estimation. However, that digital filter model still relied on the accuracy of the Foster-type TEC; and the continuous-discrete conversion in that model might not preserve the properties of the continuous-time model at high frequencies (above 1/10 of the sampling frequency).

In [42], digital filters for modeling thermal cross-couplings in power devices were obtained by fitting the corresponding frequency-domain thermal characteristics, which were measured by applying pseudo-random binary sequence (PRBS) input-power waveforms to the power devices. However, the control of the generation of the PRBS power loss in IGBTs can be very difficult, especially when the thermal characteristics over a wide range of frequencies are of interest.

The thermal models for IGBT modules in the literature are compared in terms of accuracy, complexity, and computational cost, as shown in Table 2.2. It reveals that none of these models can have high accuracy while keeping the complexity and computational cost low. The TEC and digital filter models are the best options for real-time use.

Table 2.2: Comparison of existing thermal models for IGBT modules

Models	**Accuracy**	**Complexity**	**Computational Cost**
TEC	Low	Low	Low
Analytic model	Medium	High	Medium
Numerical model	High	Medium	High
Digital filter model	Low/medium	Low	Low

However, their accuracy needs to be improved.

2.2 Condition Monitoring Techniques for IGBT Modules

The weak points in an IGBT module, in terms of aging, include the bond wires, emitter metallization, chip solder, and substrate solder [18], [43]. In the literature, the major aging processes of IGBT modules have been commonly monitored using the electrical and thermal parameters of the IGBT modules [44].

2.2.1 Bond Wire Aging Monitoring Using V_{CEon}

The wire bonding failures in IGBT modules are generally caused by bond wire liftoff, heel cracking, or metallization reconstruction. V_{CEon} has often been used for condition monitoring of bond wires and emitter metallization. As V_{CEon} is sensitive to T_j, T_j should also be acquired. Detailed methods for T_j measurements will be presented in the next subsection. This subsection focuses on the V_{CEon} measurement circuitry.

The authors in [45] developed in situ V_{CEon} measurement circuitry for IGBTs on electric vehicles, as shown in Fig. 2.2. An auxiliary power supply unit (PSU) was used to inject 100 mA current for junction temperature measurements, and a high-current (50A) pulse train for diagnosis of a selected IGBT during a vehicle stop. The selection was achieved by using a selector relay network to connect the IGBT switch terminals to the PSU. The V_{CEon} measurement, however, cannot be performed when the inverter is operating. Extreme transient voltages and common-mode voltages that affect measurement accuracy and may cause damage to the sensitive measuring equipment have to be handled carefully.

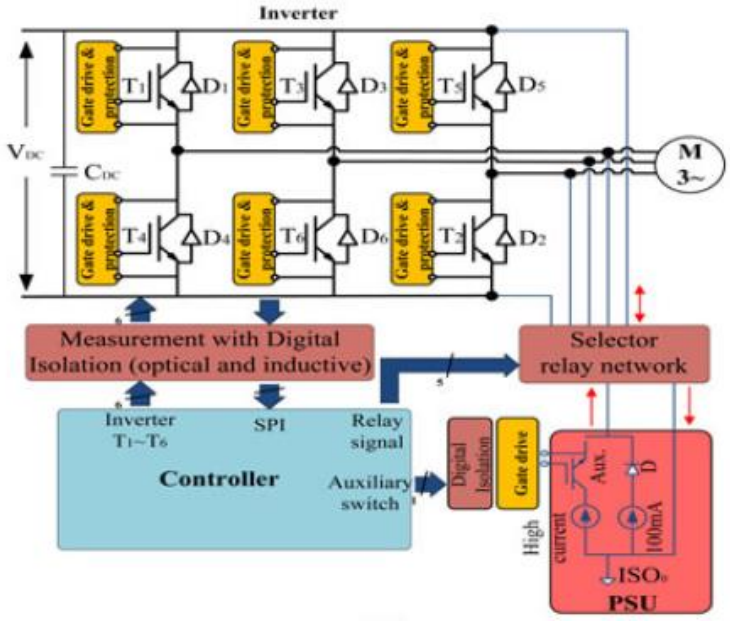


Fig. 2.2: Schematic diagram of the in situ measurement circuitry for IGBTs on electric vehicles in [45].

In [46], an "on-line" V_{CEon} measurement scheme was invented, as shown in Fig. 2.3. Different auxiliary MOSFETs had to support the high DC voltage but conduct very low currents (100 mA or less) with respect to the power IGBT. V_{CEon} at 100 mA was acquired during the bridge "dead time" to indirectly measure IGBT junction temperature. Then, within a very short time (around 1 ms), V_{CEon} was measured at about 100 A. This circuit may acquire V_{CEon} at high current and at a desired junction temperature. However, the timing or synchronization of a sequence of V_{CEon} measurements is difficult to control.

In summary, the method of using V_{CEon} usually requires complex and costly circuitry to detect millivolt-level drifts in V_{CEon} against a noisy collector-emitter voltage V_{CE}, which varies from several volts to hundreds of volts during the operation of the IGBT. The implementation may interrupt the normal operation of power converter or alter the original power converter circuit design.

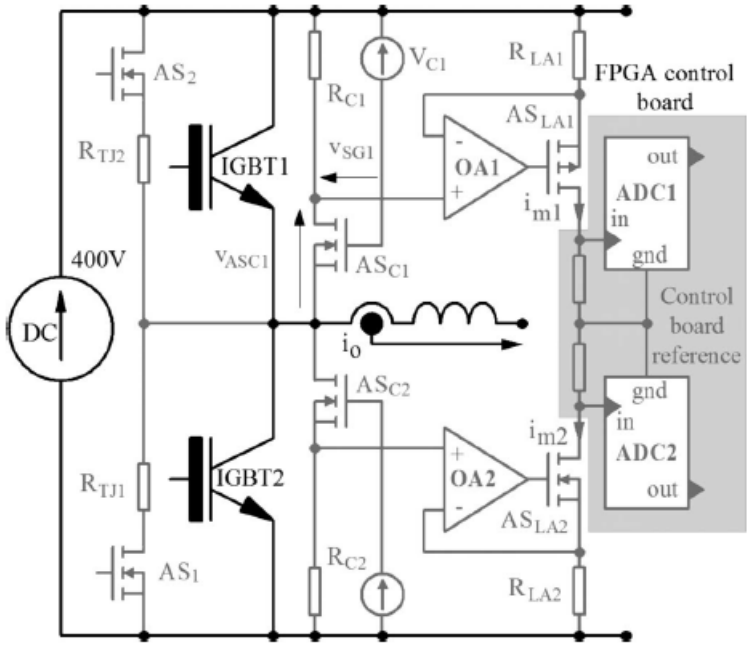


Fig. 2.3: V_{CEon} measurement scheme (parallel diodes are not drawn) in [46].

2.2.2 Solder Aging Monitoring Using Temperature-Sensitive Electrical Parameters and R_{thjc}

R_{thjc} has often been used for condition monitoring of solder layers [47], [48]. The detection of solder aging requires measurements of a temperature-sensitive electrical parameter (TSEP), e.g., the saturation collector-emitter voltage V_{CEon}, to indirectly measure T_j, which is then used to calculate the changes in R_{thjc} using (1.2).

In [49], common TSEPs were compared in terms of sensitivity, linearity, calibration need, genericity, accuracy, measurement of a thermal impedance, and on-line measurement. As shown in Fig. 2.4, voltage under a low current (e.g., V_{CEon} at 100 mA) is the best TSEP overall. However, as discussed in the previous subsection, measuring V_{CEon} requires additional high-accuracy measurement circuitry and cannot be performed during the operation of the power converter.

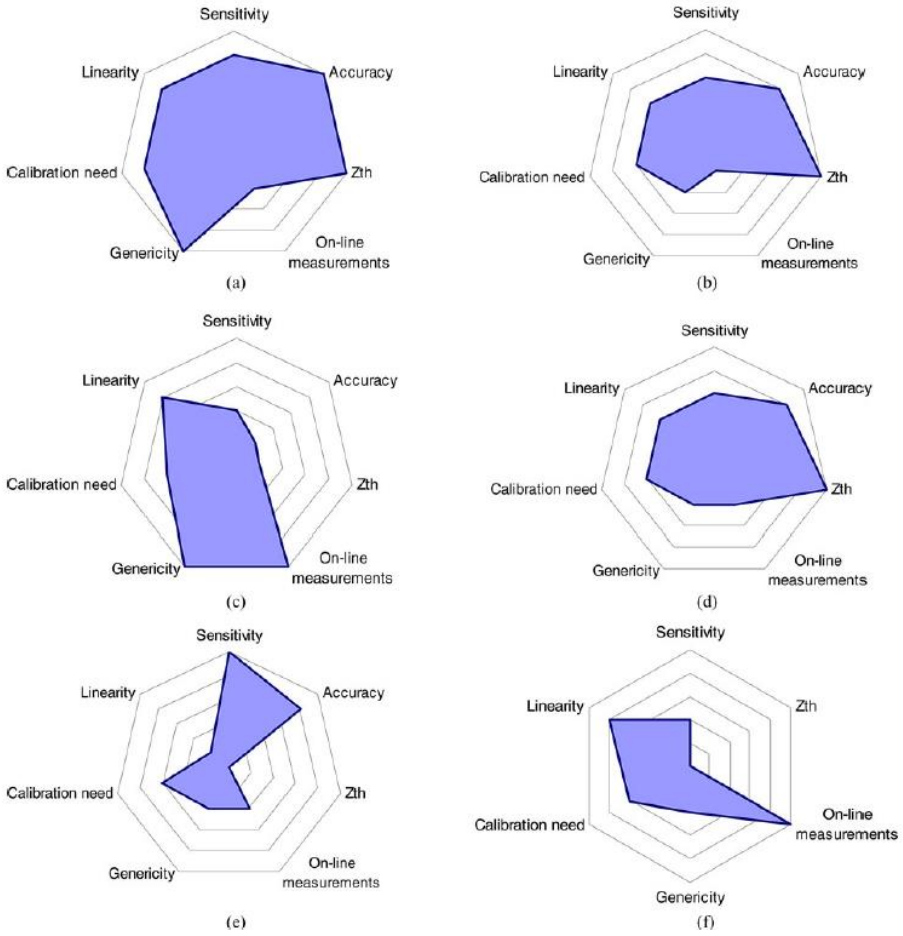


Fig. 2.4: Comparison of the different TSEPs [49]. (a) Voltage under a low current (diode, IGBT, MOSFET in OFF-state). (b) Threshold voltage. (c) Voltage under a high current. (d) Gate-emitter voltage. (e) Saturation current. (f) Switching times.

2.2.3 Other Electric Aging Precursor and Aging Monitoring Techniques

Other aging monitoring methods based on monitoring changes in the switching behaviors of IGBTs, as a consequence of junction temperature elevation, have been reported in [50]-[52]. In [50], the dynamic changes in the gate current during the turn-on and turn-off processes of an IGBT module were used to monitor the aging of the module. In [51], a small change in the inverter harmonic current was used to detect the solder aging of the IGBT modules. In [52], the turn-off time was used as a precursor for IGBT

latch-up. However, in practice, the changes in these switching behavior-related parameters are very difficult to catch, especially when the increase in the junction temperature is not significant.

2.2.4 Aging Monitoring Using Thermal Signal

Compared to electrical parameters, the changes in the temperatures of power converters are much slower and, therefore, can be more easily captured online. As a temperature signal consists of relatively low frequency components, the measurement noises can be easily filtered out. However, except for T_j, which is difficult to measure directly, other temperatures have rarely been used for monitoring the aging of IGBT modules.

In [53], a lookup table between power loss and case temperature was first constructed for a healthy IGBT module. Then, the power loss during the aging process of the IGBT module was calculated using the case-above-ambient temperature measured at one point and a one-dimensional (1D) case-to-ambient TEC model. The difference between the case temperature corresponding to the calculated power loss obtained from the lookup table and the measured case temperature was then used to estimate the increase in R_{thjc} for solder aging monitoring. That approach is based on the assumption that solder aging causes a rise of R_{thjc} and T_j, which causes an increase of the power loss. However, the increase of the power loss can be caused by either solder aging or bond-wire aging and the power loss cannot be calculated accurately by the 1D case-temperature-based method when a substrate solder crack occurs.

The condition monitoring techniques for IGBT modules in the literature are compared in terms of performance, requirement for additional circuit, and feasibility for

online implementation, as shown in Table 2.3. Using V_{CEon} for monitoring bond wire aging and measuring T_j and R_{thjc} are the only methods that can provide satisfactory performance. However, additional complex circuity is required and the operation of the power converter may be interrupted. The method that uses T_c for solder aging monitoring is the only method that is easy to implement. However, that method is limited to monitoring a simple device aging process—solder aging only.

2.3 Summary

In this chapter, previous works on thermal models and condition monitoring techniques of IGBT modules were reviewed. These thermal models were discussed in terms of accuracy, complexity, and computational cost. A simple cost-effective thermal model suitable for online transient junction temperature estimation is still lacking. Condition monitoring for IGBTs is an emerging topic. The existing aging precursors and the corresponding measurement techniques are still impractical for real-world applications. Typical drawbacks are additional complex circuits, alternation of the existing power converter design, and interruption of the normal operation of the power converters.

Table 2.3: Comparison of existing condition monitoring techniques for IGBT modules

Techniques	Performance	Additional complex circuit	Online implementation
Bond wire aging monitoring using V_{CEon}	Good	Yes	Difficult
Solder aging monitoring using TSEPs and R_{thjc}	Poor for most TSEPs	Yes	Difficult for most TSEPs
IGBT switching behaviors	Poor	Yes	Difficult
Solder aging monitoring using one point T_c	Susceptible to interference	No	Easy

Chapter 3. A Physics-Based, Improved Thermal Equivalent Circuit Model

This chapter presents a physics-based, Cauer-type thermal equivalent circuit (TEC) with improved transient performance for IGBT modules [54]. A new concept, lumped capacitance approximation error, is introduced. Based on this concept, a method is proposed to determine the appropriate number of sublayers that should be subdivided from a layer in an IGBT module. For the bulky baseplate layer, an analytical expression of its thermal impedance is derived and simplified to a first-order transfer function, which can be represented by a thermal resistance and capacitance pair in the TEC. The proposed Cauer-type TEC model greatly improves the accuracy of the conventional Cauer-type TEC model for the transient junction temperature estimation of IGBT modules with a slightly increased order only.

3.1 The Lumped Parameters of the Cauer-Type TEC

Based on the lumped capacitance model, the distributed Cauer-type TEC is approximated by a low-order, lumped Cauer-type TEC. The conventional lumped Cauer-type TEC is usually constructed based on the experience of the designer. Typically, the temperature difference across each layer in the heat flow direction in the IGBT module is neglected. Then the volume that the heat flows through in each layer is treated as a lump with uniformly distributed temperature. For a layer, its thermal resistance, R_{th}, and thermal capacitance, C_{th}, are calculated by

$$R_{th} = \int_0^{d_l} \frac{1}{k \cdot A(z)} dz \tag{3.1}$$

$$C_{th} = \int_0^{d_l} c_v \cdot A(z) dz \tag{3.2}$$

where d_l is the layer's thickness, k the thermal conductivity of the layer's material, c_v is the volumetric heat capacity of the layer's material, z is the variable representing the vertical distance from the top surface of the layer to the point of interest, and $A(z)$ is the horizontal cross-section area at the distance z. A heat spreading angle (with a typical value of 45°) can be incorporated into (3.1) and (3.2) by adjusting $A(z)$. For a "standard" IGBT module, shown in Fig. 3.1, thermal behavior can be modeled by a 7th order lumped Cauer-type TEC, as illustrated in Fig. 3.2. The conventional lumped Cauer-type TEC is computationally efficient. However, it may not be able to accurately capture the junction temperatures of IGBT modules in real-world applications, e.g., the estimation of the junction temperature variation of a power converter in a line cycle.

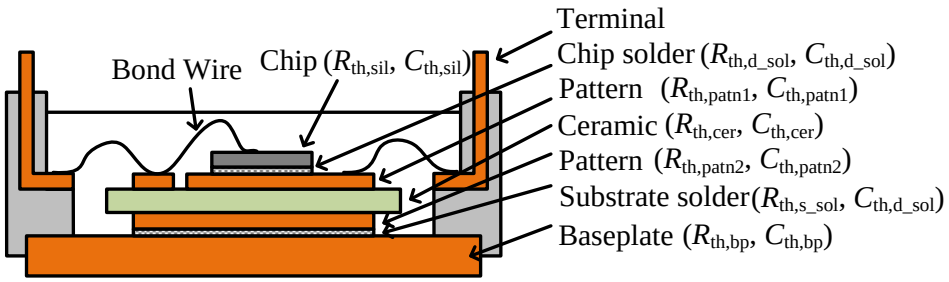


Fig. 3.1: The architecture of an IGBT module with Cauer-TEC RC parameters.

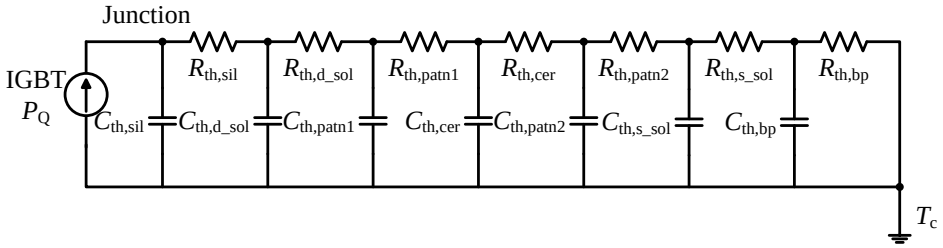


Fig. 3.2: The conventional lumped Cauer-type TEC for an IGBT module.

3.2 Construction of the Improved Cauer-Type TEC

The lumped Cauer-type TEC is built upon the lumped capacitance model. Thus, the estimated temperature distribution is discrete. As illustrated in Fig. 3.3, the steady-state temperature distribution in the layers of an IGBT module in the vertical direction z estimated by the conventional lumped Cauer-type TEC, i.e., the dash-line curve, is compared to the actual temperature distribution (i.e., the solid-line curve), where the top surface of the chip layer is the reference position with $z = 0$ and the horizontal temperature axis starts from T_c to the T_j. The actual temperature distribution through layers is continuous, as illustrated in Fig. 3.3, and can be estimated using a distributed Cauer-type TEC or an FEA model, which is more accurate than the lumped Cauer-type TEC. The slope of the temperature distribution in each thin layer is almost constant because the difference between the heat condition areas on the top and bottom surfaces of the layer, caused by the heat spreading effect, is negligible. The errors in the temperature distribution approximation using the conventional lumped Cauer-type TEC, i.e., the triangle shadow areas enclosed by the two curves, result in extra heat stored in the layers of the TEC, leading to an overestimation of the thermal capacitance of each layer. This results in an underestimation of the junction temperature changes in the transient states.

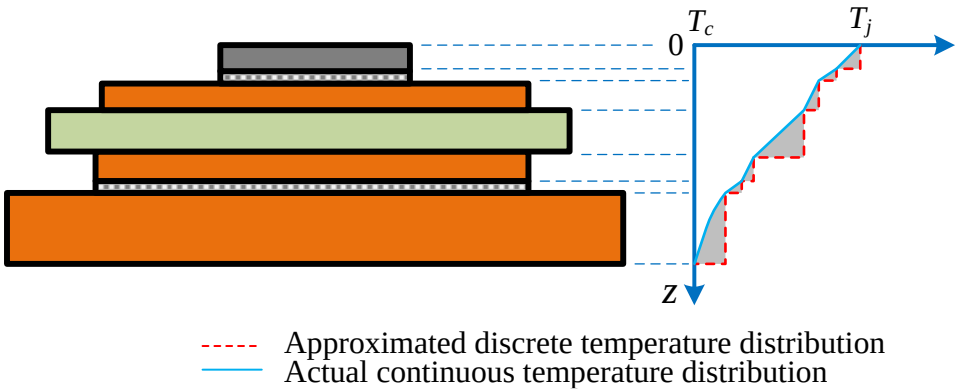


Fig. 3.3: Illustration of the temperature distributions in the layers of an IGBT module estimated by the conventional lumped Cauer-type TEC and the actual continuous temperature distribution of the IGBT module in the steady-state condition.

3.2.1 Subdivision of the Layers in IGBT Modules

The performance of the lumped Cauer-type TEC can be improved by subdividing a bulky layer into smaller sublayers with the same thickness and modeling each sublayer by a smaller lump, which can reduce the temperature approximation error and the extra heat storage capacity. To determine whether a layer needs subdivision, a lumped–capacitance approximation error CE_{lc} is defined for the layer and compared with the total thermal capacitance $C_{th,tot}$ of the IGBT module. Here CE_{lc} represents the overestimation error of the lumped thermal capacitance of the layer caused by the temperature distribution approximation error in the steady-state condition of the IGBT module, while $C_{th,tot}$ is the amount of heat needed to raise $(T_j - T_c)$ by 1 ºC. Consider the ith layer. The corresponding $CE_{lc,i}$ and $C_{th,tot}$ are calculated by

$$CE_{lc,i} = \frac{1}{2N_{sub}} \frac{R_{th,i}}{R_{thjc}} C_{th,i} \tag{3.3}$$

$$C_{th,tot} = \frac{1}{R_{thjc}} \left[\sum_{i=1}^{M} C_{th,i} \cdot \left(\sum_{j=1}^{i} R_{th,j} - \frac{1}{2} R_{th,i} \right) \right] \tag{3.4}$$

where N_{sub} is the number of sublayers of the ith layer, M is the number of layers of the IGBT module, $R_{th,i}$ is the thermal resistance of the ith layer, and $C_{th,i}$ is the lumped thermal capacitance of the ith layer. The derivation of (3.3) and (3.4) is provided in the Appendix. The thermal resistance and capacitance of each sublayer is about $1/N_{sub}$ of the thermal resistance and capacitance of the ith layer, respectively. According to (3.3), the value of $CE_{lc,i}$ is reduced by subdividing the layer and is inversely proportional to the number of sublayers N_{sub}. By specifying a desired value for $CE_{lc,i}$, N_{sub} can be determined from (3.3) for each layer. For example, a criterion for building an accurate Cauer-type TEC is that CE_{lc} of each layer is less than 5‰ of $C_{th,tot}$.

The typical layer thicknesses in a "standard" IGBT module [17] and the corresponding R_{th}, C_{th}, and CE_{lc} per chip are shown in Table 3.1, assuming a 10 mm × 10 mm × 0.2 mm chip size and a 45° heat spreading angle. According to the proposed criterion, it is straightforward to subdivide the aluminum nitride (AlN) layer into four sublayers. Moreover, since the transient temperature in milliseconds is largely determined by the thermal behavior of the silicon chip, it is suggested that the chip layer be subdivided into two to three sublayers to improve the fast transient performance of the

Table 3.1: Typical layer thicknesses and thermal parameters (without subdivision) in a high-power IGBT module.

	d_l (mm)	R_{th} (°C/W)	C_{th} (J/°C)	CE_{lc} (J/°C)	$CE_{lc}/C_{th,tot}$ (‰)
Chip	0.2	0.0161	0.0326	0.0021	2.1
Solder	0.05	0.0078	0.0086	2.6×10-4	0.26
Copper	0.3	0.0072	0.1113	0.0032	2.4
AlN	0.635	0.0275	0.1968	0.021	16.5
Copper	0.3	0.0052	0.1549	0.0032	2.4
Solder	0.2	0.0194	0.0554	0.0043	3.3
Baseplate	5	0.0438	5.4519	0.94	725.4

Cauer-type TEC model.

3.2.2 Approximation of the Thermal Impedance of the Bulky Baseplate

However, the subdivision of the bulky baseplate layer using the proposed criterion will dramatically increase the order of the TEC. To solve this problem, a physics-based analysis is presented to derive a low-order approximation of the thermal behavior of the baseplate. First, an exact description of the thermal behavior of the baseplate is derived by infinitely slicing the baseplate vertically, as shown in Fig. 3.4. This model could be described by the following equations [55]

$$\begin{cases} -\frac{dq(z_{bp})}{dz_{bp}} = sC_{th}(z_{bp})T(z_{bp}) \\ -\frac{dT(z_{bp})}{dz_{bp}} = R_{th}(z_{bp})q(z_{bp}) \end{cases} \tag{3.5}$$

where z_{bp} is the variable representing the vertical distance from the top surface towards the bottom surface of the baseplate; $q(z_{bp})$, $C_{th}(z_{bp})$, $R_{th}(z_{bp})$, and $T(z_{bp})$ denote the heat flow, distributed heat capacitance, thermal resistance, and temperature at z_{bp}, respectively. The $R_{th}(z_{bp})$ and $C_{th}(z_{bp})$ can be calculated by

$$R_{th}(z_{bp}) = \frac{dz_{bp}}{k_{bp}[a+2z_{bp}\cdot\tan(\theta)][b+2z_{bp}\cdot\tan(\theta)]} \tag{3.6}$$

$$C_{th}(z_{bp}) = c_{vbp}[a + 2z_{bp}\cdot\tan(\theta)][b + 2z_{bp}\cdot\tan(\theta)]\cdot dz_{bp} \tag{3.7}$$

where a and b are the side lengths of the heat flux area at the top surface of the baseplate, k_{bp} is the thermal conductivity of copper, c_{vbp} is the volumetric specific heat of copper, and θ is the heat spreading angle. The $q(z_{bp})$ in (3.5) can be eliminated by

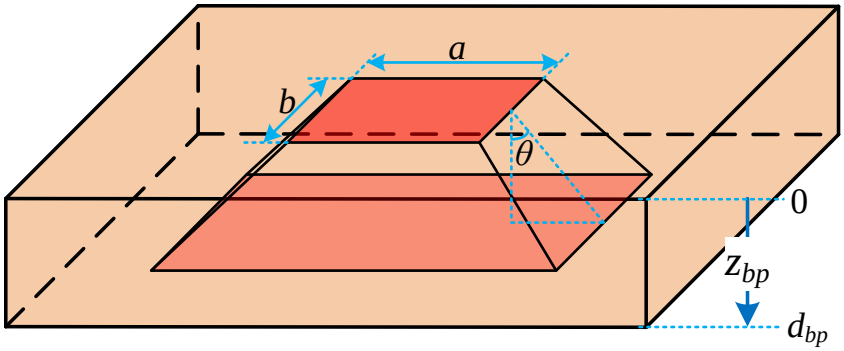
$$\begin{aligned} -\frac{d^2T(z_{bp})}{dz_{bp}{}^2} &= \frac{dR_{th}(z_{bp})}{dz_{bp}}q(z_{bp}) + R_{th}(z_{bp})\frac{dq(z_{bp})}{dz_{bp}} \\ &= \frac{dR_{th}(z_{bp})}{dz_{bp}}\left[-\frac{1}{R_{th}(z_{bp})}\frac{dT(z_{bp})}{dz_{bp}}\right] + R_{th}(z_{bp})[-sC(z_{bp})T(z_{bp})] \end{aligned} \tag{3.8}$$

Then, by substituting (3.6) and (3.7) into (3.8) and some manipulations, the governing equation for $T(z_{bp})$ is obtained by

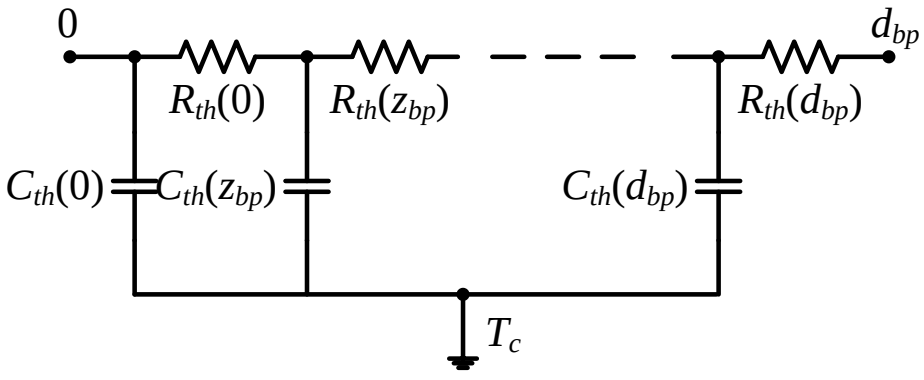
$$\frac{d^2T(z_{bp})}{dz_{bp}{}^2}+\frac{8\tan^2(\theta)\cdot z_{bp}+2\tan(\theta)\cdot(a+b)}{[a+2z_{bp}\cdot\tan(\theta)][b+2z_{bp}\cdot\tan(\theta)]}\frac{dT(z_{bp})}{dz_{bp}}-\frac{sc_{vbp}}{k_{vbp}}T(z_{bp})=0 \qquad (3.9)$$

An explicit solution of (3.9) only exists for $a = b$. Since a and b in (3.9) are usually close, they can be replaced by $c=\sqrt{ab}$. Then, the general solution of (3.9) is given by

$$T(z_{bp})=\frac{1}{1+2\tan(\theta)\cdot z_{bp}/c}\cdot\left[C_1\cosh\left(\sqrt{sc_{vbp}/k_{bp}}\cdot z_{bp}\right)+C_2\sinh\left(\sqrt{sc_{vbp}/k_{bp}}\cdot z_{bp}\right)\right] \qquad (3.10)$$



(a)



(b)

Fig. 3.4: The exact description of the thermal behavior of the baseplate. (a) The sketch of the geometry and heat spreading and (b) the distributed Cauer-type TEC model for the baseplate.

where C_1 and C_2 are constants determined by the boundary conditions of the baseplate. As the time constant of the cooling system is much larger than that of the IGBT module, the temperature of the bottom surface of the baseplate can be assumed to be a constant. Then, the boundary conditions can be simplified to

$$\begin{matrix} T(d_{bp})=0 \\ q(0)=-k_{bp}c^2\cdot\left.\frac{dT(z_{bp})}{dz_{bp}}\right|_{z_{bp}=0}=P_{flux} \end{matrix} \tag{3.11}$$

where d_{bp} is the thickness of the baseplate and P_{flux} is heat flux applied at the top surface of the baseplate. Then, the transient thermal impedance $Z_{th,bp}$ of the baseplate is

$$Z_{th,bp}=\frac{T(0)-T(d_{bp})}{P_{flux}}=\frac{1/(k_{bp}c^2)}{2\tan(\theta)/c+\sqrt{sc_{vbp}/k_{bp}}\cdot\coth(\sqrt{sc_{vbp}/k_{bp}}\cdot d_{bp})} \tag{3.12}$$

where s is the Laplace variable. Equation (3.12) can be further simplified by substituting the Taylor series of the term $\coth(\sqrt{sc_{vbp}/k_{bp}}\cdot d_{bp})$. For the baseplate layer, only the relatively low frequency components (typically 0 ~ 20 Hz) need to be considered. Then, the value of $\sqrt{sc_{vbp}/k_{bp}}\cdot d_{dp}$ is small enough to allow the term $\coth(\sqrt{sc_{vbp}/k_{bp}}\cdot d_{dp})$ approximated by the first two terms of its Taylor series. Then, (3.12) is reduced to

$$\begin{aligned} Z_{th,bp} &= \frac{1/(k_{bp}c^2)}{1/d_{bp}+2\tan(\theta)/c+\frac{1}{3}sc_{vbp}d_{bp}/k} \\ &= \frac{d/(k_{bp}c^2)}{1+2\tan(\theta)d_{bp}/c}\cdot\frac{1}{1+\frac{1}{3}d_{bp}/[k_{bp}\cdot c^2\cdot(1+2\tan(\theta)d_{bp}/c)]\cdot sc_{vbp}d_{bp}c^2} \\ &\approx R_{th,bp}\cdot\frac{1}{1+sR_{th,bp}C_{th,bp}/3} \end{aligned} \tag{3.13}$$

where $R_{th,bp}$ and $C_{th,bp}$ are the thermal resistance and the lumped thermal capacitance of the baseplate, respectively. Equation (3.13) suggests that the equivalent thermal capacitance for the baseplate approximates one third of $C_{th,bp}$. Therefore, the transient thermal behavior of the bulky baseplate can be modeled more accurately by still using a first-order transfer function, i.e., a single thermal resistance and capacitance pair.

3.3 Simulation Validation

A commercial IGBT module, CM400DY-12NF, made by Powerex was studied to compare the transient performance of the conventional Cauer-type TEC and the proposed Cauer-type TEC. The IGBT module has two switches. Each switch consists of two IGBT chips and two diode chips.

A high-fidelity FEA thermal model of the test IGBT module cooled by a cold plate (see Fig. 3.5) was built as a reference model in Autodesk Simulation Multiphysics 2012, which is a commercial FEA software platform. The geometry information of the module was provided by Powerex. The IGBT module was mounted on a liquid-cooled cold plate, which is represented by an aluminum block with coolant pipes. The temperature of the pipes was set to the inlet coolant temperature. The thickness of the thermal grease layer between the baseplate of the module and the cold plate was 0.1 mm. In the FEA thermal model, a fine mesh was used for the IGBT module, while a relatively

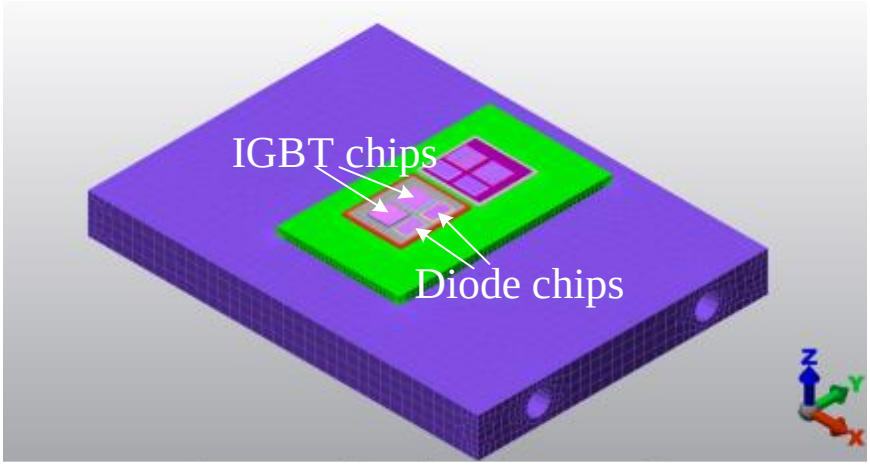


Fig. 3.5: The model of a CM400-12NF IGBT module with a cold plate built in Autodesk Simulation Multiphysics.

coarse mesh with 20,044 nodes was used for the cold plate. The total mesh of the FEA thermal model of the IGBT module with the cold plate has 79,787 nodes. The power losses were assumed to be generated inside the chips close to their top surfaces [35]. The order of the conventional Cauer-type TEC is 7; while the order of the proposed Cauer-type TEC is 12, where the chip and AlN layers were subdivided into three and four sublayers, respectively.

First, the transient thermal impedances from junction to case of the IGBT module, $Z_{thjc}(t)$, were obtained from the conventional Cauer-type TEC model, the proposed Cauer-type TEC model, and the FEA thermal model by applying a step-change power loss to the three models while setting the temperature of the bottom surface of the IGBT module to be a constant. The results are compared in Fig. 3.6. It shows that the proposed Cauer-type TEC model was more accurate than the conventional Cauer-type TEC model with

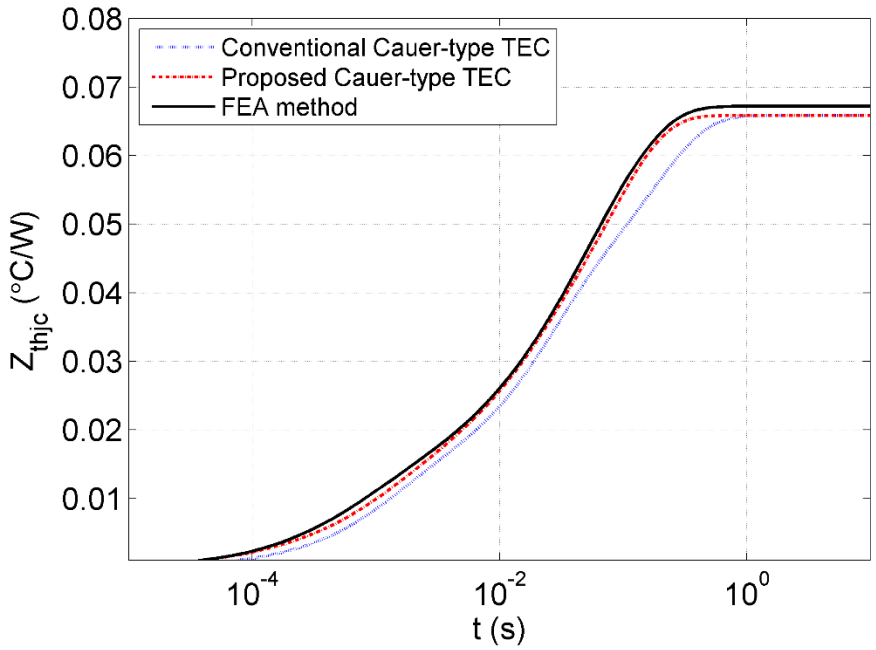
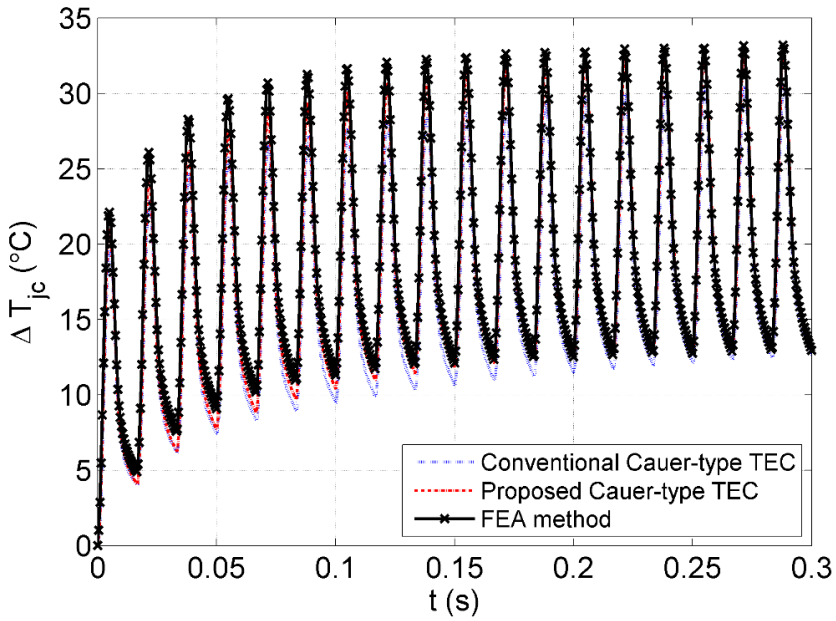


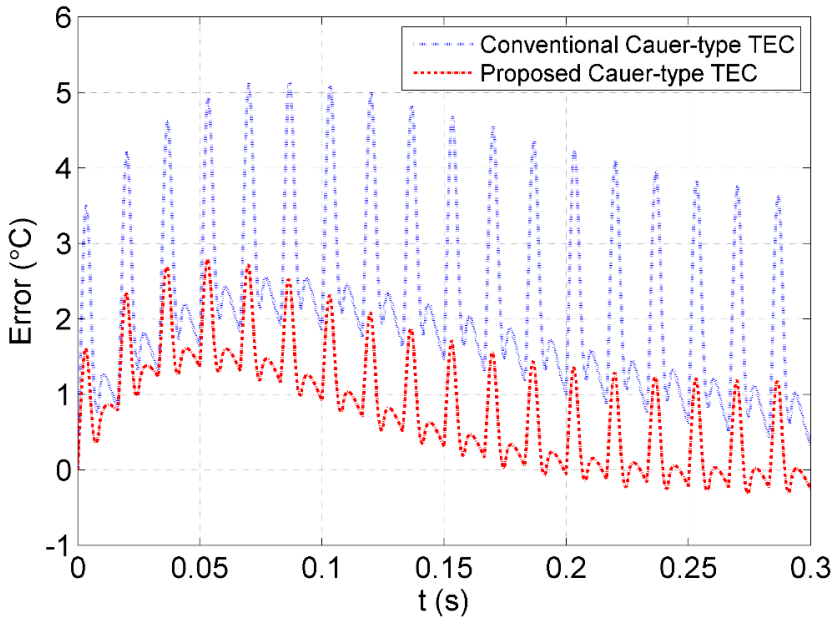
Fig. 3.6: Comparison of the transient thermal impedances from junction to case obtained from the conventional Cauer-type TEC model, the proposed Cauer-type TEC model, and the FEA model.

respect to the FEA thermal model. In particular, the value of $Z_{thjc}(t)$, from approximately 0.1 s to 0.9 s, was mainly determined by $Z_{th,bp}$, i.e., the thermal behavior of the baseplate. Due to the use of a more accurate model (3.13) to characterize the thermal behavior of the baseplate, the value of $Z_{thjc}(t)$ obtained from the proposed Cauer-type TEC model was a clear improvement over that obtained from the conventional Cauer-type TEC model, from approximately 0.1 s to 0.9 s.

The accuracy of the proposed Cauer-type TEC for the junction temperature estimation was evaluated by placing the IGBT module as a leg in a three-phase, two-level inverter. The operating condition of the inverter was the following: 400 V DC-link voltage, 400 A output current, a power factor of 0.8, a unity modulation index, 5 kHz switching frequency, and 60 Hz line frequency. Fig. 3.7(s) compares the values of the junction-to-case temperature difference, $\Delta T_{jc}(t)$, estimated by using the conventional Cauer-type TEC model, the proposed Cauer-type TEC model, and the FEA thermal model. Fig. 3.7(b) shows the temperature estimation errors of the conventional Cauer-type TEC model and the proposed Cauer-type TEC model with respect to the FEA thermal model. The maximum error of the proposed Cauer-type TEC model was 2.8 °C, which increased to 5.1 °C when using the conventional Cauer-type TEC model. The average error of the proposed Cauer-type TEC model was only about 30% of that of the conventional Cauer-type TEC model over the operating period of the inverter.



(a)



(b)

Fig. 3.7: Comparison of junction temperature estimation by the three models when the inverter was operated at a constant operating condition: (a) $\Delta T_{thjc}(t)$; and (b) errors with respect to the FEA thermal model.

3.4 Summary

This chapter proposed a method for constructing an improved low-order Cauer-type TEC model for IGBT modules. First, the lumped capacitance approximation error was introduced to determine the appropriate number of lumps needed to model a layer in an IGBT module. For the bulky baseplate layer that requires many lumps to model, an analytical expression of its thermal impedance was derived and simplified to a first-order transfer function, which was then represented by a thermal resistance and capacitance pair in the TEC. The proposed Cauer-type TEC model was validated by simulation studies for a commercial IGBT module. Compared to the conventional Cauer-type TEC, the proposed Cauer-type TEC has a slightly higher order but greatly improved the accuracy of the transient junction temperature estimation for IGBT modules.

Chapter 4. Real-Time Junction Temperature Estimation Using Low-Order Digital Filters

This chapter presents a digital filter model to characterize the thermal behaviors of IGBT modules as well as heat sinks [57]. The thermal impedances from junction to ambient/coolant are characterized by low-order infinite impulse response (IIR) digital filters. Compared to the conventional Foster-type TEC model, the low-order IIR filter model can greatly improve the accuracy of the transient junction temperature estimation for IGBT modules. The IIR filters can be implemented easily and efficiently in digital processing systems for real-time junction temperature estimation of IGBT modules.

4.1 An IGBT Module with Liquid Cooling

An IGBT module typically contains multiple IGBT chips and diode chips, which are placed on one or several multilayer substrate stack(s) on a baseplate. The IGBT module with liquid cooling is illustrated in Fig. 4.1. During the operation of the IGBT

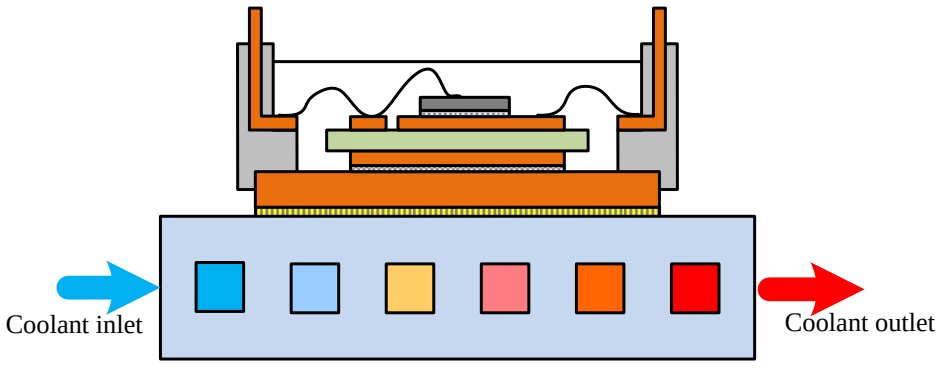


Fig. 4.1: An IGBT module (only one chip is shown) cooled by a cold plate.

module, heat is generated at the chips and spreads through the layers to the bottom of the baseplate, which is cooled by a cold plate. The thermal behavior of the IGBT module can be characterized by a linear system when the cooling condition is stable and the temperature effects of the materials' thermal properties are negligible.

4.2 IIR Digital Filter

This section provides a brief introduction of the IIR filter. The use of digital filters instead of analog filters has many advantages, e.g., it is easy to design and implement digital filters, digital filters can handle larger dynamic ranges, and the performance of digital filters is stable [41]. Digital filters can be classified into two categories: finite impulse response (FIR) filters and IIR filters. The primary advantage of IIR filters over FIR filters is that they typically meet a given set of specifications with a much lower filter order [58]. The function of an IIR filter, $H(z)$, in the z domain is

$$H(z) = \frac{B_{IIR}(z)}{A_{IIR}(z)} = \frac{b_0 + b_1 z^{-1} + \cdots + b_{nb} z^{-nb}}{a_0 + a_1 z^{-1} + \cdots + a_{na} z^{-na}} \tag{4.1}$$

where a_i (i = 0, 1, ⋯, na and $a_0 \neq 0$) and b_j (j = 0, 1, ⋯, nb) are coefficients. The coefficients of $H(z)$ for a target system can be easily determined by using the input $u(t)$ and the output $y(t)$ of the target system obtained in a certain system response and a filter parameter identification algorithm, such as the Steiglitz-McBride method. In this dissertation, the input and output during the impulse response of the target system are obtained from the step response of the system to identify the coefficients.

The Steiglitz-McBride method is a fast iterative algorithm that solves for all a_i and b_j simultaneously to minimize the total square error between the filter output and the

given output signal. For example, the coefficients can be determined iteratively by solving the following least-square problem.

$$min \sum_{t=1}^{N} \left\{ \hat{A}_{IIR,k+1}(z) \left[\frac{1}{\hat{A}_{IIR,k}(z)} y(t) \right] - \hat{B}_{IIR,k+1}(z) \left[\frac{1}{\hat{A}_{IIR,k}(z)} u(t) \right] \right\}^2 \qquad (4.2)$$

where k is the iteration index and N is the number of data. $\hat{A}_{IIR,k}(z)$ and $\hat{B}_{IIR,k}(z)$ are the estimates of the denominator and numerator in (4.1) obtained at iteration k; $\hat{A}_{IIR,k+1}(z)$ and $\hat{B}_{IIR,k+1}(z)$ are the refined estimates of denominator and numerator in (4.1) obtained by solving (4.2). The coefficients can also be identified when noises are present in input and output samples. More details of this algorithm can be found in [59], [60].

4.3 IGBT Thermal Modeling Using IIR Filters

In an IGBT module, the junction temperature of a chip depends on the heat generated by the chip (self-heating) and the heat generated by other chips (cross-heating). The self-heating of chips and the cross-heating between chips can be characterized by self-heating and cross-heating thermal impedances, respectively. The self-heating thermal impedances are typically provided in the datasheets of IGBT modules. The cross-heating thermal impedances can be obtained from FEA simulations and experiments. The thermal impedances can be considered as the step responses of the systems characterizing the self-heating of chips and cross-heating between chips [56]. Then, the impulse responses of the systems needed to design the IIR filters can be obtained from the derivatives of the transient thermal impedance curves. As the IIR filter uses the junction temperature as a feedback, accurate junction temperature estimation can be achieved by an IIR model with several orders. It is recommended that the order selected be the same as that of the Foster-type TEC model (typically 4-8) to ensure a much improved performance.

Given the impulse responses derived from the self-heating thermal impedances, the coefficients of the IIR filters characterizing the self-heating of chips can be easily obtained using the method mentioned in the previous subsection. Let $H_{nn}(z)$ be the IIR filter charactering the self-heating of the *n*th chip. The implementation of the IIR filter in the *z* domain and the discrete time domain are expressed by (4.3) and (4.4), respectively.

$$T_{jn}(z) = H_{nn}(z)P_n(z) + T_a(z) \tag{4.3}$$

$$T_{jn}[k_{dt}] = \frac{1}{a_0}\left\{\sum_{j=0}^{nb} b_j \cdot P_n[k_{dt} - j] - \sum_{i=1}^{na} a_i \cdot T_{jn}[k_{dt} - i]\right\} + T_a[k_{dt}] \tag{4.4}$$

where T_{jn} and P_n are the junction temperature and power loss of the *n*th chip, respectively; k_{dt} is the index of the discrete time sequence; and T_a is the ambient temperature.

The pure delay time due to the heat propagation path between chips needs to be considered to design the IIR filters to characterize the cross-heating between chips. This can be easily addressed by adding a discrete time delay term, z^{-c}, to $H(z)$, where c is an integer, which is the division of the delay time and sampling period. Let $H_{nm}(z)$ be the IIR filter charactering the relationship between the junction temperature, T_{jn}, of the *n*th chip and the power loss, P_m, of the *m*th chip. Then, the implementations of the IIR filter in the *z* domain and the discrete time domain are expressed by (4.5) and (4.6), respectively.

$$T_{jn}(z) = z^{-c}H_{nm}(z)P_m(z) + T_a(z) \tag{4.5}$$

$$T_{jn}[k_{dt}] = \frac{1}{a_0}\left\{\sum_{j=0}^{nb} b_j \cdot P_n[k_{dt} - j - c] - \sum_{i=1}^{na} a_i \cdot T_{jn}[k_{dt} - i]\right\} + T_a[k_{dt}] \tag{4.6}$$

When multiple chips are powered, their junction temperatures can be calculated by the superposition of the temperature rises from the ambient, caused by all of the chips. The *z* domain matrix form of the proposed method to calculate the junction temperatures

of *N* chips of interest for an IGBT module with *M* heat sources is given as follows, where $\mathbf{1}_{1\times N}$ is a *N*-dimensional column vector with all elements being 1.

$$\begin{bmatrix} T_{j1} \\ T_{j2} \\ \vdots \\ T_{jN} \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} & \cdots & H_{1M} \\ H_{21} & H_{22} & & H_{2M} \\ \vdots & & \ddots & \vdots \\ H_{N1} & H_{N1} & \cdots & H_{NM} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_M \end{bmatrix} + T_a \cdot \mathbf{1}_{1\times N} \tag{4.7}$$

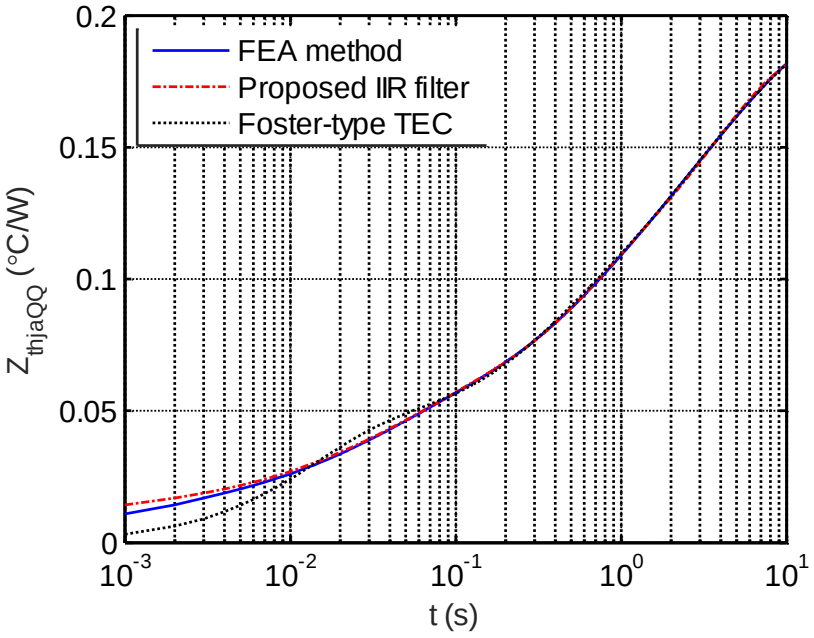
4.4 Simulation Validation

A commercial IGBT module CM400DY-12NF made by Powerex (described in Chapter 3) was studied to compare the transient performance of the Foster-type TEC model and the proposed IIR filter thermal model. The same high-fidelity FEA thermal model of the test IGBT module cooled by a cold plate built in Autodesk Simulation Multiphysics 2012 was used as the reference model. A detailed description of the FEA thermal model can be found in Chapter 3. In the study described here, the inlet coolant temperature was set to 60 ºC.

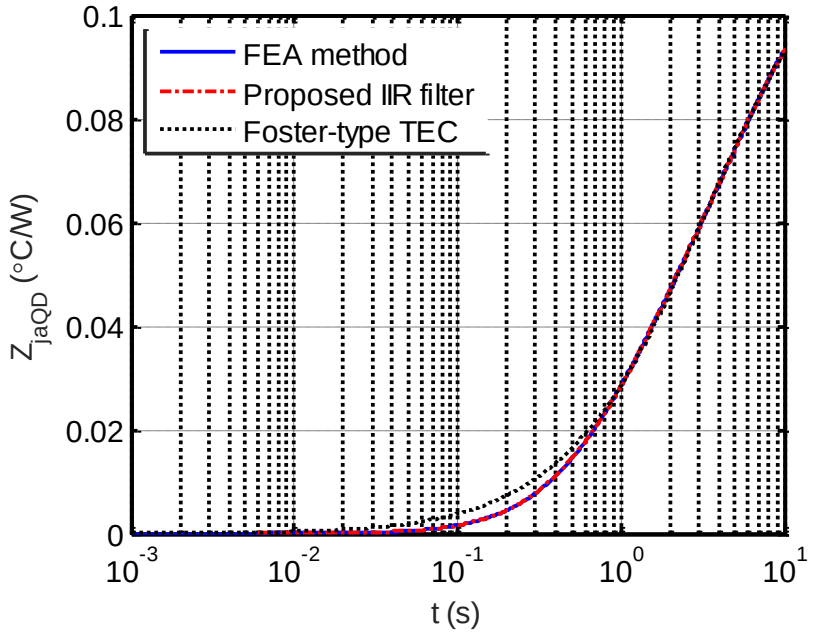
As the cross-heating between chips on different stacks is negligible, only the thermal coupling effect between IGBT chips and diode chips on the same stack was considered. A step-change power loss was applied to the two IGBT chips in parallel on a stack to obtain the self-heating thermal impedance from the IGBT junction to ambient, $Z_{thjaQQ}(t)$. Another simulation, in which a step-change power loss was applied to the two diode chips on the same stack, was performed to obtain the cross-heating thermal impedance from the IGBT junction to ambient, $Z_{thjaQD}(t)$. Two 5th-order digital IIR filters were designed to characterize the two thermal impedances, respectively. The sampling period for the implementation of the IIR filters was 1 ms. The coefficients of the digital IIR filters were obtained by using the built-in Steiglitz-McBride method, stmcb(), in

MATLAB®. Two 6th-order Foster-type TECs were also obtained by fitting the responses of the two thermal impedances using the curve fitting toolbox of MATLAB. The performance of the digital IIR filters and the Foster-type TECs were compared with respect to the FEA thermal model, as shown in Fig. 4.2. The proposed IIR filter thermal model agrees well with the FEA thermal model for characterizing both $Z_{thjaQQ}(t)$ and $Z_{thjaQD}(t)$. However, noticeable errors were observed in $Z_{thjaQQ}(t)$ characterized by the Foster-type TEC model when $t < 0.07$ s. The performance of the Foster-type TEC model for $Z_{thjaQD}(t)$ characterization is even worse−erroneous when $t < 0.4$ s−because the Foster-type TEC model cannot model the pure delay caused by the distance between the IGBT and diode chips.

The accuracy of the proposed IIR filter thermal model for junction temperature estimation was further evaluated in a power converter operating scenario. The IGBT module was operated as a leg in a two-level three-phase inverter. The operating point was: 400 V DC-link voltage, 400 A output current, power factor of 0.8, unity modulation index, 5 kHz switching frequency, and 60 Hz line frequency. The $T_j(t)$ responses estimated by the FEA thermal model, the proposed IIR filter thermal model, and the Foster TEC model are compared in Fig. 4.3. The maximum error between the FEA thermal model and the proposed IIR filter thermal model was less than 1.5 °C. The Foster-type TEC model can track the trend of a $T_j(t)$ increase but fails to estimate the fast $T_j(t)$ variation in each fundamental period of the inverter. This is because Foster-type TECs cannot accurately characterize the thermal impedances, especially $Z_{thjaQQ}(t)$ and $Z_{thjaQD}(t)$ when t is small.

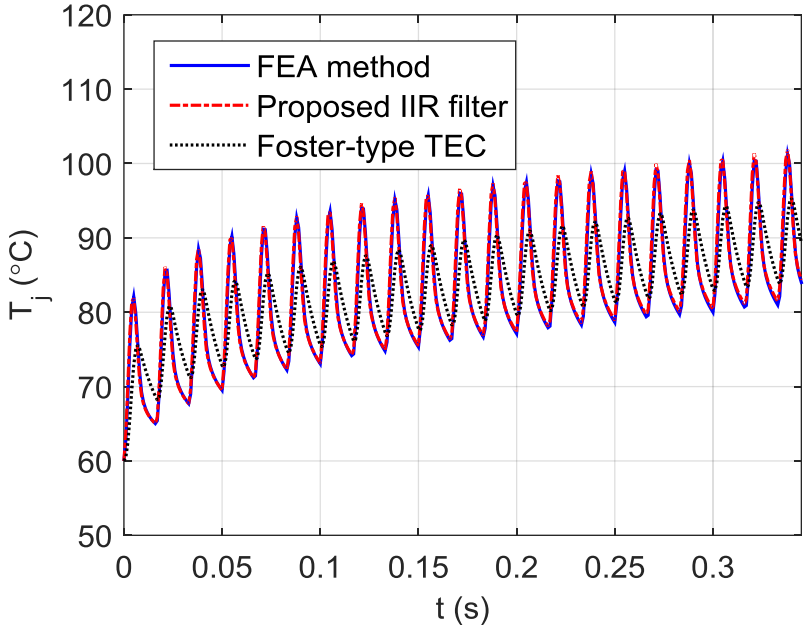


(a)



(b)

Fig. 4.2: Comparison of the thermal impedances modeled by the 6th-order Foster-type TECs, the proposed 5th-order IIR filters, and the FEA method: (a) $Z_{thjaQQ}(t)$ and (b)$Z_{thjaQD}(t)$.



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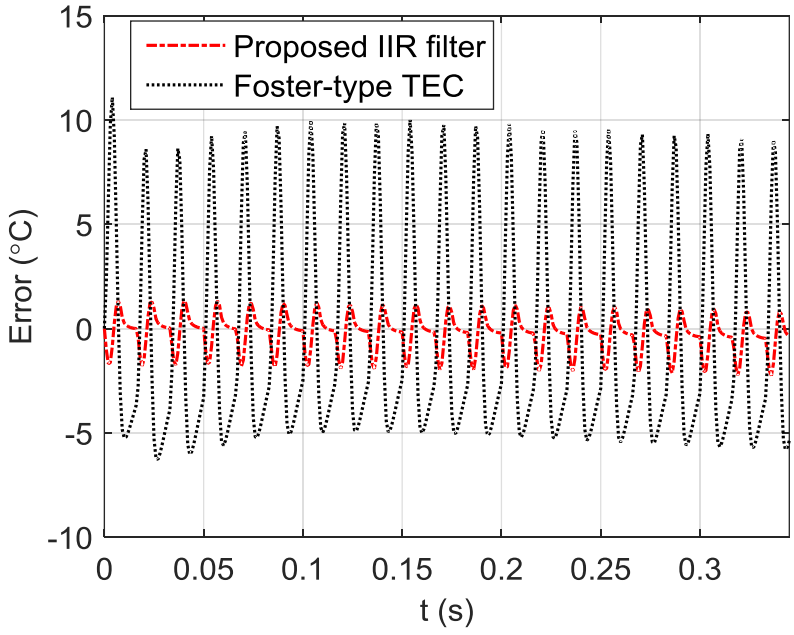


(b)

Fig. 4.3: Comparison $T_j(t)$ of the IGBT estimated by the three methods when the inverter is operated at a constant operating condition: (a) junction temperature and (b) error with respect to the FEA method.

A transient load, which mimicked the starting process of an electric motor in a hybrid electric vehicle (HEV), was applied to the inverter to evaluate the accuracy of the proposed IIR filter thermal model for real-time junction temperature estimation. The rotor speed of the motor was accelerated from 0 rpm at 0 s to 500 rpm at 1 s. The currents through the IGBT module during this period were generated by simulating an HEV powertrain using a battery model provided by the MATLAB/Simulink® example library. The power losses, $P_{loss}(t)$, generated by the chips were calculated based on the simulated currents as well as the conduction voltage-current curve and switching loss-current curve provided by the datasheet for the IGBT module. The total power loss profile of the IGBT chips in one switch of the module is shown in Fig. 4.4, where the power loss is averaged over each switching period.

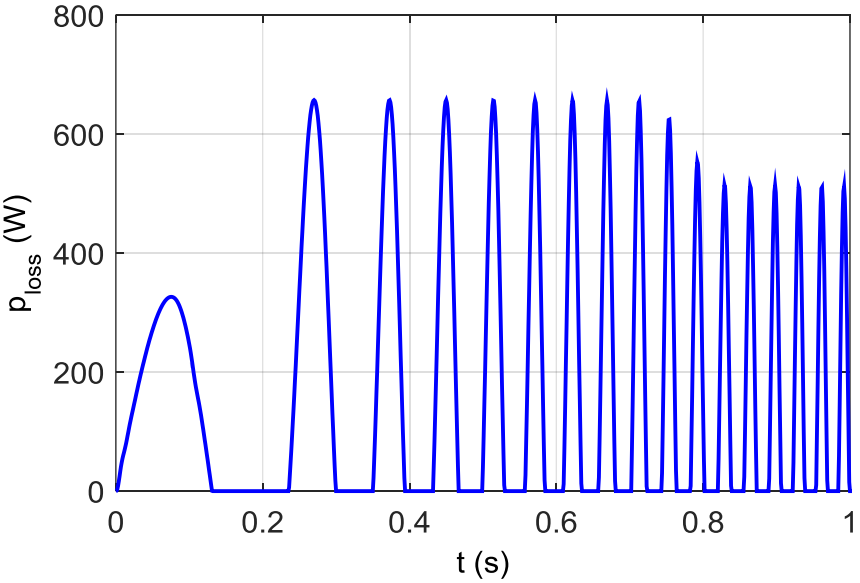
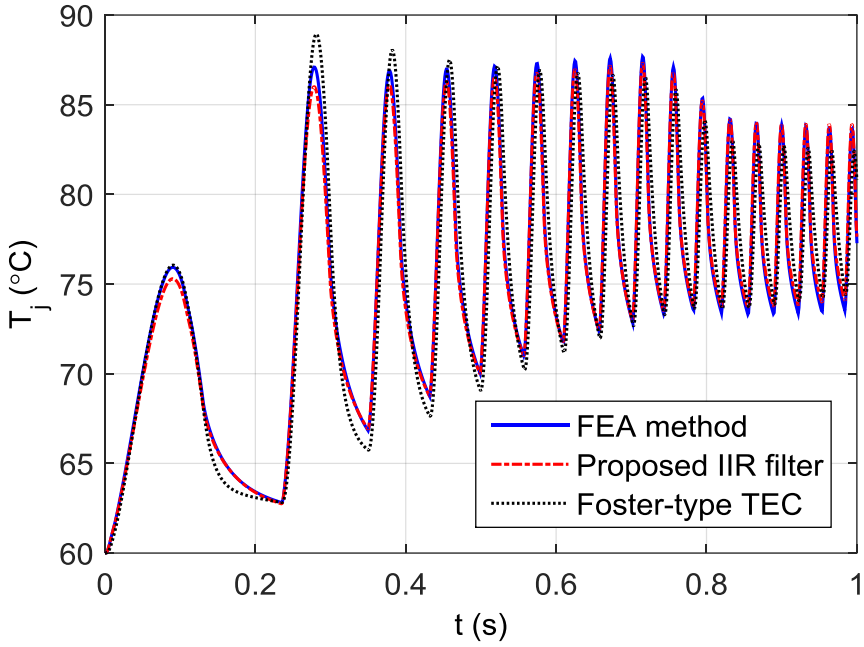
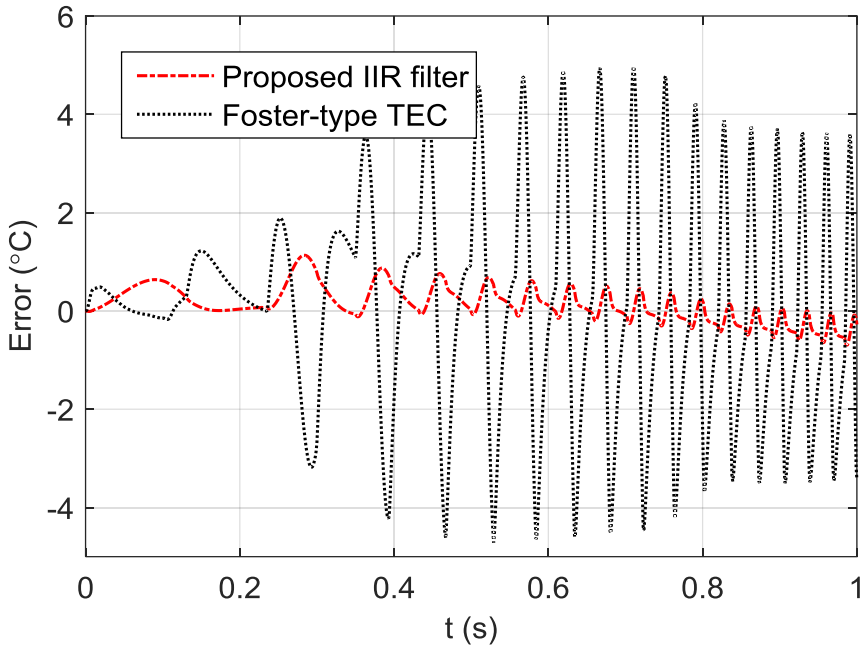


Fig. 4.4: Total power loss profile of the IGBT chips in one switch of the IGBT module in a transient load condition.



(a)



(b)

Fig. 4.5: Comparison $T_j(t)$ estimated by the three methods when the inverter is operated with a transient load: (a) junction temperature; and (b) error at peaks and valleys with respect to the FEA method.

The values of $T_j(t)$ estimated by the FEA thermal model, the proposed IIR filter thermal model, and the Foster-type TEC model are compared in Fig. 4.5. The proposed IIR filter thermal model agrees with the FEA thermal model much better than the Foster-type TEC model. The maximum error of the IIR filter thermal model is only 1 °C when $T_j(t)$ varies between 60 °C and 87 °C, while the maximum error of the Foster-type TEC model is about 5 °C. The proposed IIR thermal model can always provide an accurate $T_j(t)$ estimation when both the amplitude and frequency of the $P_{loss}(t)$ vary. In contrast, the Foster-type TEC model overestimates $T_j(t)$ fluctuations when the frequency is low but underestimates $T_j(t)$ fluctuations after the frequency increases, indicating an unstable performance during the transient load.

4.5 Summary

This chapter presented the use of low-order IIR digital filters for accurate real-time junction temperature estimation of IGBT modules. The self-heating and cross-heating thermal impedances of the IGBT module were characterized by low-order IIR filters. The coefficients of the IIR filters were obtained by using the Steiglitz-McBride method. Simulation results have shown that the transient junction temperature of IGBT modules can be accurately estimated by using the IIR filters with orders even lower than those of the Foster-type TECs. The digital IIR filters can be easily implemented in a digital processing system for real-time junction temperature estimation of IGBT modules.

Chapter 5. An Effective Heat Propagation Path-Based Online Adaptive Thermal Model

Information on the junction temperature is crucial for operational management of IGBT modules. In practice, junction temperature is typically estimated by using an electrothermal model. IGBT modules are subject to various aging processes during operation, some of which, e.g., substrate solder cracking, change the thermal impedance of an IGBT module. However, little work has been reported in the literature on including aging effects in online thermal behavior modeling of IGBT modules.

This chapter presents an effective heat propagation path (EHPP)-based online adaptive thermal model for IGBT modules [61], where the EHPP is proposed to quantify the impact of substrate solder cracks on heat propagation inside IGBT modules. A straightforward relationship between substrate solder crack and the degree of nonuniformity of case temperature distribution is established. Based on the EHPP, the parameters of a TEC, e.g., a Cauer-type TEC, are adjusted online to track thermal behavior changes of the IGBT modules caused by substrate solder cracks, leading to an adaptive thermal model. The proposed adaptive thermal model is validated by comparing its results with FEA simulation results for a commercial IGBT module.

5.1 EHPP-Based Thermal Behavior Characterization for IGBT Modules

Due to the complexity of the geometry and differences in the materials' properties, the heat propagation inside an IGBT module is a complex, dynamical process. In this section, a new concept of EHPP is introduced to effectively quantify the impact of substrate solder cracks on the thermal behavior of IGBT modules. Then, the dissertation will show that the change in the thermal resistance from the junction to the case of an IGBT module caused by substrate solder cracks can be interpreted by the change in the EHPP, which can be quantified by the degree of nonuniformity of the case temperature distribution.

The EHPP is defined as the thermal path in an IGBT module through which most heat flows, as illustrated in Fig. 5.1. During operation of an IGBT, heat is assumed to be generated at the top surface of a die and to spread down through different layers to the bottom of the baseplate, which is cooled by a heat sink or a cold plate. Compared to the top surface of a die, the EHPP covers a larger area at the bottom surface of the baseplate,

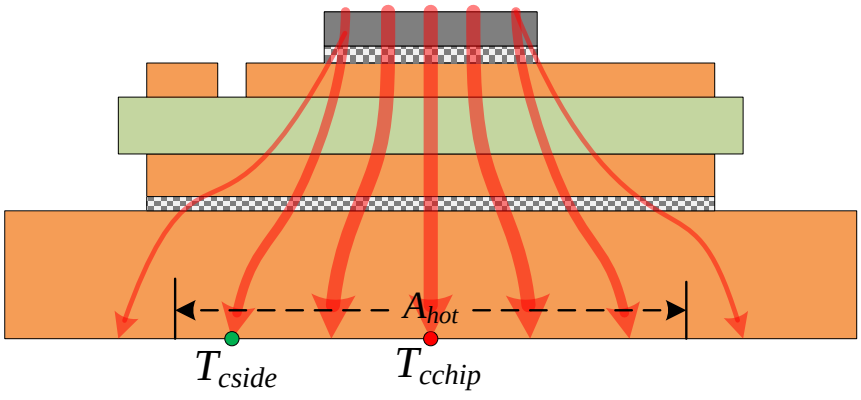


Fig. 5.1: The EHPP in a healthy IGBT module.

called the baseplate hot area, A_{hot}. The temperature inside A_{hot} is much higher than that in the remaining area of the bottom surface of the baseplate. The baseplate hot area, A_{hot}, can be viewed as the thermally effective contact to the heat sink or the effective heat removal area. The following paragraphs describe how the EHPP and A_{hot} change with substrate solder aging and how the relationship between the change in case temperature distribution and the remaining noncracking solder area in the substrate solder layer is derived.

A crack usually initializes from the edge of the substrate solder layer and then propagates to the center [71]-[73]. The crack does not significantly affect the heat propagation inside the module or the thermal resistance of the module until it encroaches on the EHPP. When that occurs, the status of the IGBT module is dangerous as the heat flows are forced to concentrate in the remaining noncracking portion of the substrate solder layer. Both the EHPP and A_{hot} shrink, resulting in an increase in the IGBT module's thermal resistance and the degradation of heat removal at the bottom surface of the baseplate, as illustrated in Fig. 5.2.

Assuming that the same amount of heat is generated at the top surface of the chip,

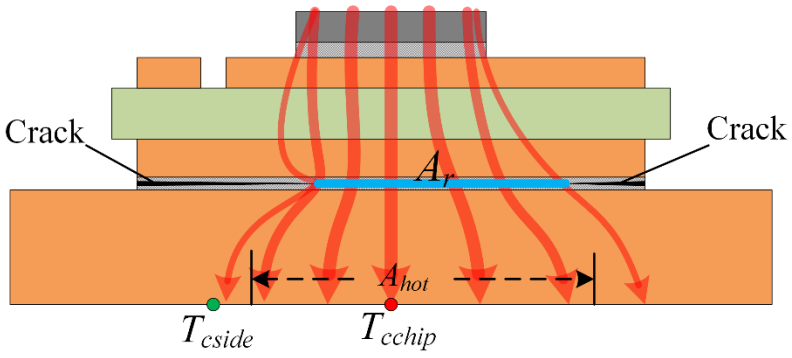


Fig. 5.2: The EHPP in an IGBT module when cracks developed from the edge to the center in the substrate solder layer.

the shrinkage of the A_{hot} can be indicated by an increase in the difference between the case temperature, i.e., T_{cchip}, at a location right beneath the die (i.e., in the middle of the A_{hot}) and the case temperature, i.e., T_{cside}, at a location inside but near the edge of the A_{hot}. If the A_{hot} shrinks, T_{cchip} will increase due to greater concentration of the heat flows, while T_{cside} will drop as its location tends to move out of the A_{hot} or away from the main EHPP. Obviously, it is important to choose appropriate locations at the bottom surface of the baseplate to acquire the nonuniformity of the case temperature distribution related to a change in the EHPP.

However, establishing the relationship between the difference of T_{cchip} and T_{cside}; the remaining noncracking area, A_r, in the substrate solder layer; and the change in the EHPP caused by substrate solder cracks is still not straightforward, as an IGBT module involves multilayer thermal conduction and heat storage and spreading. To establish an effective relationship, this chapter simplifies the problem to a baseplate layer inverse heat conduction problem (IHCP), which utilizes the measurable case temperatures to inversely estimate the remaining noncracking solder area. By neglecting the heat spreading in the thin substrate solder layer, the heat flux flowing through the substrate solder layer to the baseplate is perpendicular to the baseplate top surface. Then, the A_r in the substrate solder layer is equivalent to the heat flux area on the top surface of the baseplate.

Fig. 5.3 shows the change in the heat flux on the baseplate top surface due to the aging of the substrate solder. It is assumed that the cooling condition is stable such that the boundary condition on the bottom surface of the baseplate is stationary. Since the heat flux is concentrated at the center of the baseplate top surface and the total heat propagating through the EHPP at a certain operating condition is specific, the IHCP

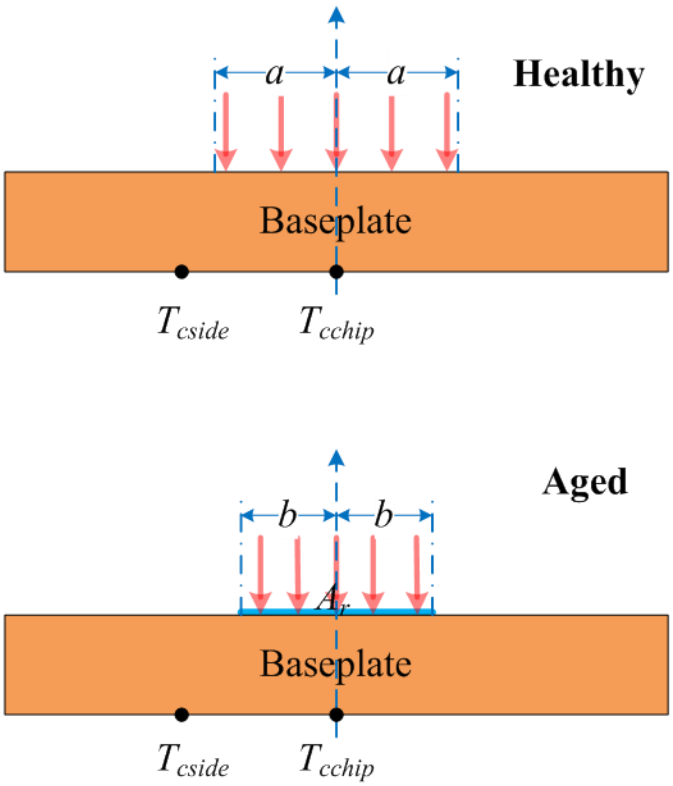


Fig. 5.3: IHCP using case temperature to estimate the effective heat flux area.

solution, A_r, is unique. Thus, a look-up table can be conveniently built via a numerical method, such as FEA, to relate (T_{cchip}−T_{cside}) to A_r for various operating conditions for online applications.

5.2 The EHPP-Based Online Adaptive Thermal Model for IGBT Modules

Once the health condition of the substrate solder of an IGBT module is quantified online using A_r, the next problem is how to model the thermal behavior of the IGBT module adaptively by taking into account the substrate solder aging effect. The FEA method can provide a high-fidelity thermal model which, however, requires extensive time and memory to implement. This dissertation proposes an EHPP-based online

adaptive RC TEC model for IGBT modules. In the proposed model, a traditional RC TEC, e.g., a Cauer-type TEC, is used to physically represent each layer of the EHPP inside an IGBT module. The EHPP, shown as the area within the dashed lines in Fig. 5.4, is approximated by using the heat spreading angle technique [74]. The impact of substrate solder cracks on the thermal behavior of the IGBT module is interpreted via the change in the EHPP. Assuming that only the EHPP through the substrate solder layer and its two adjacent layers, i.e., the substrate copper layer and baseplate layer, is altered by the substrate solder cracks, then the area A_c of the EHPP through the bottom surface of the ceramic layer is constant.

The heat spreading angles, θ, in degrees in the pattern layer and the ceramic layer, can be calculated by [75]:

$$\theta = 90\tanh\left\{0.355\left(\frac{\pi k}{180}\right)^{0.6}\right\} \tag{5.1}$$

where k is the thermal conductivity in W/(m ℃) of the material. The heat spreading angle in the substrate solder layer is neglected owing to the relatively low thermal conductivity of solder and the relatively thin thickness of the substrate solder layer. The heat spreading

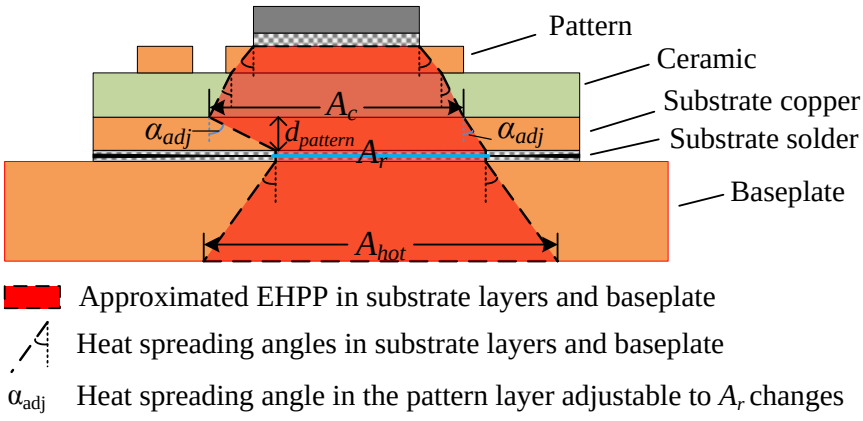


Fig. 5.4: The approximated EHPP for an IGBT module with substrate solder cracks.

angle in the baseplate is cooling-condition dependent and is given as a function of the ratio between the total thickness of all of the heat-spreading layers beneath the chip and the side length of the chip [55]. Therefore, only the heat spreading angle, α_{adj}, in the substrate copper layer needs to be determined according to the status of the substrate solder crack. Once the value of A_r in the substrate solder layer is obtained, α_{adj} can be calculated using the geometry information, A_c and A_r, and the thickness, $d_{pattern}$, of the substrate copper layer.

The thermal resistance of each layer is calculated by:

$$R_{th,i} = \int_0^{d_i} \frac{1}{k_i \cdot A_i(z)} dz \tag{5.2}$$

where $R_{th,i}$, d_i, k_i, and z are the thermal resistance, thickness, thermal conductivity of the material, and vertical distance from the top surface to the bottom surface of the ith layer, respectively; and $A_i(z)$ is the horizontal cross-section area at a distance z, which is calculated according to the geometry information, including the heat spreading angle, of the layer. The calculation for the thermal capacitance of each layer, however, is not straightforward. Detailed information on the calculation of thermal impedances of electronic packaging can be found in [30], [76].

The approximated EHPP in the substrate solder layer and the adjacent copper layer and baseplate is adjusted according to A_r. Based on the approximated EHPP, the RC parameters of the three layers can be adjusted for the Cauer-type TEC, leading to an adaptive thermal model. The schematic of the proposed online adaptive TEC model is illustrated in Fig. 5.5, where I_c, f_{sw}, PF, P_{loss}, and T_a are the collector current, switching frequency, power factor, power loss, and ambient temperature of the IGBT module, respectively.

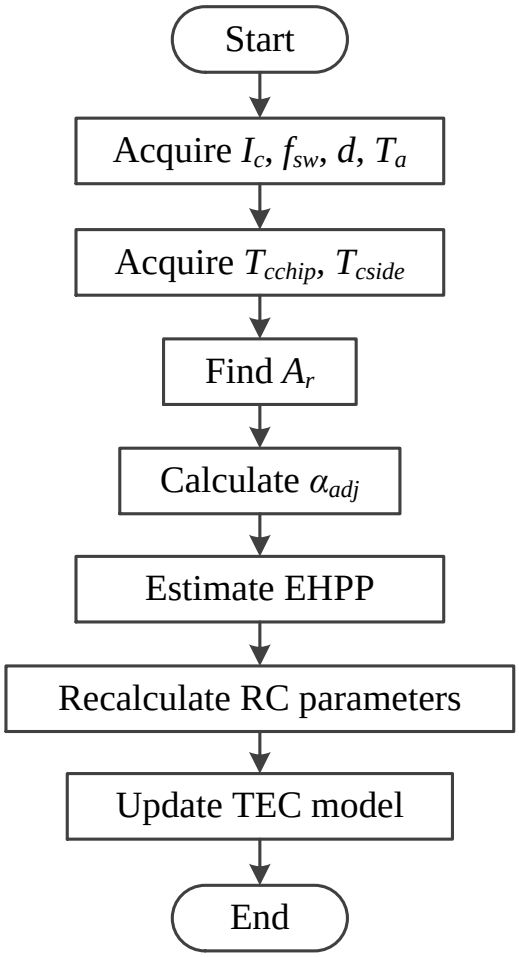


Fig. 5.5: Schematic of the proposed online adaptive TEC model.

5.3 Simulation Validation

A commercial IGBT module, CM1400DU-24NF, made by Powerex was studied to validate the proposed EHPP-based adaptive RC TEC model. The geometry information of the module was provided by Powerex. The IGBT module was in a half-bridge configuration. Each IGBT switch consisted of nine parallel dies placed on three DBC transistor stacks. Taking advantage of the symmetry of the stack layout, one-sixth of the module (41.5 mm × 75 mm), i.e., a thermal stack with three IGBT dies, was built in ADINA, a commercial FEA software platform, as shown in Fig. 5.6. The cold plate

was simplified to an aluminum block with the bottom surface temperature set to be the inlet coolant temperature. The thermal interface between the baseplate and the cold plate was a thermal grease layer with a thickness of 0.1 mm.

The substrate solder was assumed to have a uniform crack from the edge to the center. Fig. 5.7 illustrates the geometry of the module viewed from the baseplate with the locations of the case temperature measuring points. Since the three dies were connected in parallel in one switch, the power losses in the three dies were assumed to be the same. The EHPP of the center die was assumed to be unchanged during the substrate solder cracking process. The approximated EHPPs of the three dies, as shown in Fig. 5.8, are separated by dashed lines. It should be noted that Fig. 5.8 is for illustration purposes only and does not reflect the real geometry of the module.

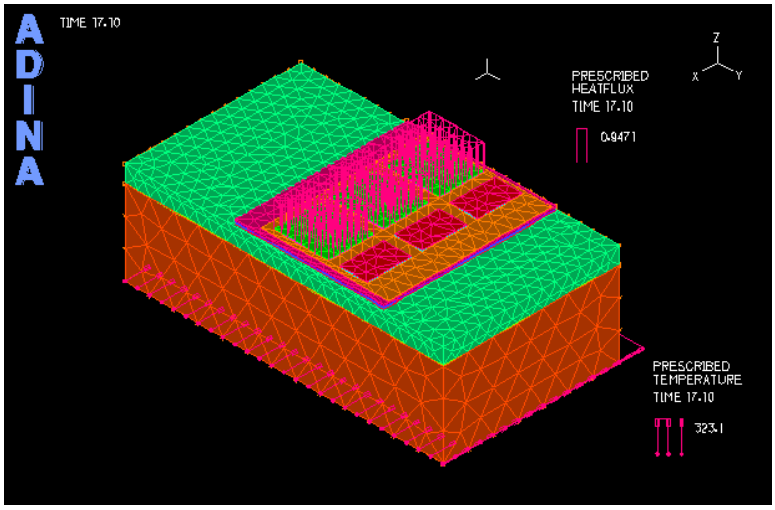


Fig. 5.6: The model of one-sixth of a CM1400 IGBT module built in ADINA.

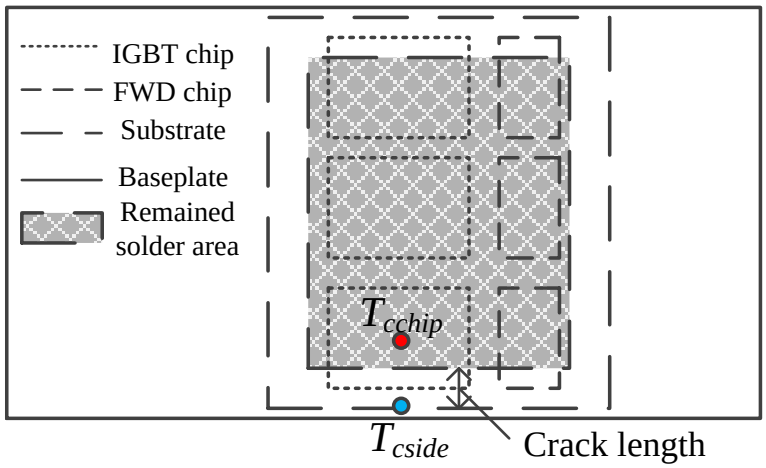


Fig. 5.7: Baseplate side view of the IGBT module.

The effectiveness of using the nonuniformity of the case temperature distribution (T_{cchip}−T_{cside}) as an indicator of substrate aging was evaluated for three solder crack cases at two specific operating conditions using the FEA method. The first operating condition was a constant load, i.e., constant power loss, case, where the test IGBT was conducted long enough to reach a steady-state temperature. The second operating condition was a dynamic load case, where the test IGBT was operated as a leg in a three-phase inverter with the collector current I_c = 450 A, switching frequency f_{sw} = 2 kHz, and power factor PF = 0.85. The AC output frequency of the inverter was 1 Hz, as an accurate thermal

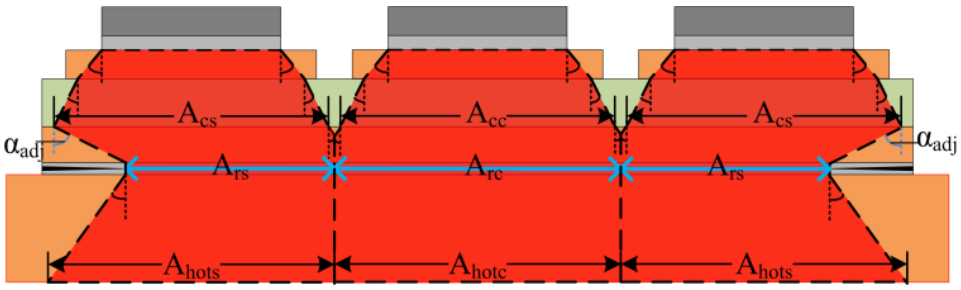


Fig. 5.8: EHPPs of the side dies and the center die (separated by dashed lines).

modeling of the IGBT module is important as the IGBT undergoes more severe thermal stress under a low-frequency load [77]. The power loss profiles of one die for the two load conditions are shown in Fig. 5.9, where the power loss was averaged over each switching period in the dynamic load case. Fig. 5.10 shows the changes in nonuniformity of the case temperature distribution ($T_{cchip}-T_{cside}$) and the changes in maximum junction temperature, $T_{jmax,side}$, of the side die for different solder crack cases with respect to those of the healthy case. The case temperature was acquired after the maximum junction temperature was reached while considering the phase delay between the power loss and the measured case temperatures.

It can be seen that nonuniformity of the case temperature distribution and the junction temperature increased with the development of the substrate solder crack in both constant and dynamic load conditions. The increases in ($T_{cchip}-T_{cside}$) and $T_{jmax,side}$ in the 1.75-mm solder crack case were noticeable. However, in the other two cases where the

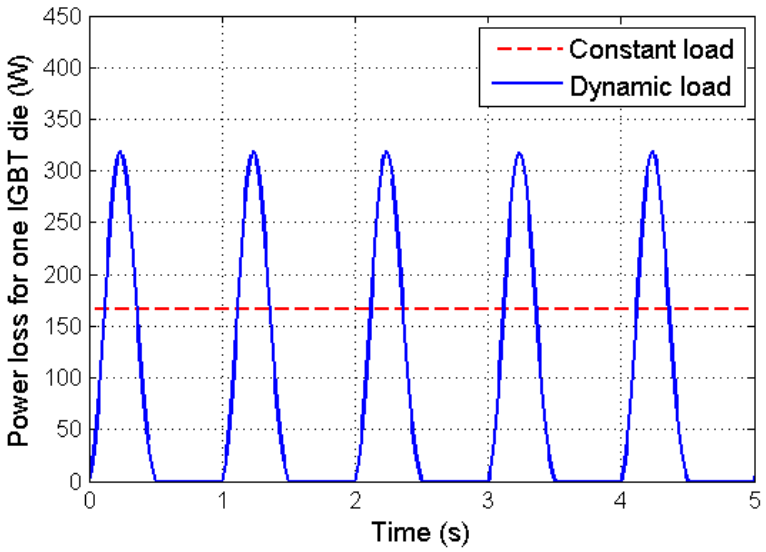


Fig. 5.9: Power loss profiles of constant load and dynamic load cases for one IGBT chip.

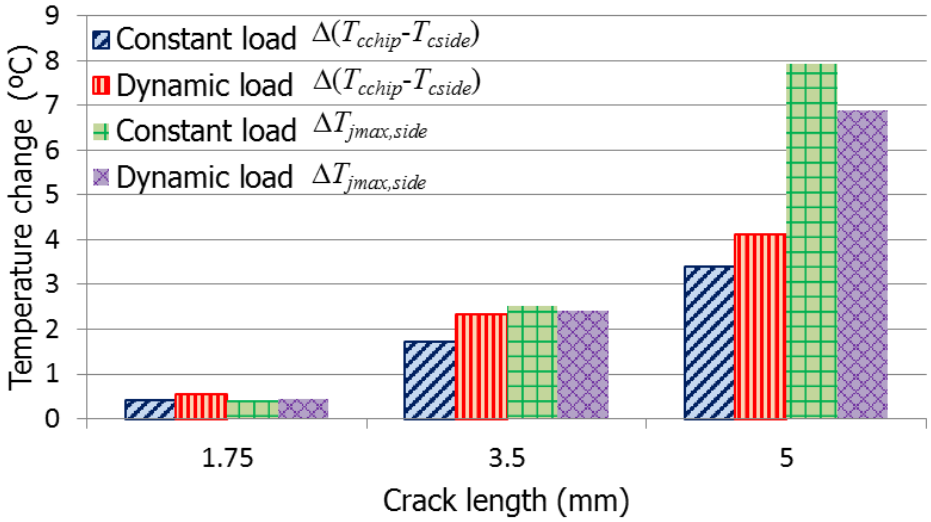


Fig. 5.10: Changes in nonuniformity of the case temperature distribution and maximum junction temperature in the three substrate solder crack cases in constant and dynamic load conditions.

solder cracks became more severe, both (T_{cchip}−T_{cside}) and $T_{jmax,side}$ increased more noticeably. These results proved that (T_{cchip}−T_{cside}) is a sensitive indicator of the substrate solder aging process.

The thermal resistance $R_{thja,side}$ of the side die was a key concern, since the solder crack would first encroach the EHPP of the side die. Using the proposed method, the value of $R_{thja,side}$ was calculated. The thermal resistance of the thermal grease layer was also calculated by using (5.2). However, the heat spreading in the thermal grease layer was neglected; and, therefore, the cross-section area was equal to A_{hot}. The change in thermal resistance of the cold plate was not considered due to its negligible impact on the total thermal resistance. Fig. 5.11 compares the values of $R_{thja,side}$ calculated by the FEA method and the proposed model. The results showed a good match between the two models, where the error between the two models was less than 2%.

To examine the performance of the proposed model for adaptive dynamic junction temperature estimation, the results obtained from the FEA method, the proposed adaptive model, and the traditional Cauer-type TEC model without parameter adaption (i.e., using the fixed parameters extracted for the IGBT in the healthy condition) are compared in Fig. 5.12 under the dynamic load condition for the 3.5-mm crack and 5-mm crack cases. The relative error was defined as the ratio between the absolute error of the junction temperature estimated by the proposed model or the traditional Cauer-type TEC model with respect to the junction temperature obtained from the FEA method and the mean value of the junction temperature rise from coolant temperature estimated from the FEA method. The maximum error between the proposed model and the FEA model was less than 4 ℃, and the relative errors were within 5% during most of the simulations in both cases. On the other hand, the maximum error between the traditional Cauer-type TEC model and the FEA model is more than 7℃, and the relative errors are much larger

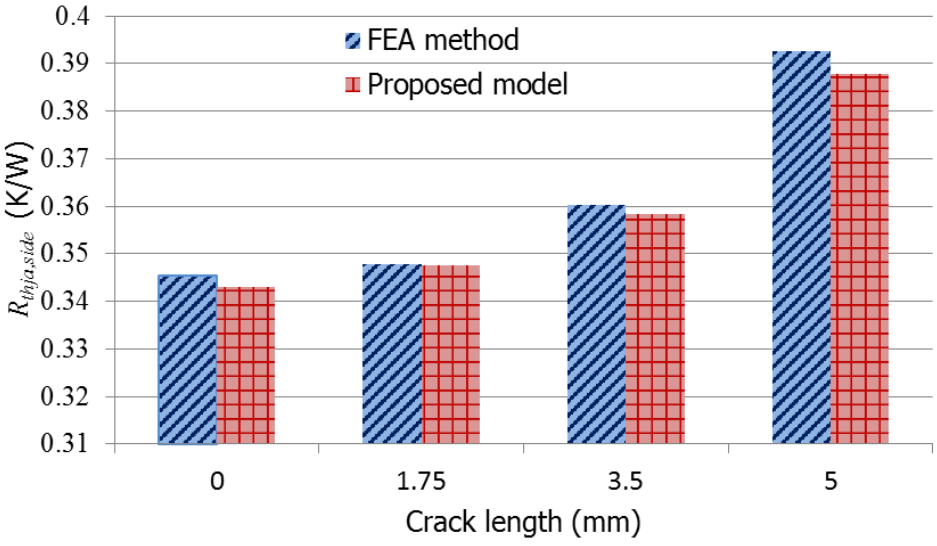


Fig. 5.11: Comparison of $R_{thja,side}$ calculated by the FEA method and the proposed model.

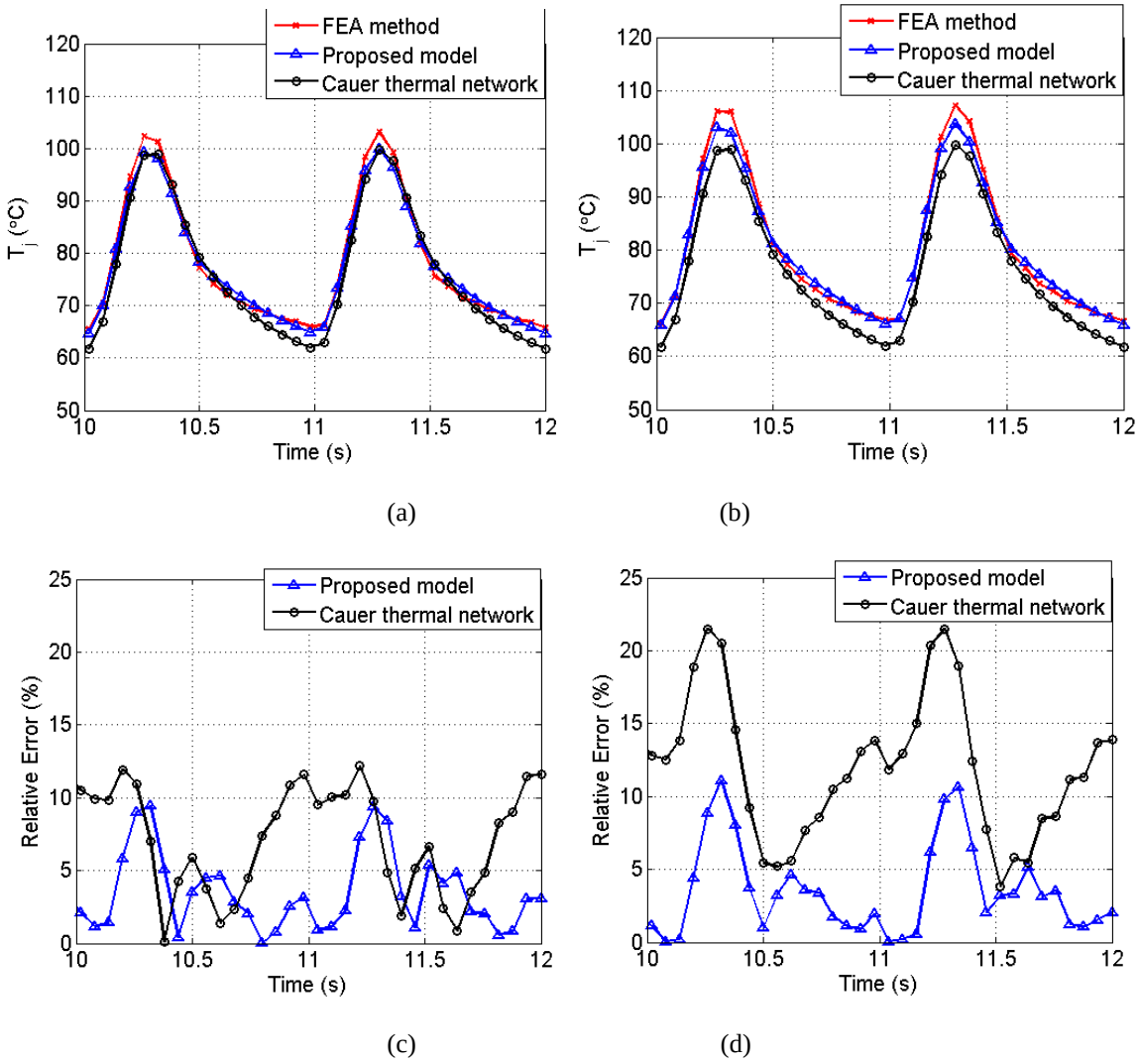


Fig. 5.12: Comparison of different models for the cases of 3.5-mm solder cracks and 5-mm solder cracks under the dynamic load condition: (a) junction temperature (3.5-mm solder crack); (b) junction temperature (5-mm solder crack); (c) relative error (3.5-mm solder crack); and (d) relative error (5-mm solder crack).

than those of the proposed model. These results clearly show that the proposed adaptive thermal model is much better than the traditional TEC models for junction temperature prediction as the proposed model includes the substrate solder aging effect by using the proposed EHPP method.

5.4 Summary

This chapter presented an EHPP-based RC TEC model for IGBT modules, where the parameters were adapted online to substrate solder cracks inside the IGBT modules. The concept of EHPP was introduced to effectively characterize the thermal behavior of IGBT modules using the heat spreading angle technique. The impact of substrate solder cracks on the thermal behavior of an IGBT module was interpreted by using the change in the EHPP as approximated based on the change in the nonuniformity of the case temperature distribution. The approximated EHPP was then used to adapt the RC parameters of the TEC online. Numerical simulation studies validated the effectiveness of using the nonuniformity of the case temperature distribution to indicate the severity of substrate solder cracks and the effectiveness of using the proposed adaptive thermal model to achieve improved junction temperature estimation with respect to traditional TEC models. The proposed model can be used for effective online condition monitoring, control, and thermal and health management of IGBTs and associated power electronic systems.

Chapter 6. Real-Time Health Monitoring for IGBT Modules Using Case Temperatures

The major aging mechanisms in an IGBT module have two thermal consequences. First, some aging processes, e.g., bond wire liftoff and metallization degradation, lead to an increase in V_{CEon} and, therefore, an increase in power loss and heat generation in the IGBT module. Moreover, some aging processes, such as substrate solder crack, will deteriorate heat propagation inside an IGBT module, causing an elevation of T_j. Compared to electrical parameters, the changes in power converter temperature are much slower and, therefore, can be more easily captured online. As a temperature signal consists of relatively low frequency components, the measurement noises can be easily filtered out. However, except for T_j, which is difficult to measure directly, other temperatures have rarely been used for monitoring the aging of IGBT modules.

This dissertation proposes a new method of using two-dimensional (2D) case temperature for monitoring the aging of substrate solder, bond wires, and emitter metallization in IGBT modules in real time [78]. The proposed method is based on two facts: 1) substrate solder aging alters the heat flow inside an IGBT module and, therefore, the nonuniformity of the 2D case temperature distribution [61]; and 2) the bond wire and emitter metallization aging increases V_{CEon} and, therefore, the power loss of an IGBT module.

The proposed method first characterizes the nonuniformity of the 2D case temperature distribution in order to monitor substrate solder aging. Then, the proposed method utilizes linear system analysis of the thermal behavior of the IGBT module to determine the increase in heat generation, from which the increase in V_{CEon} is obtained to monitor bond wire and emitter metallization aging. In practical applications of the proposed method, different aging processes of an IGBT module can be monitored separately by placing two thermal sensors for each switch at the interface between the baseplate of the IGBT module and the cold plate.

To the authors' knowledge, this is the first work which uses 2D case temperatures to monitor online the major aging processes in IGBT modules. The proposed method was validated by simulation and experimental results for a commercial IGBT module.

6.1 Linear Thermal Behavior of IGBT Modules

Although the aging processes of IGBT modules are mainly driven by thermal-related stresses and result in changes in the heat generation and temperature of IGBT modules, thermal parameters have rarely been used as precursors for monitoring the aging of IGBT modules. This is partly due to the difficulty in obtaining accurate information on some important thermal parameters, such as the T_j, during the operation and aging of IGBT modules. Moreover, some easy-to-measure temperatures, such as T_c, have not received enough attention in regard to monitoring the aging of IGBT modules. This might be due to the lack of a thorough study on the changes in thermal behavior caused by major aging mechanisms and the complexity in thermal modeling for IGBT modules. The linear thermal behavior of IGBT modules is discussed in this section. This discussion will serve as the basis for establishing the principle of the proposed method of

using 2D case temperatures for real-time monitoring of the major aging processes of IGBT modules.

An IGBT module typically has a multilayered structure. The thermal behavior of an IGBT module is complex due to the complex geometry and differences in the materials' properties. The thermal behavior of an IGBT module in a certain health condition can be accurately modeled by a high-order, 3D, Cauer-type RC TEC based on the geometry and materials of the module. The RC parameters of the thermal model are assumed to be constant if the performance of the cooling system is stable and the IGBT works with the junction temperature in the allowed operating range in which variations of the materials' thermal properties, caused by junction temperature variations (called the temperature effect), are negligible. Under this circumstance, the thermal behavior of the IGBT module is linear during normal operation. Thus, the superposition principle can be used to model the temperature rise from the coolant to any point in the IGBT module caused by multiple sources of power loss in the IGBT module, such as the IGBT chips and the free-wheeling diode (FWD) chips. Since the power losses generated by the FWD chips are relatively small and their contribution to the case temperature rise as the IGBT module ages is negligible, only the power losses generated by IGBT chips are considered during the aging process. Then, as the thermal behavior of the IGBT module changes over time during the aging process, the temperature rise (from ambient to any point at the case) of the IGBT module has a linear time-varying relationship with the total power loss generated by the IGBT chips.

6.2 2D Case Temperature-Based Monitoring of IGBT Module Aging

The power loss, $P_{loss}(T_j)$, of a switch in an IGBT module includes the conduction loss, $P_{Closs}(T_j)$, and the switching loss, $P_{SWloss}(T_j)$, of the switch, which typically consists of multiple chips in parallel. The power losses depend on T_j, which is difficult to measure in practice. The values of T_j and $P_{loss}(T_j)$ change with the aging of the IGBT module. The initial power loss, $\hat{P}_{loss}(\hat{T}_j)$ (including $\hat{P}_{Closs}(\hat{T}_j)$ and $\hat{P}_{SWloss}(\hat{T}_j)$), and initial junction temperature, $\hat{T}_j$, are the values of the IGBT module when it is new (healthy); and they do not change with the aging of the IGBT module. The values of $\hat{P}_{loss}(\hat{T}_j)$ and $\hat{T}_j$ can be obtained by an iterative electrothermal modeling process using the datasheet parameters of the IGBT module, the power loss calculation equations in [62] or a power loss lookup table, and a thermal model for the IGBT module and the cold plate. When the IGBT module is healthy, the initial $\hat{T}_j$ is the same as T_j, then

$$P_{loss}(T_j) = \hat{P}_{loss}(\hat{T}_j) \tag{6.1}$$

Unlike the junction temperature, the case temperature of an IGBT module can be directly measured and, therefore, is a good thermal parameter for monitoring the aging of IGBT modules in practical applications. First, consider a 1D RC TEC, in which the relationship between the steady-state 1D case temperature, T_c, and $P_{loss}(T_j)$ is given by

$$T_c = P_{loss}(T_j) \cdot R_{thca} + T_a \tag{6.2}$$

where R_{thca} is the thermal resistance from case to ambient.

According to (6.2), a change in T_c reflects a change in the power loss and/or R_{thca} during the aging process. However, T_c in (6.2) represents the average case temperature, which is difficult to measure by using one or multiple thermal sensors in practice, especially when the nonuniformity of the case temperature distribution changes during

the aging process of the substrate solder [61]. To solve the problem of using a 1D case temperature, this dissertation proposes to monitor the major aging processes of an IGBT module by using 2D case temperatures.

An IGBT module cooled by a cold plate with selected points for 2D case temperature measurements is illustrated in Fig. 6.1. Assuming that the IGBT module has linear thermal behavior, the steady-state temperature, T_{cp}, at any point $p(x, y)$ on the bottom surface of the baseplate can be expressed by the following equation

$$T_{cp} - T_a = R_{eqcp} \cdot P_{loss}(T_j) \tag{6.3}$$

where R_{eqcp} is the equivalent thermal resistance characterizing the temperature rise from ambient to the point p when the IGBT module has a certain power loss, $P_{loss}(T_j)$. Equation (6.3) can be extended to the steady-state 2D case temperatures, $\mathbf{T}_C$, for all of the points of interest on the baseplate as follows:

$$\mathbf{T}_C - T_a \cdot \mathbf{J} = \mathbf{R}_{eqC} \cdot P_{loss}(T_j) \tag{6.4}$$

where $\mathbf{J}$ is the matrix of ones, and $\mathbf{R}_{eqC}$ is the matrix of the equivalent thermal resistances

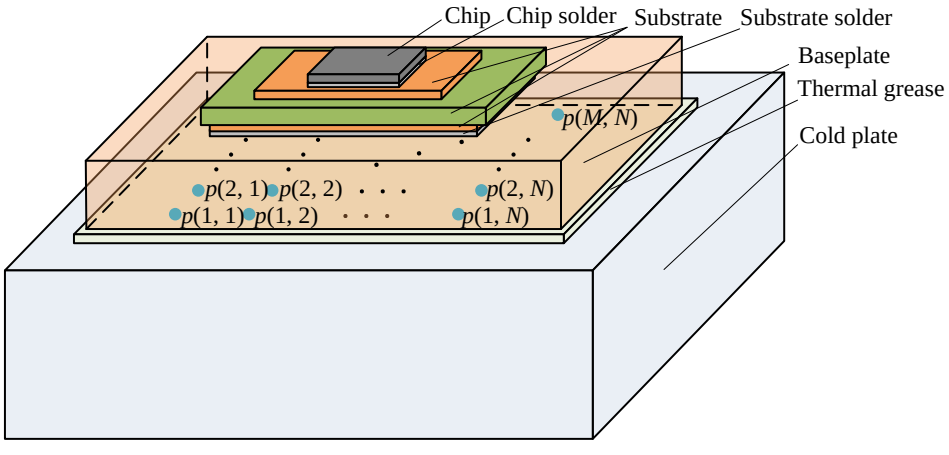


Fig. 6.1: An IGBT module cooled by a cold plate
with selected points for 2D case temperature measurements.

from the points of interest on the 2D bottom surface of the baseplate to ambient. The aging processes of an IGBT module result in changes in $\mathbf{R}_{eqC}$ and/or $P_{loss}(T_j)$. This dissertation proposes a method of using the measured $\mathbf{T}_C$ and T_a to monitor the changes in $\mathbf{R}_{eqC}$ and $P_{loss}(T_j)$ by (6.4) for real-time monitoring of the major aging processes of IGBT modules.

6.2.1 Substrate Solder Aging

The fatigue of solder joints is a major failure mechanism of IGBT modules. Compared to the chip solder, the substrate solder is more critically subject to fatigue, commonly leading to solder cracks [63]. Substrate solder cracks shrink the area for heat conduction in the substrate layer, which deteriorates the heat propagation inside the IGBT module and increases the value of R_{thjc}. This will intensify the nonuniformity of the case temperature distribution at the bottom surface of the baseplate [61]. As a consequence, $\mathbf{R}_{eqC}$ changes over time during the substrate solder aging process. The ratio (k_{hc}) between an element R_{eqCh} of the matrix $\mathbf{R}_{eqC}$ for a hot spot $h(x_1, y_1)$ and an element R_{eqCc} of $\mathbf{R}_{eqC}$ for a relatively cold point $c(x_2, y_2)$ on the baseplate is defined as.

$$k_{hc} = \frac{R_{eqCh}}{R_{eqCc}} \tag{6.5}$$

The value of k_{hc} characterizes the impact of the alternation of the heat flow inside an IGBT module caused by substrate solder aging on the nonuniformity of the 2D case temperature distribution. As the substrate solder ages, the value of k_{hc} increases over time. Therefore, k_{hc} is a good parameter for real-time monitoring of the substrate solder aging process. An advantage of using k_{hc} is that it is independent of the operating condition of the IGBT module.

6.2.2 Bond Wire and Emitter Metallization Aging

The aging of bond wires and metallization in an IGBT module results in an increase of V_{CEon} and, therefore, an increase in the total conduction loss of IGBT chips in a switch. A commonly used criterion indicating that the bond wire and emitter metallization are aged is that V_{CEon} has increased by 10~20% [64], which corresponds to a 10~20% increase in conduction loss. During this aging process, $\mathbf{R}_{eqC}$ is constant, while $P_{loss}(T_j)$ increases over time. By monitoring $\mathbf{T}_C$ and T_a, $P_{loss}(T_j)$ can be estimated using (6.4). As the switching loss can be calculated using the equations in [62] with the information of T_j, the conduction loss can be obtained; and then V_{CEon} can be calculated [62] to examine the aging condition of the bond wires and emitter metallization.

6.2.3 Mixed Aging Mode of Bond Wires, Metallization, and Substrate Solder

When an IGBT module undergoes multiple aging processes, both $P_{loss}(T_j)$ and $\mathbf{R}_{eqC}$ may change over time. Let α_P be the ratio between $P_{loss}(T_j)$ and $\hat{P}_{loss}(\hat{T}_j)$,

$$P_{loss}(T_j) = \alpha_P \cdot \hat{P}_{loss}(\hat{T}_j) \tag{6.6}$$

Let $\hat{\mathbf{R}}_{eqC}$ be the matrix of the equivalent thermal resistances from the points of the 2D case temperature measurements to ambient estimated by (6.4) using $\hat{P}_{loss}(\hat{T}_j)$ and $\mathbf{T}_C$. Then, according to (6.4) and (6.6), the relation between $\hat{\mathbf{R}}_{eqC}$ and $\mathbf{R}_{eqC}$ can be obtained:

$$\hat{\mathbf{R}}_{eqC} = \frac{\mathbf{T}_c - T_a \cdot \mathbf{J}}{\hat{P}_{loss}(\hat{T}_j)} = \alpha_P \cdot \frac{\mathbf{T}_c - T_a \cdot \mathbf{J}}{P_{loss}(T_j)} = \alpha_P \cdot \mathbf{R}_{eqC} \tag{6.7}$$

According to (6.7), $\hat{\mathbf{R}}_{eqC}$ is proportional to $\mathbf{R}_{eqC}$ by a scalar α_P. This indicates that other than using $\mathbf{R}_{eqC}$, it is equivalent to use $\hat{\mathbf{R}}_{eqC}$ to obtain k_{hc} in (6.5) for monitoring the aging of the substrate solder without the need for using the $P_{loss}(T_j)$.

Moreover, since k_{hc} only changes with the aging process of the substrate solder but is independent of the operating condition of the IGBT module, the relationships between k_{hc} and $\mathbf{R}_{eqC}$ and between k_{hc} and R_{thjc} can be easily characterized. For example, such relations can be obtained by recording the evolutions of k_{hc}, $\mathbf{R}_{eqC}$, and R_{thjc} over time at a certain operating condition using an offline substrate solder aging test and stored in a lookup table. Then, according to k_{hc}, the values of $\mathbf{R}_{eqC}$ and R_{thjc} can be obtained in real time for various operating conditions of the IGBT module even when a mixed mode aging process occurs in the IGBT module.

Once $\mathbf{R}_{eqC}$ is known, α_P can be calculated by using (6.7). Then, the power loss, P_{loss}, can be calculated from (6.6) using $\hat{P}_{loss}$ and α_P. In addition, according to the linear thermal behavior of the IGBT module, T_j and the corresponding change in the total power loss, $\Delta P_{loss}(T_j)$, during the aging process can be updated by using (6.8) and (6.9), respectively.

$$T_j = \alpha_P \cdot \hat{P}_{loss}\left(\hat{T}_j\right) \cdot \left(R_{thjc} + R_{thca}\right) + T_a \tag{6.8}$$

$$\Delta P_{loss}(T_j) = P_{loss}\left(T_j\right) - \hat{P}_{loss}\left(T_j\right) \tag{6.9}$$

The use of the updated T_j to recalculate $\hat{P}_{loss}$ in (6.9) removes the power loss increase caused by the rise of the junction temperature from $\Delta P_{loss}(T_j)$, and the resulting $\Delta P_{loss}(T_j)$ only reflects the aging of bond wires and emitter metallization. Then, the change of V_{CEon} at T_j, $\Delta V_{CEon}(T_j)$, is obtained by using (6.10) to monitor the aging processes of bond wires and emitter metallization:

$$\Delta V_{CEon}\left(T_j\right) = \frac{\Delta P_{loss}(T_j)}{\hat{P}_{Closs}(T_j)} \tag{6.10}$$

The changes of the key parameters for different aging mechanisms are summarized in Table 6.1, where α_P may increase during the aging process of the substrate

solder because of the elevation of T_j, which increases the power loss generation. Table 6.1 clearly shows that by monitoring these parameters online, not only the aging of the IGBT module can be detected but also the aging mechanism(s) can be identified.

6.2.4 Other Major Aging Mechanisms

Since the DBC layers have good heat spreading properties, the shrinking or alternation of the heat conduction area caused by a crack or void in the chip solder typically has a negligible impact on $\mathbf{R}_{eqC}$ and, therefore, does not alter the nonuniformity of the case temperature distribution. However, if an aging mechanism causes an increase in P_{loss} but does not change $\mathbf{R}_{eqC}$, then according to the linear thermal behavior expressed by (6.7), the aging process can be monitored by the increase in ($\mathbf{T}_C - T_a \cdot \mathbf{J}$) indirectly.

6.3 Implementation of the Proposed Method

A simple implementation of the proposed method is to place two thermal sensors, such as thermocouples, for each switch on the bottom surface of the baseplate of an IGBT module. One sensor should be placed at the hot spot, e.g., underneath an IGBT chip of the switch, to monitor the case temperature, T_{cchip}, which is most sensitive to the changes in $P_{loss}(T_j)$. The other sensor should be placed somewhere away from the hot spot to monitor the case temperature, T_{cside}. For example, the placement of thermal sensors for a three-phase inverter module having six IGBT switches is illustrated in Fig. 6.2. The use

Table 6.1: Changes of key parameters for different aging mechanisms.

Aging Mechanisms	P_{loss}	k_{hc}	α_P
Bond wire, emitter	Increase	Constant	Increase
Substrate solder	Rely on T_j	Increase	Rely on T_j
Mixed mode aging	Increase	Increase	Increase

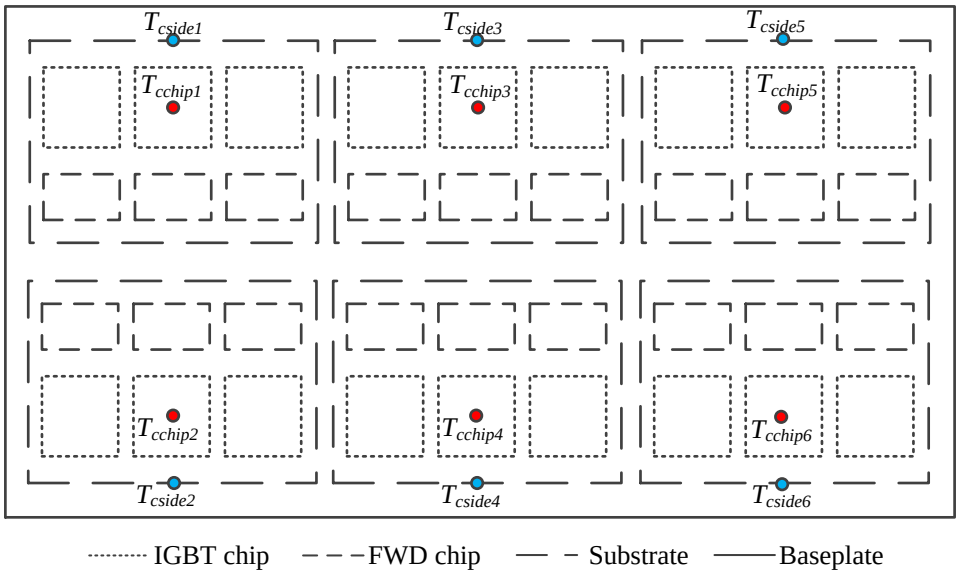


Fig. 6.2: The placement of thermal sensors on the bottom surface of the baseplate of a three-phase inverter module having six IGBT switches.

of thermocouples to measure temperature was discussed in [65]. The temperature signals measured are compensated and analog-to-digital converted by using an integrated circuit (IC), such as MAX31855 [66].

For one IGBT switch, the ratio k_{cs} (a specific case of k_{hc}) between the equivalent thermal resistances from the two selected points to ambient is used to evaluate the nonuniformity of the case temperature distribution, which is solely related to the alternation of the heat flow inside the IGBT module caused by the substrate solder aging:

$$k_{cs} = \frac{\hat{R}_{eqCchip}}{\hat{R}_{eqCside}} = \frac{R_{eqCchip}}{R_{eqCside}} \tag{6.11}$$

where $\hat{R}_{eqCchip}$ and $\hat{R}_{eqCside}$ are the equivalent thermal resistances from the two selected points to ambient, respectively, estimated from (6.7) using $\hat{P}_{loss}(\hat{T}_j)$ and measured T_a, T_{cchip}, and T_{cside}; $R_{eqCchip}$ and $R_{eqCside}$ are the corresponding actual equivalent thermal resistances. Since the values of k_{cs} of all the six switches are independent of the operating

condition of the IGBT module, it can be used for real-time monitoring of the substrate solder for various operating conditions of the IGBT module. When the IGBT module experiences a mixed mode aging process, the change of V_{CEon} over time can be obtained in real time according to the procedure described in Section 6.2.3 for monitoring the aging processes of bond wires, emitter metallization, etc. Since the case temperatures do not vary quickly, a short period steady state can be found in practice for the execution of the proposed method. The flowchart of the proposed method is shown in Fig. 6.3, where d is the duty ratio and K is typically in the range of 15-20.

The proposed method is capable of monitoring the major aging modes separately by separating the changes in case temperature caused by the increase of the power loss from those caused by the heat flow change during the aging process of the IGBT module. The method in [53] only uses a one point case temperature to detect the rise of the power loss for solder age monitoring. This, however, can be erroneous because an increase in the one point case temperature can be a result of an increase in the power loss or an alteration of the heat flow inside the IGBT module.

The scope of this work is monitoring the aging of IGBT modules, which does not consider the degradation of the thermal grease between the IGBT module and the cold plate. The issue of thermal grease degradation was discussed in [67], [68] and can be easily addressed by regular maintenance [67]. The inspection and maintenance for thermal grease is much easier than that for IGBT modules. Moreover, the recent development in thermal interface materials has dramatically improved the reliability of the thermal interface between the IGBT module and the cold plate [69]. With proper

thermal grease maintenance, the potential impact of thermal grease degradation on the proposed method can be safely eliminated.

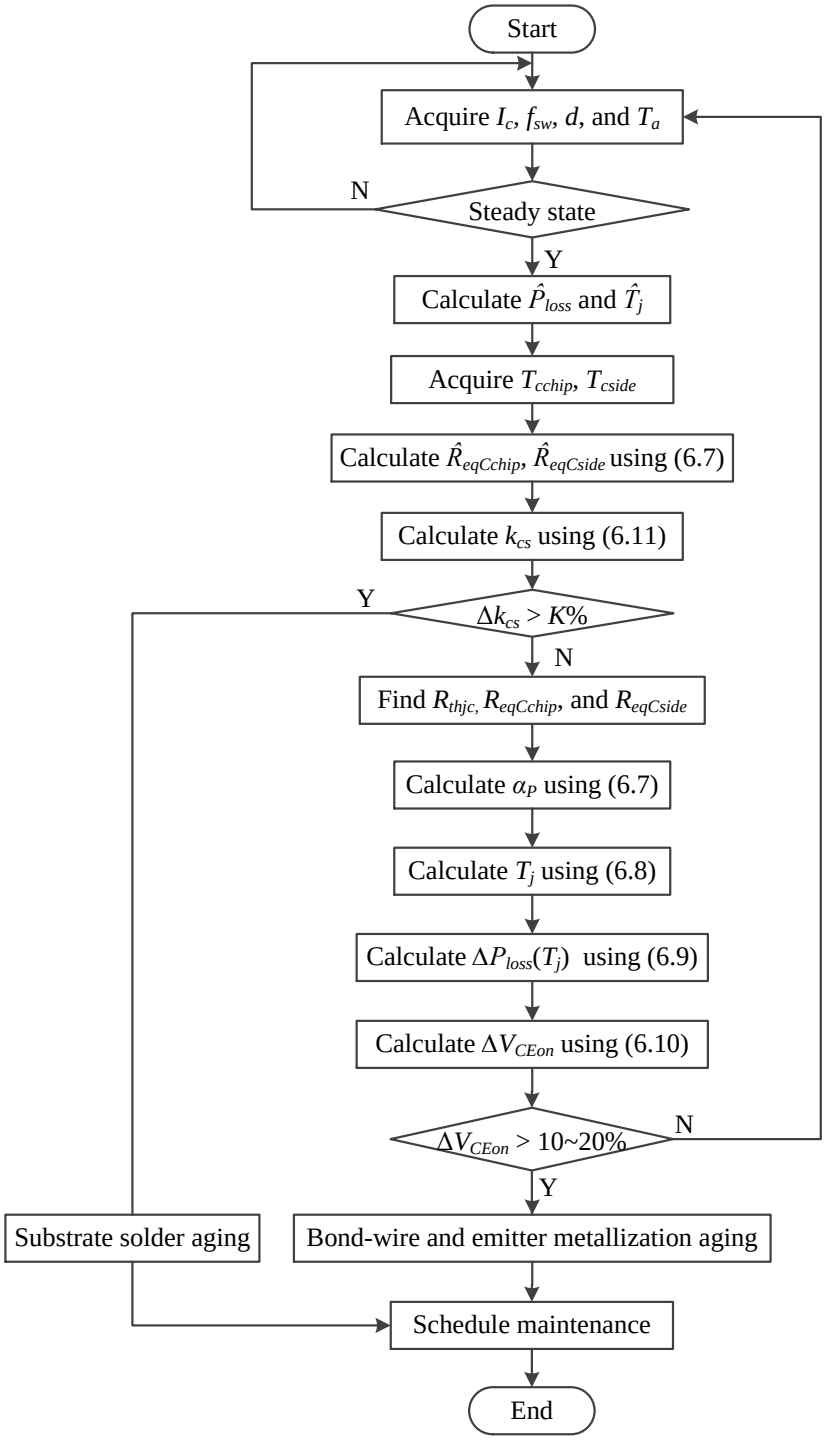


Fig. 6.3: The flowchart of the implementation of the aging monitoring method using two case temperatures.

6.4 Simulation Validation

The commercial IGBT module CM400DY-12NF made by Powerex (described in Chapter 3) was studied to validate the proposed case-temperature-based, real-time monitoring method for aging of IGBT modules. Two points at the bottom surface of the baseplate of the IGBT module, one underneath an IGBT chip and the other underneath the edge of the substrate solder layer, were selected for measuring the case temperature, as shown in Fig. 6.4.

The same FEA model of the test IGBT module built in Autodesk Simulation Multiphysics, described in Chapter 3, was used. The temperature of the pipes was set to be the inlet coolant temperature of 20 ºC, i.e., T_a = 20 ºC. The IGBT module was operated as a leg in a two-level three-phase inverter with the following operating conditions: the DC-link voltage was 400 V, I_c = 400 A, f_{sw} = 5 kHz, the power factor PF

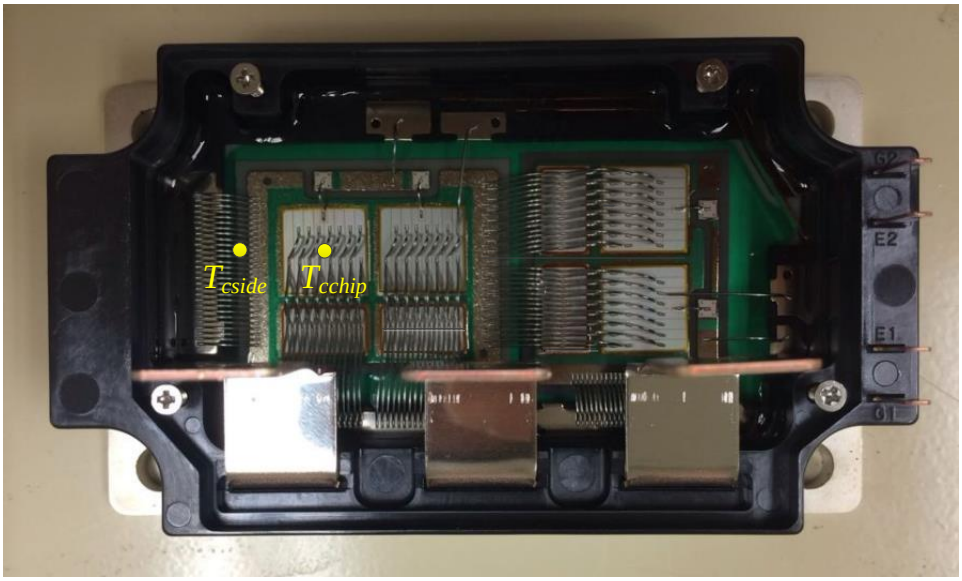
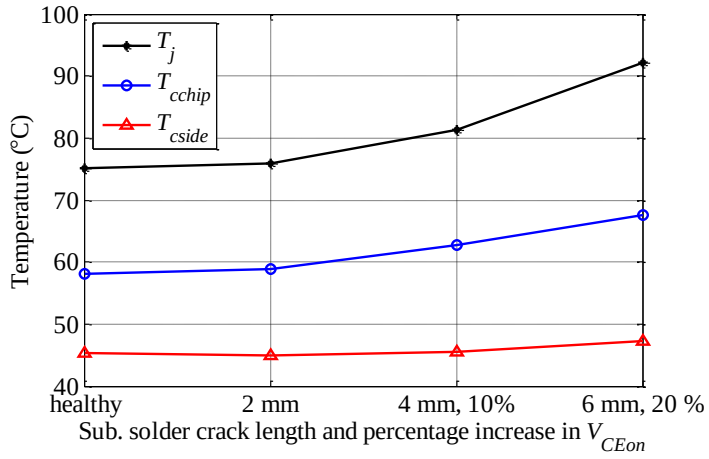


Fig. 6.4: The test IGBT module with the positions of the two thermal sensors placed on the bottom surface of the baseplate (top view from the upper side of the module).

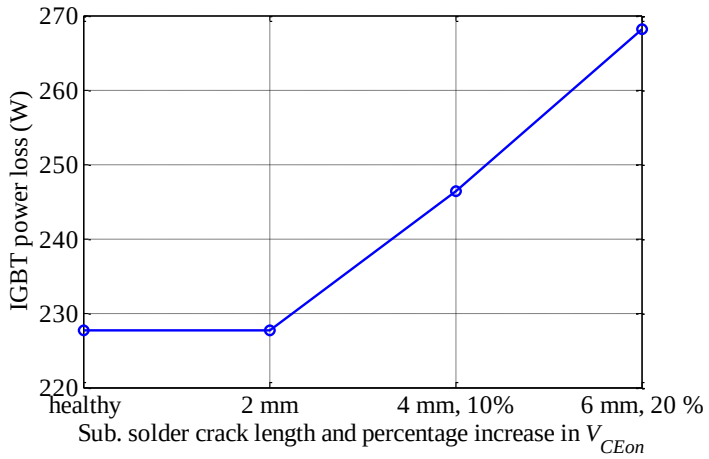
= 0.8, a unity modulation index, and 60 Hz line frequency.

When the IGBT module was healthy, the initial junction temperature was 75.2 °C; and the corresponding initial power losses of the IGBT chips and the FWD chips in a switch were calculated to be 227.63 W and 42.52 W, respectively, using the equations in [62]. The initial switching loss of the IGBT switch was 69.48 W, which increased during the aging process as the junction temperature increased. Then, based on (6.6), (6.9), and (6.10), the increase in α_P related to the increase in V_{CEon} could be obtained. The losses of the FWD elevated T_{cchip} and T_{cside} by approximately 4.7 °C and 3.4 °C, respectively, which were almost constant throughout the aging process of the IGBT module due to a relatively long distance between the FWD and the two selected points on the baseplate and the relatively small values of the FWD losses. In practice, the case temperature increases caused by the FWD losses should be removed to perform the proposed method, which can be easily implemented by applying superposition.

The aging processes of the substrate solder, bond wires, and emitter metallization of the IGBT module were simulated. Snapshots were taken in the following four scenarios to show the aging development in the IGBT module: 1) healthy condition, 2) a minor aging in the substrate solder with a 2 mm crack, 3) an intermediate aging of the substrate solder with a 4 mm crack and an aging of bond wires and emitter metallization mimicked by a 10% increase in V_{CEon}, and 4) a dangerous aging status with a 6 mm crack in the substrate solder and a 20% increase in V_{CEon}. The substrate solder cracks were assumed to be uniform from the edge to the center. The measured T_{cchip} and T_{cside} and the calculated T_j, R_{thjc}, and P_{loss} in the four scenarios during the simulated aging process of the IGBT module are shown in Fig. 6.5.



(a)



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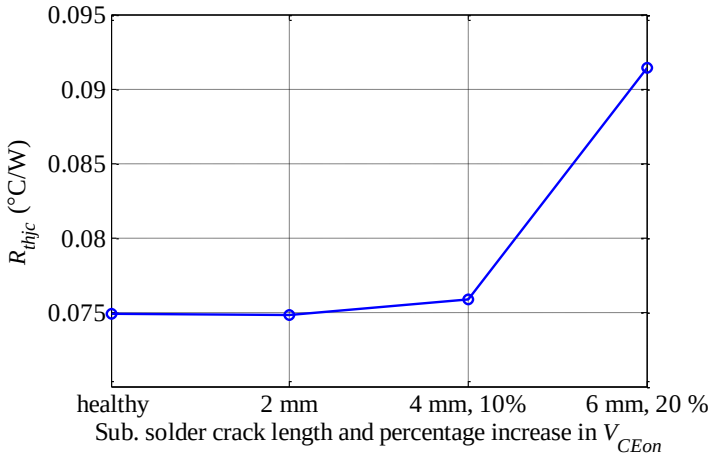


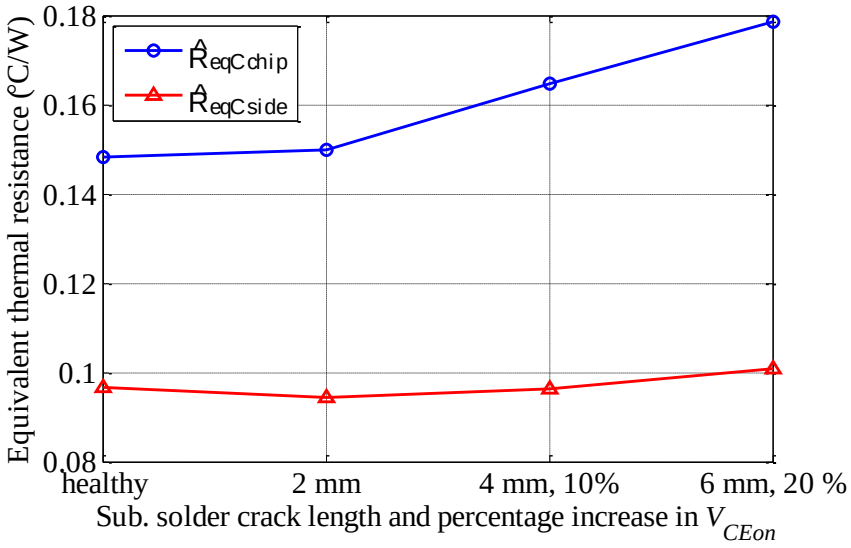
(c)

Fig. 6.5: Evolution of parameters during the mixed mode aging process of the IGBT module: (a) T_{cchip}, T_{cside}, and T_j; (b) $P_{loss}(T_j)$; and (c) R_{thjc}.

The value of R_{thjc} increased during the development of a substrate solder crack. The power loss increased noticeably when V_{CEon} increased 10% and 20%. The value of T_j first increased slightly due to an increase in T_{cchip} caused by the substrate solder crack in Scenario 2, then increased dramatically in Scenarios 3 and 4 due to the increases in P_{loss}, R_{thjc}, and T_{cchip}. The value of T_{cchip} increased due to the increasing nonuniformity of the case temperature distribution and the increase in P_{loss}. Note that T_{cside} decreased first due to the substrate solder crack and then increased due to the increase in P_{loss}.

The proposed method only needs additional measurements of T_{cchip} and T_{cside} to evaluate the health condition of the IGBT module. The values of $\hat{R}_{eqCchip}$ and $\hat{R}_{eqCside}$ were estimated by using (6.7) with the information of $\hat{P}_{loss}$, T_{cchip}, and T_{cside}; and the results are shown in Fig. 6.6(a). Then, k_{cs} was calculated by using (6.11); and the result is shown in Fig. 6.6(b). The dip and increase in $\hat{R}_{eqCside}$ indicated a mixed aging model. The value of k_{cs}, however, increased monotonically along with the development of the substrate solder crack and increased 16% from the healthy case when the crack became 6 mm.

Table 6.2 characterizes the relationships between k_{cs}, $R_{eqCchip}$, $R_{eqCside}$, and R_{thjc} during the aging process. The table was built based on the simulation data from a single substrate solder aging (crack) process when a 200-A DC current was applied to a switch of the IGBT module (i.e., I_c = 200 A). From Table 6.2, the value of R_{thjc} can be found based on the value of k_{cs}, which matches the evolution of R_{thjc} in Fig. 6.5.



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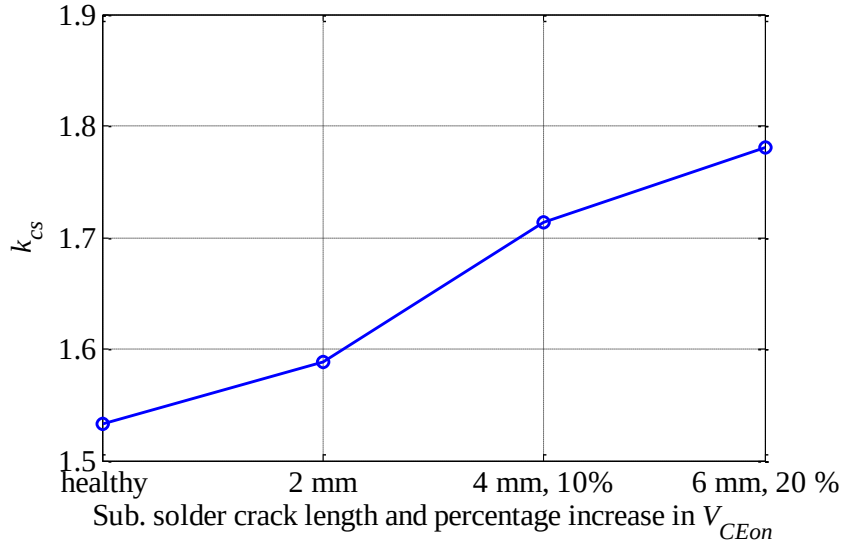


(b)

Fig. 6.6: Evolution of the estimated parameters during the mixed mode aging process of the IGBT module: (a) $\hat{R}_{eqCchip}$ and $\hat{R}_{eqCside}$; (b) k_{cs}.

Table 6.2: Lookup table for k_{cs} and thermal resistances for solder aging monitoring.

k_{cs}	1.53	1.59	1.71	1.78
$R_{eqCchip}$ (°C/W)	0.148	0.150	0.154	0.157
$R_{eqCside}$ (°C/W)	0.097	0.094	0.090	0.088
R_{thjc} (°C/W)	0.0749	0.0749	0.0759	0.0920

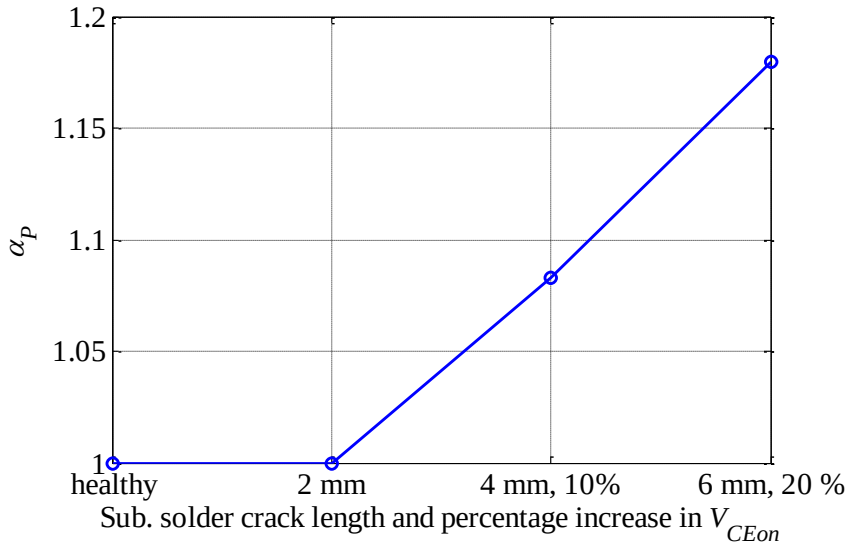
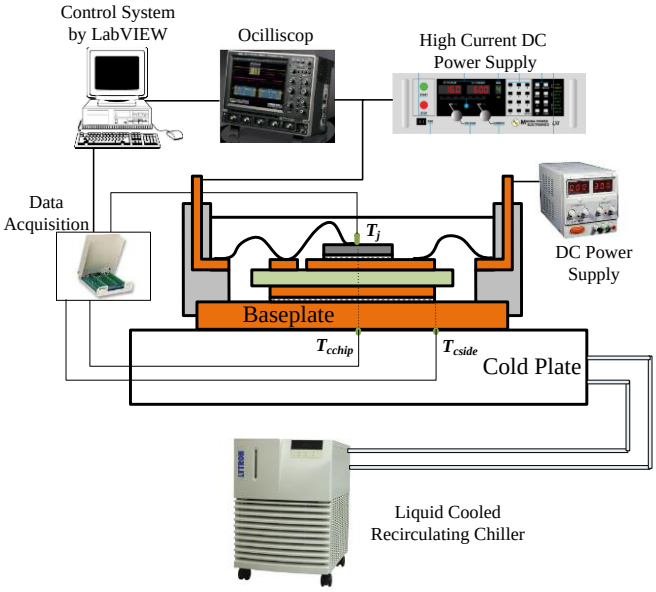


Fig. 6.7: Calculated α_P during the aging process of the IGBT module.

By using $R_{eqCchip}$ and $R_{eqCside}$ and applying (6.7), the value of α_P was calculated, as shown in Fig. 6.7. The junction temperature T_j could be updated during the aging process by (6.8) using R_{thjc} and $\alpha_P \cdot \hat{P}_{loss}(\hat{T}_j)$, where $\hat{T}_j$ = 75.2 °C was the initial junction temperature when the IGBT module was healthy. In Scenarios 3 and 4, the updated values of T_j were 81.4 °C and 91.5 °C, respectively; the values of $\hat{P}_{loss}(T_j)$ were 230.46 W (the conduction loss was 159.73 W) and 236.49 W (the conduction loss was 162.89 W), respectively. By using (6.9) and (6.10), the percentage increases in V_{CEon} due to bond wire and emitter metallization aging were correctly detected. Since k_{cs}, $R_{eqCchip}$, $R_{eqCside}$, and R_{thjc} are independent of the operating condition because of the linear thermal behavior of the IGBT module, The lookup table (e.g., Table 6.2) obtained at a specific operating condition can be used for condition monitoring of the IGBT module for various operating conditions. This feature is validated by experimental results in the next section.

6.5 Experimental Validation

Experimental studies were conducted to further validate the proposed method. Fig. 6.8 illustrates the experimental setup, which consisted of an oscilloscope for steady and



(a)

(b)

Fig. 6.8: Experimental setup for validation of the proposed method: (a) the schematic and (b) the actual setup.

transient electrical signal acquisition, such as I_c and V_{CE}; a DC source for generating gate signals for the test IGBT module; a programmable high-power DC source for providing test currents; a liquid recirculating chiller for providing the inlet coolant at 20 °C for cooling the IGBT module; a National Instruments (NI) data acquisition system (with a measurement resolution of 0.01 °C) for acquiring T_j, T_{cchip}, and T_{cside}, which were measured by using precise fine wire (0.13 mm diameter) thermocouples, Omega 5TC-TT-K-36-36, with insulation; and a control system developed in LabVIEW™ operating on a laboratory computer. The thermocouples were recommended by the manufacturer of the IGBT module to measure the case temperature for calculating the module's thermal resistance [70]. Shallow grooves were carved on the bottom surface of the baseplate and filled with thermal grease for the installation of the thermocouples.

6.5.1 Validation of the Linear Thermal Behavior of the IGBT Module

To validate the linear thermal behavior of the IGBT module, which is the foundation of the proposed method, a set of tests were performed by applying different DC currents to the IGBT module. In each test, a DC current with an amplitude between 80 A and 150 A was applied to the IGBT module to heat it until a steady state was reached. Different current amplitudes were used to emulate variations in the power loss

Table 6.3: The measured temperatures at different operation conditions.

I_c (A)	V_{CE} (V)	T_{Cchip} (°C)	T_{Cside} (°C)	T_{cool} (°C)
80	1.16	53.3	50.5	20
100	1.197	63.1	59.5	20
120	1.227	73.1	68.6	20
150	1.308	90	84.2	20

and junction temperature of the IGBT. The R_{thja} was deliberately increased by mounting the module on the cold plate with a low torque to realize higher T_j variations. This facilitated examination of the linearity of the thermal behavior of the IGBT module in a wide operating temperature range. The values of T_{cchip}, T_{cside}, and coolant (ambient) temperature T_a at different currents were recorded in Table 6.3. Then, $R_{eqCchip}$, $R_{eqCside}$, and k_{cs} were calculated using these data. Although the power loss and junction temperature varied significantly at different currents, the values of $R_{eqCchip}$, $R_{eqCside}$, and k were almost constant, as shown in Fig. 6.9. The maximum variations of $R_{eqCchip}$, $R_{eqCside}$, and k_{cs} at different currents and junction temperatures were only 1.1%, 0.9%, and 0.2%, respectively. Such small variations can be neglected. These results validated the linearity of the thermal behavior of the IGBT module over a wide range of junction temperatures. The value of k_{cs} was almost constant at different power loss conditions if the health condition of the solder was unchanged.

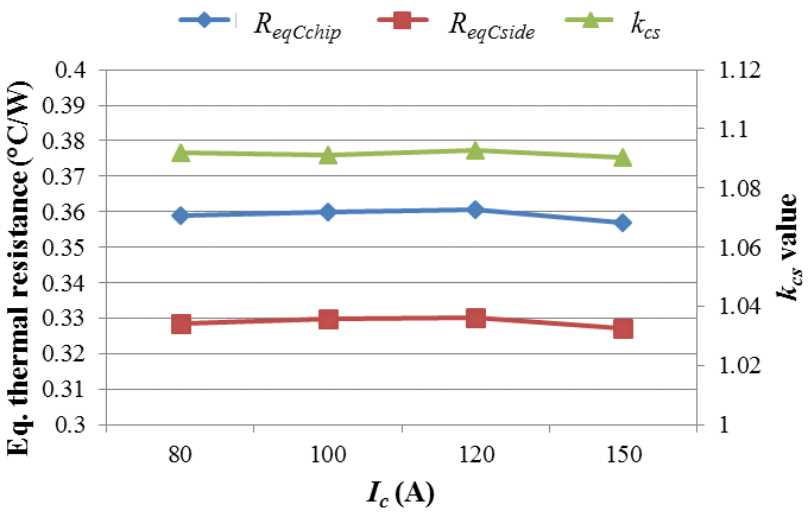


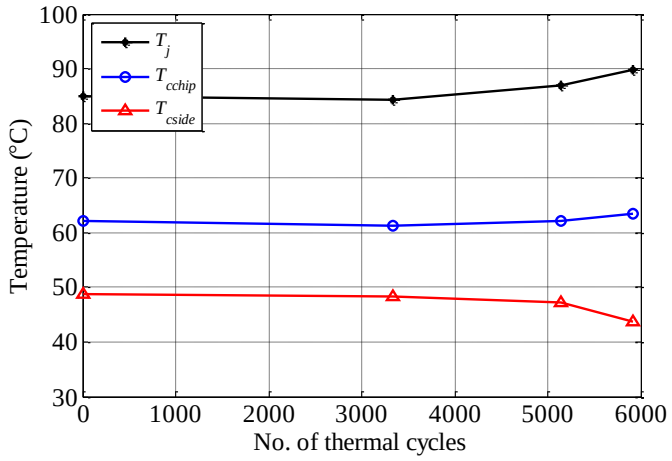
Fig. 6.9: The values of $R_{eqCchip}$, $R_{eqCside}$ and k_{cs} at different operating conditions.

6.5.2 Solder Aging Monitoring

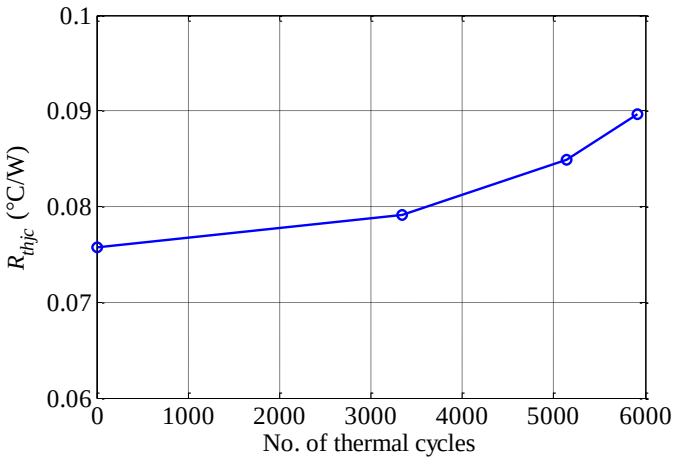
After the linear thermal behavior of the IGBT module in a specific health condition was validated, the values of k_{cs} and α_P were estimated using the proposed method to monitor the solder aging and mixed mode aging of solder and bond wires.

First, a thermal cycling test was designed to accelerate the aging process of the substrate solder, where the thermal cycles were excited by the power loss in the IGBT module. To maximize the temperature variation in the substrate solder layer while keeping T_j below 125 °C, the allowed maximum T_j specified by the manufacturer, the IGBT module was air cooled and powered by a relatively small current of 80 A. In this case, R_{thca} was much larger than R_{thjc}, making the case temperature close to the junction temperature. In each thermal cycle, the 80 A current was applied to the IGBT module for 3 minutes to gradually heat it up. Then, the module was cooled down in the next 15 minutes. The maximum T_j per thermal cycle was 105 °C. The variation of T_{cside} in one thermal cycle was about 70 °C, which was only 10 °C less than that of T_j.

The thermal cycling test was interrupted after certain cycles to inspect the changes in T_{cchip}, T_{cside}, T_j, and R_{thjc}. The value of k_{cs} was calculated using the measured case temperatures. During the inspection test, the IGBT module was remounted on the cold plate with the mounting torque recommended by the datasheet and was powered by a 200 A DC current. No change in V_{CEon} was observed. The test results are shown in Fig. 6.10 and are consistent with the simulation results. After 3,300 thermal cycles, R_{thjc} only increased by 4.5%; and T_{cchip}, T_{cside}, and T_j decreased slightly due to a 0.7 °C decrease in the coolant temperature. After that, the difference between T_{cchip} and T_{cside}, (T_{cchip}-−T_{cside}), increased from 13 °C at about 3,300 thermal cycles to 15 °C when R_{thjc} increased 12.2%



(a)



(b)

Fig. 6.10: Evolution of parameters during thermal cycling of the IGBT module: (a) measured T_{cchip}, T_{cside}, and T_j; (b) R_{thjc}.

at about 5,100 thermal cycles, and finally increased to 19.8 °C when R_{thjc} increased 18.6% at the end of the test. The nonuniformity of the case temperature distribution grew significantly during the aging process of the substrate solder.

The value of k_{cs} was estimated during the thermal cycling test, as shown in Fig. 6.11. The trend of change of k_{cs} obtained from the experiment was similar to that in the simulation. Compared to the first thermal cycle, the value of k_{cs} only increased 0.2% at

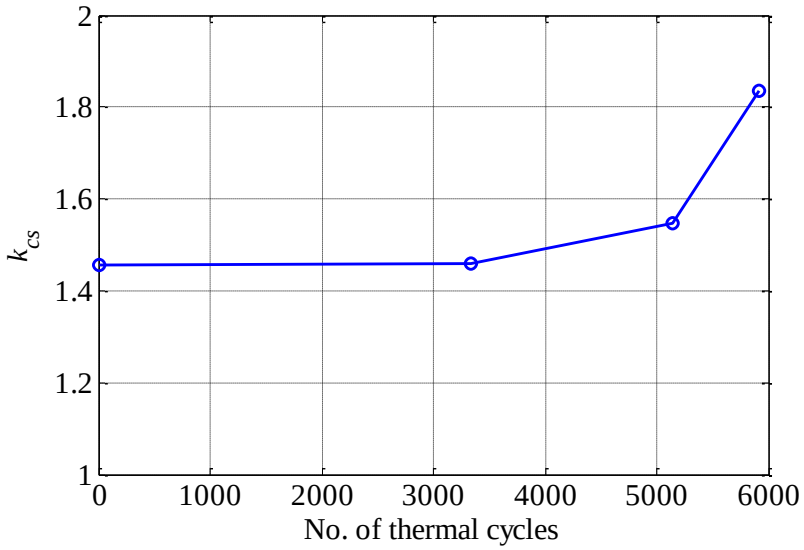


Fig. 6.11: Evolution of *k* during the thermal cycling test of the IGBT module.

the 3,300 thermal cycle, indicating that the IGBT module was healthy. However, the value of k_{cs} increased 6.3% at the 5,100 thermal cycle and 25% at the end of the test, which indicates that the IGBT module was in a medium aging and a severe aging condition, respectively. The latter also indicates that maintenance is needed for the power converter. The experimental results proved that the substrate solder aging of the IGBT module can be effectively monitored by the proposed method using T_{cchip} and T_{cside}.

6.5.3 Mixed Mode Monitoring of Aging

After the thermal cycling test, a power cycling test was performed to accelerate the aging process of the bond wires of the same IGBT module mounted onto the cold plate. In each power cycle, a 400 A current was applied to the IGBT module for 5 seconds, followed by 15 seconds to cool down the module. The variation of T_j in a power cycle was about 100 °C. The value of V_{CEon} at the same junction temperature of 90 °C was acquired in each power cycle. The evolution of V_{CEon} at 400 A during the

power cycling test is shown in Fig. 6.12. The value of V_{CEon} increased 10% at the end of the power cycling test. No increase in R_{thjc} was observed. The power cycling test was interrupted after certain cycles to inspect the changes in α_P and k_{cs} by applying 100 A and 200 A DC currents to the IGBT module. The values of α_P and k_{cs} were calculated during the steady state after the DC currents were applied for the mixed mode aging. As shown in Fig. 6.13, The value of α_P increased from 1 at the beginning of the power cycling test to 1.12 at 200 A and to 1.09 at 100 A at the end of the power cycling test. The value of α_P calculated at 200 A was larger than that at 100 A due to the temperature effect on the power loss generation. The values of k_{cs} were around 1.82 at different currents and different bond wire health conditions. The small variation in k_{cs} was caused by coolant temperature variations and thermocouple measurement errors.

The experimental results proved that: 1) it is effective to use k_{cs} for monitoring the aging of substrate solder, and k_{cs} is independent of the health condition of the bond

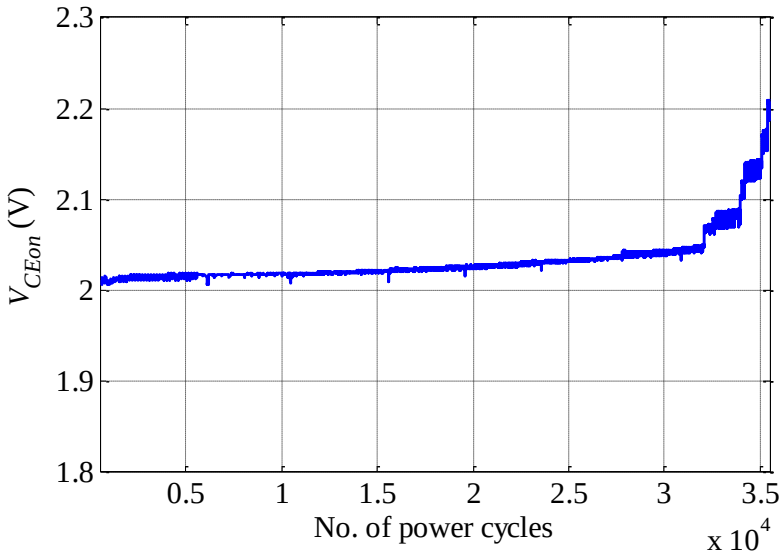
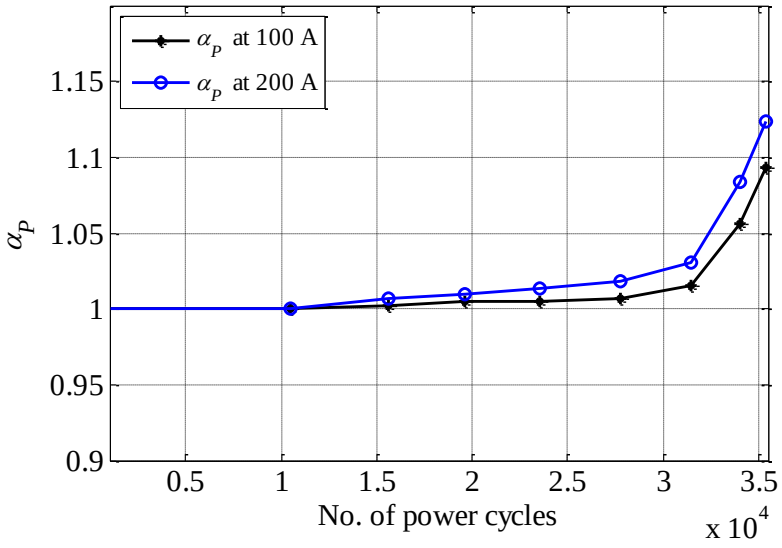
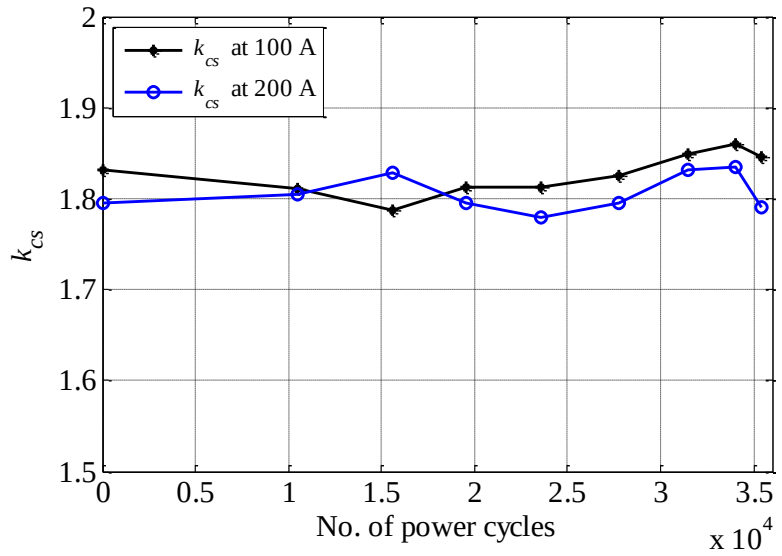


Fig. 6.12: Evolution of V_{CEon} during the power cycling test of the IGBT module.

wires; and 2) α_P is sensitive to changes in V_{CEon} and, therefore, is an effective precursor for monitoring the aging of bond wires and emitter metallization.



(a)



(b)

Fig. 6.13: Evolution of parameters during the power cycling test of the IGBT module: (a) α_P and (b) k_{cs}.

6.6 Summary

This dissertation has proposed a real-time method for monitoring the aging of IGBT modules using 2D case temperatures. The proposed method is effective for monitoring major aging processes in an IGBT module, such as bond wire liftoff, metallization aging, and substrate solder aging. A simple implementation of the proposed method using two temperature sensors for each switch was validated by simulation and experimental studies on a commercial IGBT module. Results have shown that a mix of the major aging processes can be easily detected and separated by monitoring the case temperatures at two selected points. As the case temperature is relatively stable and easy to monitor, the proposed method can be easily implemented for monitoring the aging of IGBT modules in power converters. It is recommended that the calculation of k_{cs} and α_P using the proposed method be performed when the case temperature reaches a steady state. However, when the power converter experiences a transient load, the proposed method can also be performed by averaging the case temperature measurements over a relatively long period to filter out the variations caused by the load transient.

Table 6.4 compares the proposed method with three other methods in the literature. It reveals that the proposed method achieved the best performance for all of the three metrics. For example, the proposed method is capable of monitoring all of the three major aging mechanisms and detecting which aging process or processes occur. These cannot be achieved by any of the three other methods. Moreover, compared to the first two methods in the table, the implementation of the proposed method has lower hardware complexity and does not affect power converter operation.

Table 6.4: Comparison of aging monitoring methods for IGBT modules.

Methods	Aging Mechanisms That Can Be Detected	Hardware Complexity	Affect Converter Operation
Using V_{CEon}	Bond wire, emitter metallization	High	Possible
Using TSEP	Any mechanisms causing T_j elevation	High	Yes
Using (T_c–T_a) [53]	Solder	Low	No
Proposed method	Bond wire, emitter metallization, substrate solder	Low	No

Chapter 7. Frequency-Domain Transient Temperature Estimation and Aging Analysis for Weak Points

This chapter presents a new frequency-domain thermal model for online junction temperature estimation of IGBT modules [56]. This model characterizes the thermal behavior of an IGBT module by a linear time invariant (LTI) system. The frequency response at junction is obtained by applying the fast Fourier transform (FFT) to the time derivative of the transient thermal impedance from junction to a reference position of the IGBT module. The junction temperature of the IGBT is then estimated using the frequency responses at junction and the frequency spectra of heat sources of the IGBT module. This model can be extended to estimate temperature responses at different weak points and analyze the aging modes of the IGBT module under complex working conditions [25]. By examining the frequency spectra of the power losses of an IGBT at an operating condition and the frequency responses of the temperatures at weak points, the information on bottleneck weak point(s) can be obtain. Simulation results show: 1) the proposed method is accurate and computationally efficient for estimating junction temperature and temperatures at the weak points of IGBT modules in both steady-state and transient loading conditions; and 2) the proposed method can reveal that the power losses at different loading conditions with different frequency spectra stress the weak points differently.

7.1 Heat Equation for IGBT Modules

The IGBTs with the "standard" power module packaging [17] are considered herein. During the operation of an IGBT module, the heat is generated at the chips and spreads through multiple layers to the bottom of the baseplate, which is cooled by a heat sink or cold plate. The heat conduction in the heat diffusion layers is governed by Fourier's law. By assuming that the materials are isotropic and neglecting the temperature effects of the materials' thermal properties, a differential form of heat equation governing the heat diffusion in a certain layer in the rectangular coordinate system is given by

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = \frac{1}{\alpha}\frac{\partial T}{\partial t} \tag{7.1}$$

where T is the temperature and α is the thermal diffusivity of the material of the layer. The thermal dynamics of the overall IGBT module can be modeled by equations similar to (7.1) for all of the layers constrained by the boundary conditions between different layers.

The exact solution to (7.1) can be very complex if the module geometry and boundary conditions are taken into account.

7.2 Frequency Domain Junction Temperature Estimation

Since (1) is linear, the dynamical thermal behavior of an IGBT module can be characterized by an LTI system by neglecting the cooling system performance variations. In this section, the relationship between an IGBT's power loss, $P_{loss}(t)$, and the temperature rise from junction to case, $\Delta T_{jc}(t)$, is characterized by a high-order LTI

system, $h_{pj}(t)$, which represents the time-domain impulse response of $\Delta T_{jc}(t)$ excited by the heat source $P_{loss}(t)$. The junction temperature, $T_j(t)$, is then given by

$$T_j(t) = \Delta T_{jc}(t) + T_c(t) = P_{loss}(t) * h_{pj}(t) + T_c(t) \tag{7.2}$$

In this section, $T_j(t)$ is estimated in the frequency domain using the Fourier transform technique to avoid determination of the explicit expression for $h_{pj}(t)$ and calculation for the convolution between $p_{loss}(t)$ and $h_{pj}(t)$, as follows:

$$T_j(t) = P_{loss}(t) * h_{pj}(t) + T_c(t) = \mathcal{F}^{-1}\left(P_{loss}\left(e^{jw}\right) \cdot H_{pj}\left(e^{jw}\right)\right) + T_c(t) \tag{7.3}$$

where $P_{loss}(e^{j\omega})$ is the frequency spectrum of $P_{loss}(t)$ obtained by using the Fourier transform, $H_{pj}(e^{j\omega})$ is the frequency response of $h_{pj}(t)$ obtained by using the Fourier transform, and $\mathcal{F}^{-1}$ is the inverse Fourier transform. The $h_{pj}(t)$ can be determined by taking the time derivative of the transient thermal impedance $Z_{thjc}(t)$ from the junction to the case, i.e.,

$$h_{pj}(t) = dZ_{thjc}(t)/dt \tag{7.4}$$

The values of $Z_{thjc}(t)$ can easily be obtained from FEA simulations or experiments.

For a compact IGBT module consisting of multiple heat sources, the superposition principle can be applied to characterize the thermal behavior of the whole IGBT module to obtain the junction temperatures at multiple chips of interest. The matrix form of the proposed method for obtaining the junction temperatures of N chips of interest for an IGBT module with M heat sources is given by

$$\begin{bmatrix} T_{j1} \\ T_{j2} \\ \vdots \\ T_{jN} \end{bmatrix} = \mathcal{F}^{-1}\left(\begin{bmatrix} H_{11} & H_{12} & \cdots & H_{1M} \\ H_{21} & H_{22} & & H_{2M} \\ \vdots & & \ddots & \vdots \\ H_{N1} & H_{N1} & \cdots & H_{NM} \end{bmatrix}\begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_M \end{bmatrix}\right) + T_c \cdot \mathbf{1}_{1\times N} \tag{7.5}$$

where H_{nm} (n = 1, ⋯, N and m = 1, ⋯, M) is the frequency response of the temperature rise from the nth junction to the case excited by the mth source P_m, and $\mathbf{1}_{1\times N}$ is a N-dimensional column vector with all elements being one. The value of H_{nm} can be determined by the Fourier transform of the time derivative of $Z_{nm}(t)$, which is the equivalent transient thermal impedance from the nth junction to case when only the mth source is powered. The value of $Z_{nm}(t)$ can be obtained from FEA simulations or experiments.

In digital system applications, the discrete time form of (7.3) is given by

$$T_j[k] = P_{loss}[k] * h_{pj}[k] \cdot T_s + T_c[k] = \mathcal{F}^{-1}\left(P_{loss}(\Omega) \cdot H_{pj}(\Omega)\right) \cdot T_s + T_c[k] \quad (7.6)$$

where k is the index of the discrete time sequence, T_s is the sampling period, $P_{loss}(\Omega)$ is the discrete Fourier transform (DFT) of $P_{loss}[k]$, $H_{pj}(\Omega)$ is the frequency response of $h_{pj}[k]$, and $h_{pj}[k]$ can be calculated by

$$h_{pj}[k] = (Z_{jc}[k+1] - Z_{jc}[k])/T_s \quad (7.7)$$

The DFT can be efficiently computed using the FFT. The flowchart of the proposed method is illustrated in Fig. 7.1.

The proposed method has the following advantages.

1) Highly Accurate: The accuracy of the proposed method relies on the accuracy of $h_{pj}(t)$ of the IGBT module, which can be accurately estimated offline. Therefore, the proposed method is capable of approximating the accurate numerical thermal model obtained from FEA simulations or the experiment measurements online with good precision.

2) Computationally Efficient: The computational cost of the proposed method depends on the sampling frequency of the quantities in (7.5). According to the Nyquist-Shannon sampling theorem, f_{sw} of the power losses in (7.5) should be more than twice the highest harmonics of the power losses. According to the power loss calculation equations in [77], the highest harmonics of the power losses in an inverter are just several times higher than the line frequency, if the power losses are averaged over each switching period. Thus, the proposed method does not require a high sampling frequency. The proposed method has a computational complexity of $O(K_{sp}\times\log_2 N_l)$, where K_{sp} is the number of the time-domain data samples of the power losses; and N_l is the order of the LTI system. The value of N_l is the product of the sampling frequency in Hz, e.g., 1,000

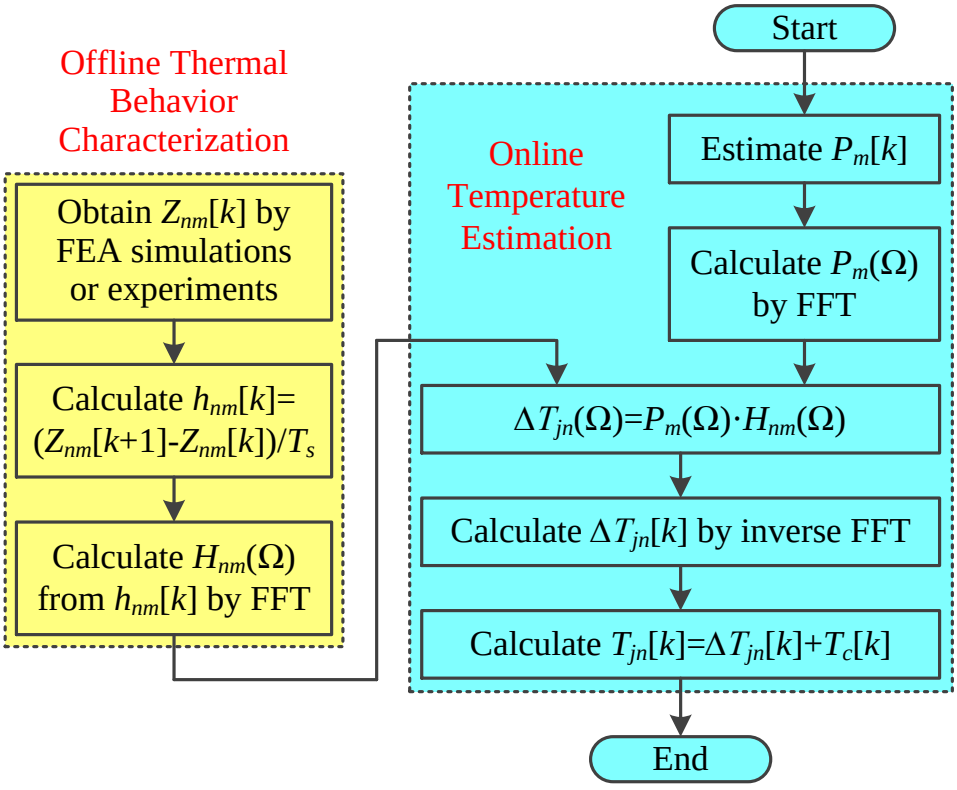


Fig. 7.1: The flowchart of the proposed method.

Hz, and the settling time in second to the steady state (typically 5-10 s) of the transient response of the time domain thermal impedance. The computational complexity of the proposed method is on the same order as that of a TEC model O(K_{sp}×N_{rc}), where N_{rc} is the order of the TEC. Therefore, the proposed method is computationally efficient for online junction temperature estimation.

3) Easy to Build: The derivation of a high-fidelity, analytical thermal model from physical principles or the extraction of a high-fidelity, low-order numerical thermal model from a high-order numerical thermal model of an IGBT module usually involves significant mathematical complexity and difficulty, especially when the target IGBT module has high geometric complexity and multichip thermal cross-coupling. The proposed method does not have any problem with mathematical complexity or difficulty.

7.3 Frequency Domain Aging Model Analysis

7.3.1 Thermomechanical Stresses

As stated in Chapter 1, the major aging mechanisms observed in power devices are mainly due to thermomechanical stresses experienced by the packaging materials, which are caused by the mismatch of the CTEs between different materials. The CTEs of copper and aluminum are much larger than those of silicon and ceramic. Therefore, during temperature swings, thermomechanical stresses are generated between the interfaces of different layers made of different materials, which results in the aging of weak points. The aging of bond wires is a result of either the shear stress generated between the bond pad and the wire or by the repeated flexure of the wires [10] during temperature swings. The aging of a solder layer in an IGBT module is mainly due to the

large mismatch of the CTEs of the two adjacent layers and temperature swings combined with the dimensions of the layers. The strain, $\varepsilon_{mismatch}$, at the interface between two different materials caused by the thermal mismatch of their CTEs is calculated by

$$\varepsilon_{mismatch} \approx \Delta\alpha_{CTE} \cdot \Delta T_{\varepsilon} \tag{7.7}$$

where $\Delta\alpha_{CTE}$ is the difference between the CTEs of the two materials, and ΔT_{ε} is the temperature change from the temperature where the strain is zero [8]. By substituting (7.7) into the Coffin-Manson equation for the low-cycle fatigue (dominated by the plastic strain) and the Basquin's equation for the high-cycle fatigue (dominated by the elastic strain) [9], the lifetime of the interface between the two materials under cyclic thermomechanical stresses has an inverse exponential relationship with ΔT as follows:

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon_f'(2N_f)^{c_f} \rightarrow N_f \propto (\Delta\varepsilon_p)^{-c_f} \propto (\Delta T)^{-c_f} \tag{7.8}$$

$$\sigma_a = E\frac{\Delta\varepsilon_e}{2} = \sigma_f'(2N_f)^{b_f} \rightarrow N_f \propto (\Delta\varepsilon_p)^{-b_f} \propto (\Delta T)^{-b_f} \tag{7.9}$$

where ε_p is the plastic strain, ε'_f is the fatigue ductility coefficient, c_f is the fatigue ductility exponent, ε_e is the elastic strain, σ_a is the alternating stress, E is Young's modulus, σ'_f is the fatigue strength coefficient, and b_f is the fatigue strength exponent. It should be noted that ΔT is the local temperature swings at the weak points. According to (7.8) and (7.9), the bond wire and large area solder lifetimes are related to the local temperature swings.

7.3.2 Aging Mode Analysis

The existing device aging analysis usually only uses the junction temperature information and a lifetime mode, such as (1.4). However, the junction temperature is much more sensitive to a transient power loss than the temperatures at other weak points.

IGBT modules with similar junction temperature records might have quite different lifetimes. For example, a 10 ºC swing in the junction temperature can be caused by a gradual or sudden change in power loss. However, for the temperature at the free edge of the substrate solder, a negligible swing is observed when a very short pulse power loss is applied to the IGBT. These facts indicate that an IGBT module might experience quite different stresses in different loading conditions when the records of ΔT_j are very close. In other words, to achieve an accurate lifetime prediction, the power loss profiles at the loading conditions and the corresponding bottleneck weak point(s) should be analyzed appropriately. Thus, a study on the temperature swings at the weak points when an arbitrary loading condition is applied to the power device is highly desirable.

Several points in an IGBT module are used to study temperature swings at weak points, including the middle of junction (P_{jm}), the free edge of the chip solder layer (P_{ce}), and the free edge of the substrate solder (P_{se}), as illustrated in Fig. 7.2. The points are chosen due to the fact that bonds usually fail from the center to the edge of the chip [79] and a crack usually starts at the free edge of a large-area solder layer in electronic

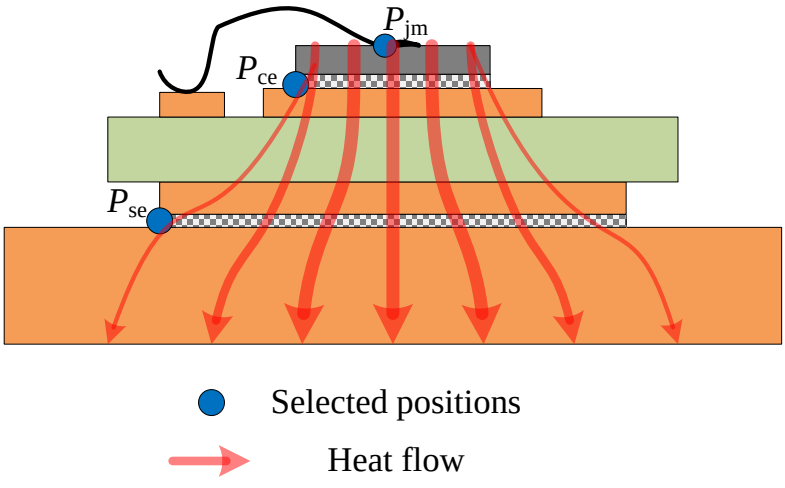


Fig. 7.2: Selected points and heat flows inside an IGBT module.

packages [72]. During the operation of an IGBT, the heat can be assumed to be generated at the top surface of a chip and to spread down through different layers to the bottom of the baseplate, which is cooled by a heat sink or a cold plate. The temperature changes at the selected points are complex due to the high complexity of the module geometry and the effects of heat storage and spreading in layers. For example, P_{jm} is the location where most heat is generated. Therefore, the temperature at P_{jm} is sensitive to the changes in power loss, while the temperature at P_{se} performs a "low-pass filtered" thermal response due to its distance to the heat source and the heat storage effect in the DBC.

The method used to thoroughly study temperature swings at weak points of an IGBT module in general operating conditions is fairly straightforward—the frequency spectra of the local thermal responses are analyzed. In this section, the thermal analysis method proposed in Section 7.2 is extended to estimate the transient temperature at the weak points. The proposed method is highly accurate and can be used for any loading conditions.

The proposed method can reveal that the power losses at the loading conditions with different frequency spectra stress the weak points differently. As stated early in this section, due to the difference in geometry, the temperature at P_{se} has a different frequency response from that at P_{jm}. The IGBT module can undergo a power cycling which stresses bond wires and chip solder or a power cycling mixed with a thermal cycling which stresses all of the weak points. An example of the temperatures at P_{jm} and P_{se} under two different loading conditions is illustrated in Fig. 7.3. Since the power loss is nonnegative, the DC components of the power losses are large. Loading 1, which has rich high-frequency components, may not severely stress the substrate solder. However, the

reliability of bond wires might deserve more consideration. For Loading 2, the lifetime prediction for the IGBT module should consider the aging of both weak points.

It is difficult to define an arbitrary working cycle in the time domain [80]. However, by examining the frequency spectrum of the power loss at a loading condition, the information on the aging mode(s) of the IGBT can be obtained. Moreover, the analysis in the frequency domain can help classify the loads in terms of the aging modes of an IGBT. Note that a quantitative lifetime cannot be directly calculated from the power loss spectrum. This is because the Fourier transform of the power loss at a loading condition is a linear decomposition of temperature excitations, and the lifetime models are exponentially dependent on the temperatures at the weak points. However, the proposed method can help determine the bottleneck weak point(s) of an IGBT module under complex operating conditions by analyzing the frequency spectra of the power

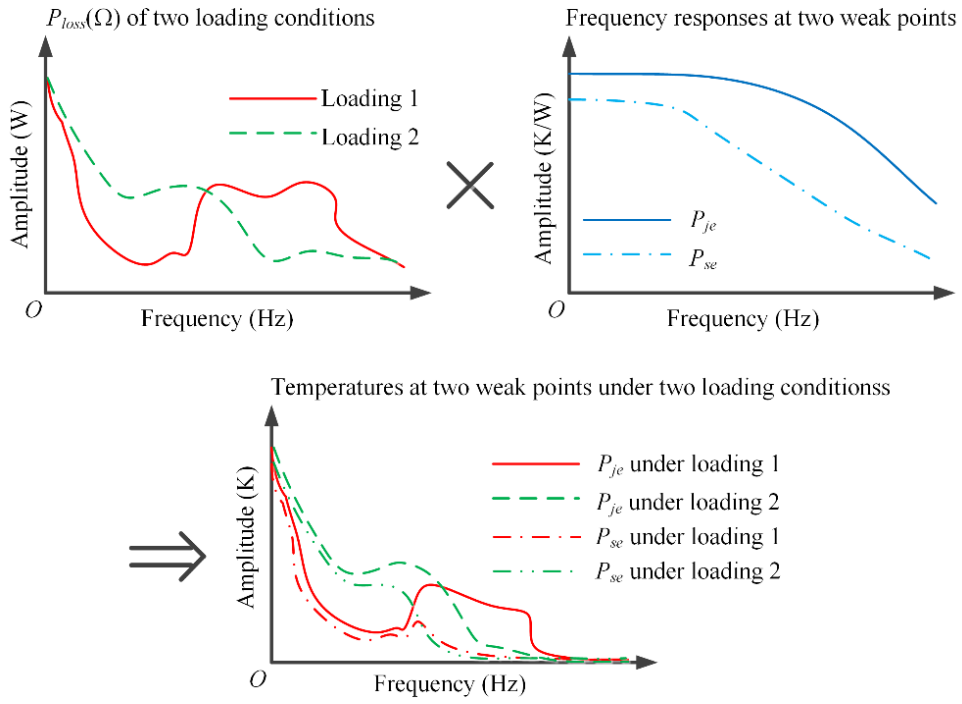


Fig. 7.3: Temperature information of P_{jm} and P_{se} under two different loading conditions.

losses at the loading conditions.

7.4 Simulation Study

In this chapter, the simulation study consists of three parts: 1) validate the accuracy of the frequency domain transient junction temperature estimation method; 2) examine the differences between temperature responses at different weak points; and 3) preliminarily verify the frequency domain aging mode analysis method by comparing time domain lifetime predictions of the weak points.

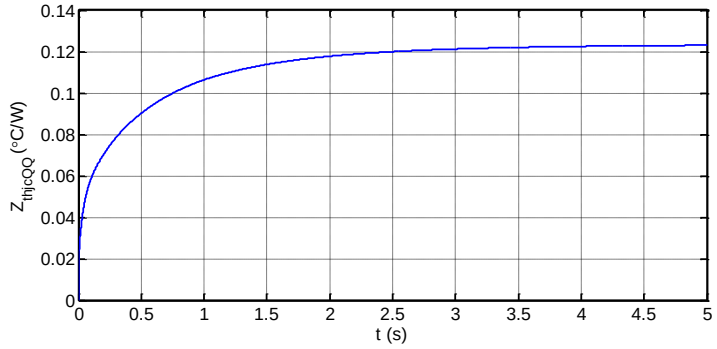
7.4.1 Frequency Domain Junction Temperature Estimation

Simulation studies were performed to validate the proposed frequency domain junction temperature estimation method against an FEA thermal model built in Autodesk Simulation Multiphysics, i.e., the reference model, and the 4^{th} order TEC model provided by the manufacturer [81] for junction temperature estimation of the commercial IGBT module, CM400DY-12NF. Note that the FEA used in this study is different from the FEA thermal model in Chapter 3. In the FEA thermal model used in this study, a fine mesh was used for the chips, solder interfaces, and DBC stack; while a relatively coarse mesh with 7551 3D elements was used for the baseplate. The total mesh of the FEA thermal model of the IGBT module has 25,955 3D elements and 39,090 nodes. It was assumed that the power losses were generated inside the chips close to their top surfaces [35]. Therefore, the calculated power losses could be converted to heat fluxes applied at the top surfaces of the chips [23]. The cooling for the IGBT module was simplified to heat convection at the bottom surface of the baseplate with a constant heat convection rate of 10,000 W/(m^2·°C). The ambient temperature was 65 °C. The IGBT module was

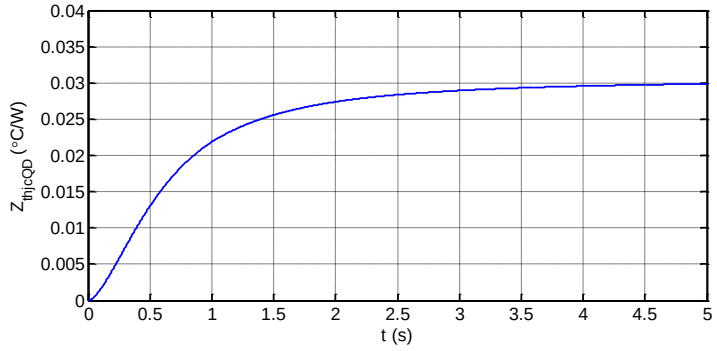
operated as a leg in a two-level three-phase inverter. The case temperature was measured at the point specified on the outline drawing and circuit diagram on the datasheet [8] for the IGBT module.

The transient thermal impedances from the junction of the IGBT chip to the case, $Z_{thjcQQ}(t)$ and $Z_{thjcQD}(t)$, which were obtained when the IGBT chip was powered alone and its parallel FWD was powered alone, respectively, are shown in Fig. 7.4. The settling times to the steady state of $Z_{thjcQQ}(t)$ and $Z_{thjcQD}(t)$ were 5 s. The $h_{QQ}(t)$ and $h_{QD}(t)$ in Fig. 7.4, which were determined by taking the time derivatives of $Z_{thjcQQ}(t)$ and $Z_{thjcQD}(t)$, respectively, were the impulse responses of the LTI systems characterizing the relationships between the IGBT junction temperature and the power losses generated by the IGBT and the FWD, respectively. The sampling frequency was 1 kHz for the proposed method. Therefore, the order of the LTI systems used in the proposed method was 5,000.

The same transient load in Chapter 4, which mimicked the starting process of an electric motor in an HEV, was applied to the inverter to evaluate the accuracy of the proposed method for online junction temperature estimation. In a TEC model, since the TECs from the junction to the case of the IGBTs and the FWDs were only interconnected at the heat sink, the thermal cross-coupling effects between chips in an IGBT module can only be partially addressed [82]. Thus, for fair comparison between different methods, the thermal couplings between IGBTs and FWDs were neglected in all of the three models. The power losses generated by the chips were calculated based on the simulated currents as well as the conduction voltage-current curve and switching loss-current curve provided by the datasheet of the IGBT module [8].



(a)



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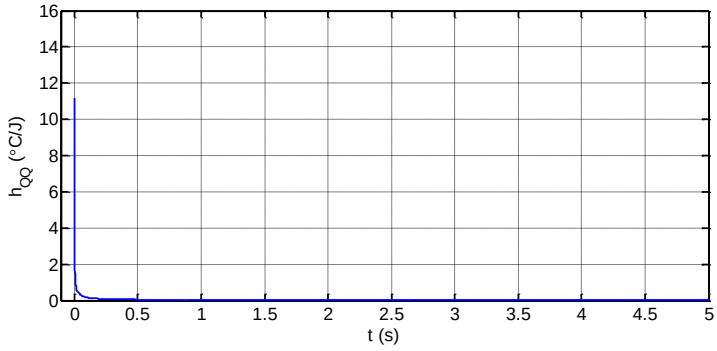

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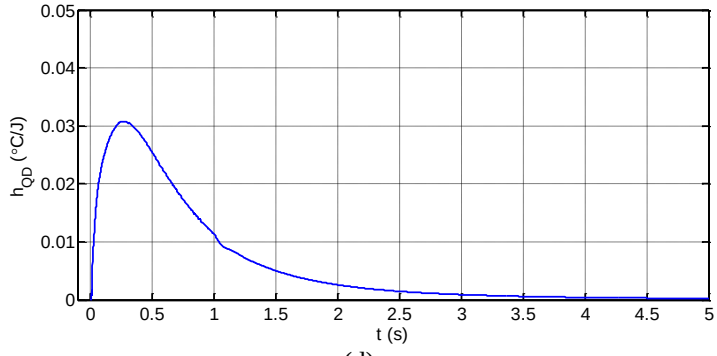
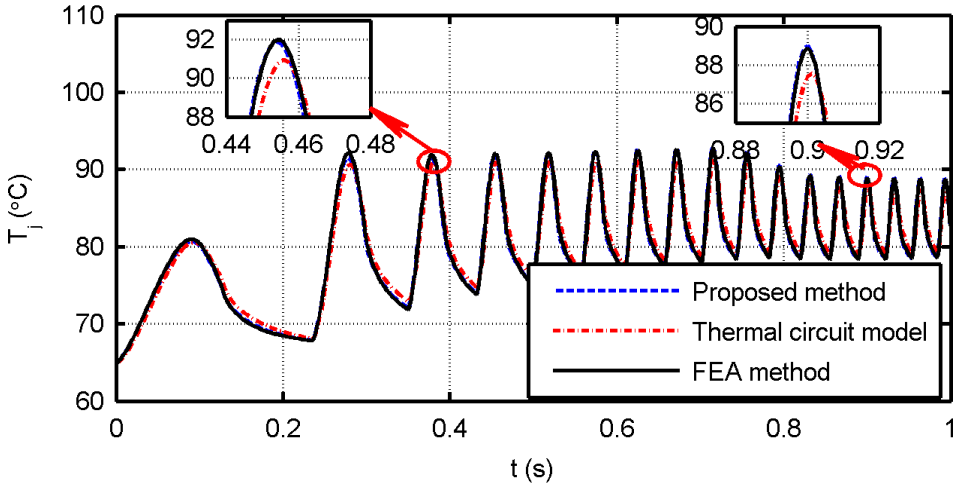


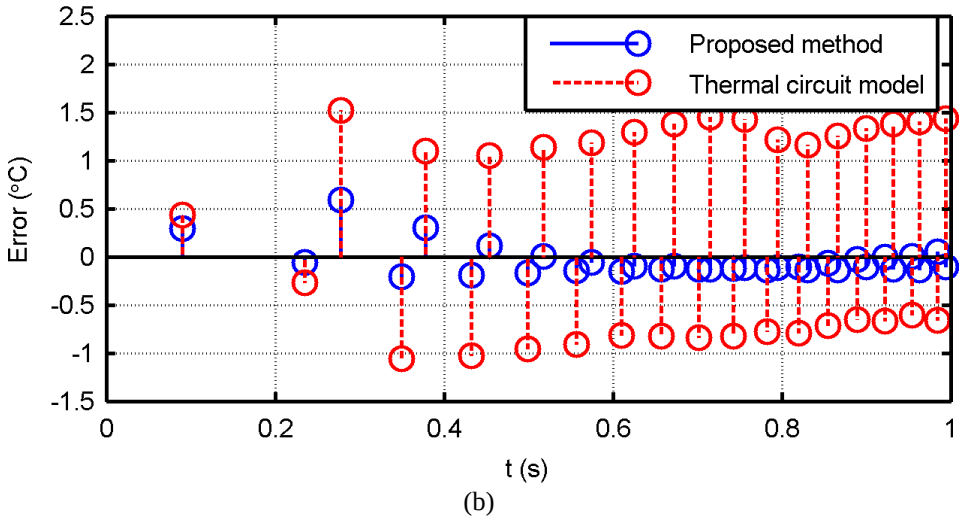
(d)

Fig. 7.4: The transient thermal impedance responses from the junction of the IGBT chip to the case and the corresponding LTI system responses: (a) $Z_{thjcQQ}(t)$; (b) $Z_{thjcQD}(t)$; (c) $H_{QQ}(t)$; and (d) $H_{QD}(t)$.

Fig. 7.5(a) compares the values of the junction temperature, $T_j(t)$, estimated by the proposed model, the TEC, and the FEA method. The value of $T_j(t)$ fluctuates in the range of 10 ~ 15 ºC. The value of $T_j(t)$ obtained from the proposed method matches that of the FEA method better than the TEC. As shown in Fig. 7.5(b), the errors of the junction temperature estimated by the proposed method with respect to the FEA method at its



(a)



(b)

Fig. 7.5: Comparison of $T_j(t)$ estimated by the three methods when the inverter was operated with a transient load: (a) junction temperature and (b) error at peaks and valleys with respect to the FEA method.

peaks and valleys are almost less than 0.2 ºC with the maximum of 0.6 ºC at 0.28 s during the transient load. On the other hand, the errors of the TEC model are between 1 ºC and 1.6 ºC at the peaks and between 0.6 ºC and 1.1 ºC at the valleys. The results showed that in general, the junction temperature estimation error of the proposed method was less than 20% of that of the TEC model. Moreover, when the line frequency of the inverter increased, the relative error of $T_j(t)$ obtained from the TEC model with respect to its amplitude of variations in one cycle increased because of more dynamic changes in the power loss. However, the increase of the inverter line frequency did not affect the proposed method, as long as the highest harmonic of the power loss was lower than half of the sampling frequency of the power loss.

The proposed method was further examined by comparing it with the FEA method at a constant operating point of the converter: 400 V DC-link voltage, 400 A output current, power factor of 0.8, unity modulation index, 5 kHz switching frequency, and 60 Hz line frequency. In this study, the thermal couplings between the chips of IGBTs and FWDs were considered in both models to further examine the capability of the proposed method for handling the thermal coupling effects. The results in Fig. 7.6 show a negligible difference between the proposed method and the FEA method because the relative error of the junction temperature estimated by the proposed method was almost always less than 1% with respect to that obtained from the FEA method.

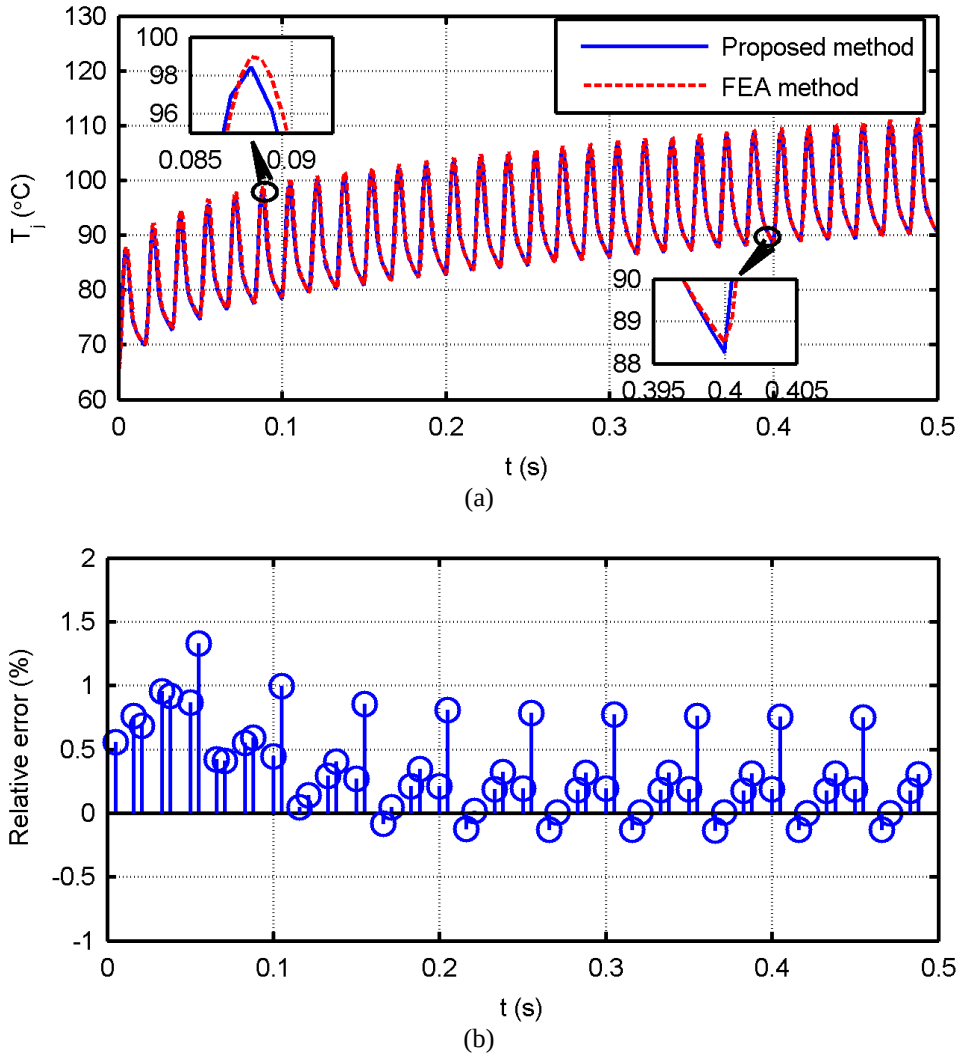


Fig. 7.6: Comparison of $T_j(t)$ estimated by the proposed method and the FEA method when the inverter was operated at a constant operating condition: (a) junction temperature and (b) relative error at peaks and valleys with respect to the FEA method.

7.4.2 Illustration of Temperature Reponses at Different Weak Points

For simplicity without loss of generality, temperature swings of a "general" single-chip symmetric IGBT module (Fig. 7.7) were studied by using the proposed frequency-domain analysis method. For multichip IGBT modules, the temperatures at the points of interest were estimated by applying superposition of the thermal responses at the points of interest to the excitations of multiple heat sources. The size of the chip was

10 × 10 × 0.25 mm. The geometry and material composition of the substrate were the same as the "standard" high power IGBT module with AlN ceramic and copper baseplate. The size of the baseplate was 18 × 18 × 4 mm. The cooling system was simplified to a heat convection surface at the bottom of the baseplate with the ambient temperate being set to 0 ºC.

As Fig. 7.8 shows, the transient thermal impedance from P_{se} to ambient, which was derived from an FEA simulation using a step-change input power, was distinctive from those from P_{jm} and P_{ce} to ambient. Moreover, the temperature at P_{se} was strongly resistant to high-frequency power losses, e.g., the temperature amplitude at P_{se} was only -20 dB for a 10 Hz power loss input. Note that all of the transient thermal impedances were normalized with respect to the steady-state thermal resistance from P_{jm} to ambient, and the frequency responses of the temperatures at the selected points were normalized by a power loss of 100 W.

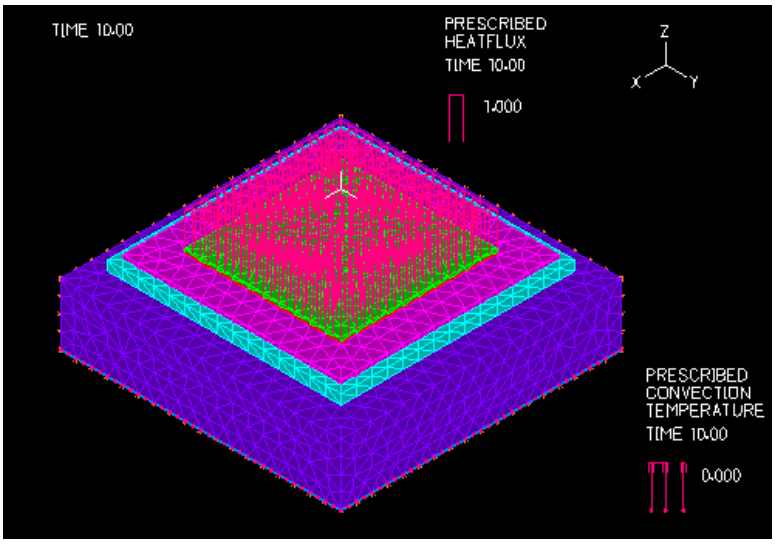
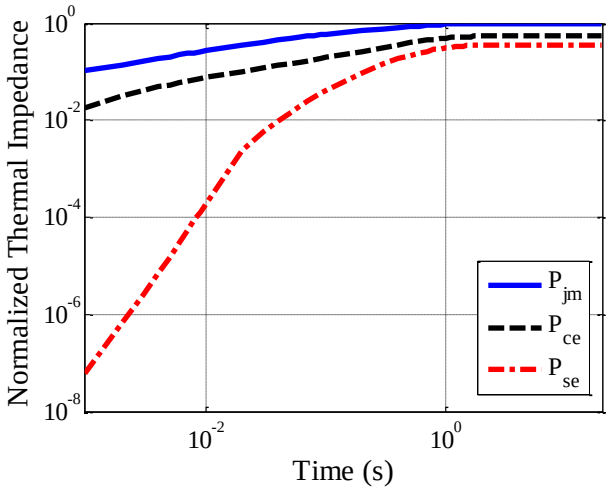
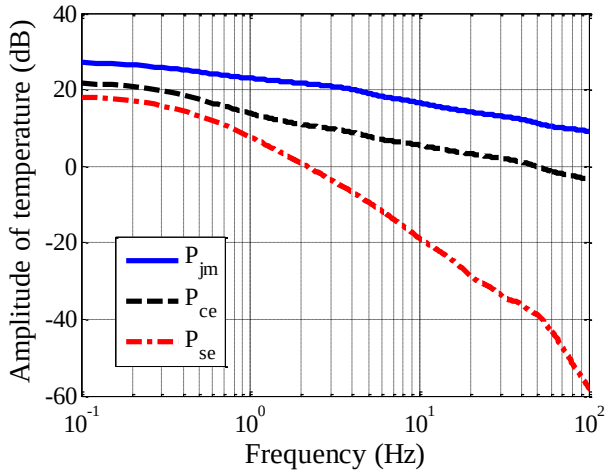


Fig. 7.7: FEA model of the general IGBT module.

The accuracy of the proposed frequency-domain analysis method was examined by comparing the estimated transient temperature at P_{jm}, which was the point most sensitive to power loss changes, with that obtained from the FEA method for an arbitrary loading condition. The estimated temperature at P_{jm} using the proposed method matched the result of the FEA method very well, as shown in Fig. 7.9. The maximum error was



(a)



(b)

Fig. 7.8: FEA simulation results for a step-change input power. (a) Normalized transient thermal impedances from the selected points to ambient and (b) frequency responses of the temperatures at P_{jm}, P_{ce}, and P_{se}.

less than 0.3 ºC. The estimated transient temperatures at P_{ce} and P_{se} are also shown in Fig. 7.9. Quite different thermal responses were observed at the three points: 1) the temperature at P_{jm} increased and fluctuated significantly, 2) the temperature at P_{ce} increased and fluctuated slightly, and 3) the temperature at P_{se} increased slowly with negligible fluctuation. The result was consistent with that the temperature at P_{se} is resistant to high frequency components of power losses. If the dominant components of the power loss at a loading condition are relatively high-frequency components, the substrate solder is much less stressed.

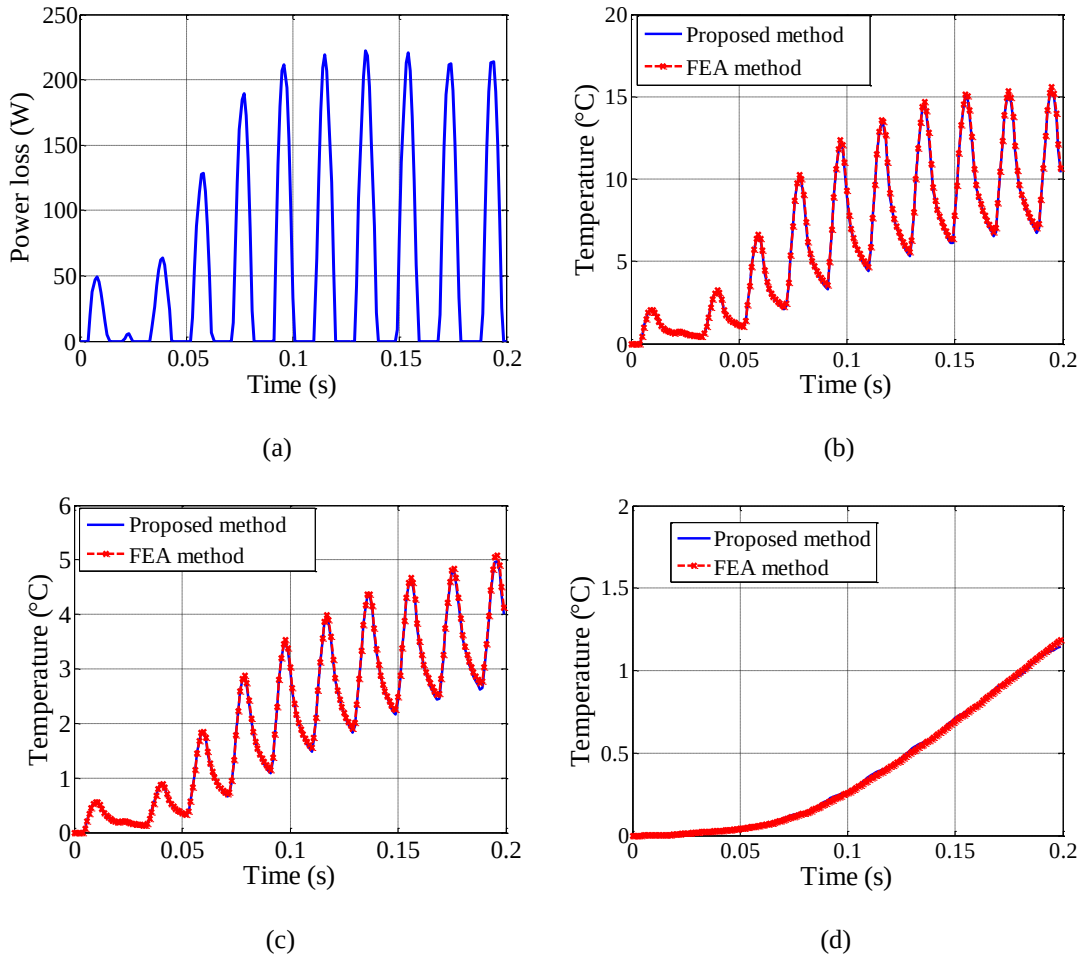


Fig. 7.9: Comparison of the proposed method with the FEA method. (a) The power loss and the transient temperatures estimated by the two methods at (b) P_{jm}, (c) P_{ce}, and (d) P_{se}.

7.4.3 Frequency Domain Aging Mode Analysis

To study the impact of different real-world loading conditions on the lifetime of IGBT modules, the "general" test IGBT module was used as a switch in the inverter of an HEV under slow acceleration [loading (a)] and fast acceleration and braking [loading (b)] conditions. As bond wires are usually observed as a bottleneck weak point [45], the focus was placed on determining if the device would undergo mixed aging modes under the loading conditions. Thus, the lifetime of the substrate solder was examined under the two loading conditions. The speed of the HEV, frequency spectrum of the generated heat in the IGBT chip, and temperature at P_{se} under the two loading conditions are shown in Fig. 7.10(a) and Fig. 7.10(b), respectively. The frequency spectrum in the range of 0.1-10 Hz was used for rough substrate solder aging analysis. The range was selected based on the frequency response of the temperature at P_{se}. The temperature at P_{se} was estimated by using the full frequency spectrum to ensure accuracy. The amplitudes of the low frequency components of the heat generated under loading (b) were approximately five times larger than those under loading (a), which indicates that the device undergoes a more stressful thermal cycling under loading (b). As a consequence, the temperature swing of P_{se} is about 14 °C under loading (b), while only around 3 °C under loading (a). The rainflow counting algorithm [83] was used to process the temperature-time data, i.e., the cyclic information of the temperatures at P_{se}. Then, by substituting the processed cyclic information of the temperatures at P_{se} under loadings (a) and (b) into the fatigue lifetime model for the substrate solder [84], the lifetimes of the substrate solder under loadings (a) and (b) were predicted to be 7,442 hours and 1,585 hours, respectively. The lifetime predictions verified that the aging of the substrate solder under loading (a) was

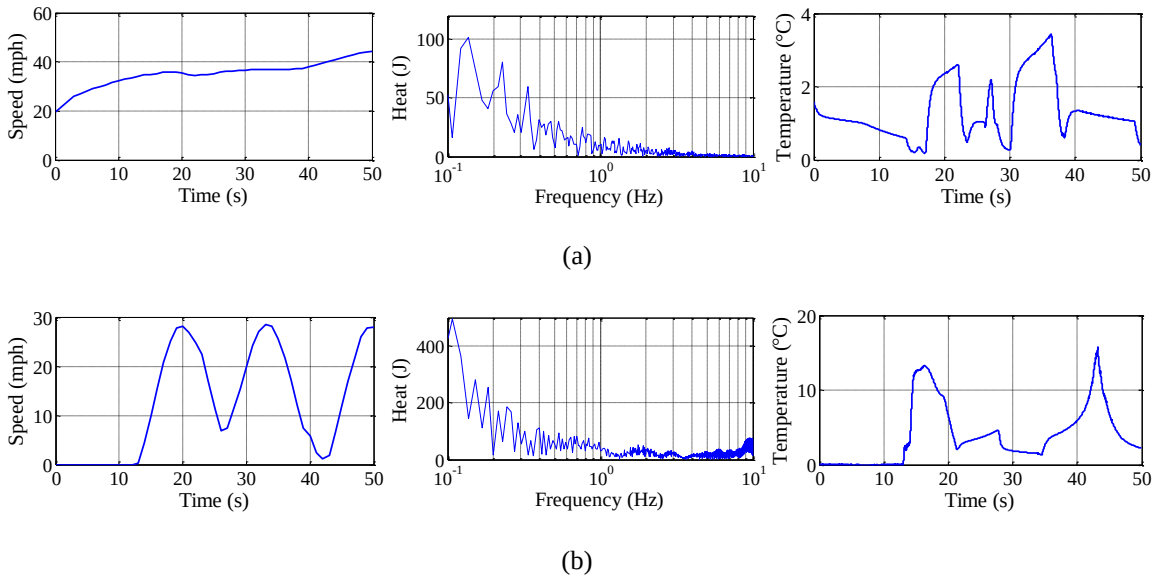


Fig. 7.10: Speeds of HEV, frequency spectra of heat generation, and temperatures of P_{se} for loading (a) and loading (b).

more severe than that under loading (b). This suggests that the substrate solder can be a bottleneck weak point of the IGBT module, and the IGBT module might undergo mixed aging modes under loading (b).

7.5 Summary

This chapter has proposed a computationally efficient, high-fidelity, easily built, online, frequency-domain junction temperature estimation method for IGBT modules. The proposed method characterized the dynamical thermal behavior of an IGBT module by an LTI system, which approximated an FEA thermal model for the IGBT. The junction temperature was then estimated from the FTT-based frequency responses of the LTI system and the heat sources of the IGBT module. The proposed method removed the need for deriving an explicit expression of the system's transfer function and could be easily built using numerical simulations or experiments. The proposed method has been

validated by simulation studies for a commercial IGBT module. Results have shown that the accuracy, particularly the accuracy during transient operating conditions, of the proposed method is comparable to the FEA method and is much higher than the commonly used TEC model. However, the computational cost of the proposed method is much lower than that of the FEA method and is comparable to the TEC model.

Further, the proposed method can be extended to estimate the temperatures at weak points in an IGBT module. Simulation results have proved that the temperatures at the weak points can also be accurately estimated. By examining the frequency spectra of the power losses of an IGBT at a loading condition and the frequency responses of the temperatures at weak points, the information on bottleneck weak points under the specific operating conditions can be obtained.

Chapter 8. Conclusions, Contributions, and Recommendations for Future Research

The goal of this dissertation research was to develop accurate real-time internal temperature estimation and health monitoring methods to provide better overtemperature protection and lifetime prediction for and avoid unexpected wear-out failures of IGBT modules used in many applications, such as automobiles and wind turbines. The thermal dynamics and major aging mechanisms of the "standard" IGBT module were considered in this dissertation research. First, three cost-effective thermal models suitable for real-time implementation were developed to accurately estimate the junction temperature of the IGBTs for better overtemperature protection and lifetime prediction. Second, a physics-of-failure-based practical technique using 2D case temperatures was invented to monitor and identify the major aging processes of the IGBT modules for effective maintenance scheduling. Third, a novel frequency-domain thermal analysis method was developed for fast and accurate estimation of temperature swings at the weak points of the IGBT modules. This method can give a quick determination of the potential bottleneck weak point(s) of the IGBT modules in a specific application, if its typical duty cycle is given and help choose an appropriate lifetime mode for the RUL prediction.

8.1 Conclusions and Contributions

Two cost-effective thermal models for healthy IGBT modules were developed and presented in Chapter 3 and Chapter 4. The physics-based improved Cauer-type TEC

in Chapter 3 introduced a new concept of lumped-capacitance approximation error, which can be used to determine the number of RC pairs for each layer of the module architecture. Further, an analytical expression of the thermal impedance of the bulky baseplate layer was derived and simplified to a first-order transfer function, which can be represented by an RC pair in a TEC. By using the proposed modeling method, the structure and parameters of a Cauer TEC can be appropriately designed to meet the high-accuracy and low-cost requirements for real-time implementation. A simulation study proved that the proposed Cauer-type TEC model greatly improves the accuracy of the conventional Cauer-type TEC model for the transient junction temperature estimation of IGBT modules with a slightly increased order only.

In Chapter 4, a thermal model based on low-order IIR digital filters was developed to characterize the thermal behaviors of IGBT modules. The coefficients of the IIR digital filters can easily be determined by using some mature digital filter parameter identification techniques, such as the Steiglitz-McBride method. The digital filters can handle dynamics in large frequency range, have stable performance, and model the thermal cross-coupling in the IGBT modules more accurately than TEC models. Simulation results showed that the accuracy of the proposed digital filter thermal model is much higher than the TEC model. One more advantage of the digital IIR filters is that they can be easily implemented in a digital processing system for real-world applications.

In Chapter 5, to properly manage the operation of power converters during the IGBT aging process, an adaptive TEC model was developed that can be used for accurate junction temperature estimation over the lifespan of IGBT modules. Based on a new method for online monitoring of solder cracks in IGBT modules, the changes in the

thermal behavior of the IGBT modules were interpreted by the changes in the EHPP, which is a new concept introduced in this research. Further, based on the EHPP, the changes in the thermal behavior of the IGBT modules were quantified online; and the parameters of the TEC model were updated online as well. Simulation studies validated the effectiveness of using the proposed EHPP and adaptive TEC model to track changes in device thermal resistance from junction to case and achieve improved junction temperature estimation during the process of substrate solder cracks.

All of the three thermal models can be used for real-time junction temperature estimation. The advantage of the improved Cauer-type TEC model is that it has physical meanings. It can incorporate temperature effects on materials' thermal properties and aging effects, such as the substrate solder crack considered in the adaptive thermal model in Chapter 5. However, the improved Cauer-type TEC model is a simplified 1D model. In order to model the thermal behavior of an IGBT module with multiple chips and complex thermal cross-coupling effects, a better choice is the digital filter thermal model. However, since the digital filter thermal model does not have physical meanings, it is not straightforward to include aging effects in the model.

In Chapter 6, multiple aging processes (caused by different mechanisms) of IGBT modules were monitored by only acquiring package surface temperatures at a few selected points. The proposed method was based on the physics-of-failure of the IGBT modules, which was interpreted via abnormal heat generation and heat dissipation path degradation. Further, by taking advantage of the linear thermal behavior of the IGBT modules and introduction of new aging indicators k_{hc} and α_P, the proposed method was capable of monitoring the major aging mechanisms and detecting which aging process or

processes occur, which is an advantage over the existing techniques. Also, the implementation of the proposed method has lower hardware complexity and does not affect power converter operation.

In Chapter 7, a novel frequency domain thermal and weak points analysis method was presented. In the first part of the chapter, an online frequency-domain junction temperature estimation method for IGBT modules was proposed. The proposed method characterized the dynamical thermal behavior of an IGBT module by an LTI system. Then, the junction temperature was estimated in the frequency domain by using the frequency responses of the LTI system and FFT-based analysis of the power losses generated in the IGBT module. The proposed method was computationally efficient, had high-fidelity, and was easy to build. In the second part, the bottleneck weak point(s) that limits the lifetime of IGBTs under complex loading conditions was analyzed in the frequency domain. As the aging of the weak points are caused by thermomechanical stresses, the typical frequency responses of temperatures at the weak points of a general IGBT module were analyzed. This revealed that the IGBT power losses at loading conditions with different frequency spectra stress the weak points differently. Therefore, the information on the aging mode(s) of the IGBT can easily be obtained in the frequency domain. The analysis in the frequency domain can help classify the power converter duties in terms of the aging modes of the "standard" IGBT module.

The main contributions of this research are summarized as follows:

1. A comprehensive survey of state-of-the-art thermal models and aging monitoring techniques for IGBT modules was presented. These thermal

models were discussed in terms of accuracy, complexity, and computational cost. Typical drawbacks of the aging monitoring techniques were discussed.

2. A new method of constructing an improved low-order Cauer-type TEC model for IGBT modules was proposed. Compared to the conventional Cauer-type TEC, the proposed Cauer-type TEC had a slightly higher order but greatly improved the accuracy of the transient junction temperature estimation for IGBT modules.
3. Using low-order IIR digital filters for accurate real-time junction temperature estimation of IGBT modules was proposed. The transient junction temperature of IGBT modules can be accurately estimated by using the IIR filters with the orders even lower than those of the Foster-type TECs.
4. An EHPP-based TEC model for IGBT modules, where the parameters have been made adaptive online to substrate solder cracks inside the IGBT modules, was proposed in this research. To the author's knowledge, it is the first time that the aging effects are included in the thermal behavior modeling of IGBT modules.
5. A real-time aging monitoring method for IGBT modules using 2D case temperatures was proposed. The proposed method is effective for monitoring major aging processes and identifying their mechanisms in an IGBT module, such as bond wire liftoff, metallization aging, and substrate solder aging. This method is simple to use and easy to implement. To the author's knowledge, this is the first work using surface temperatures for the monitoring of IGBT major aging processes.

6. A computationally efficient, high-fidelity, easily built, online, frequency-domain junction temperature estimation method for IGBT modules was proposed. The accuracy of the proposed method is comparable to the FEA method, but the computational cost of the proposed method is comparable to the TEC model.
7. The frequency domain thermal analysis method was extended to estimate the temperatures at the weak points of IGBT modules and determine the bottleneck weak point(s) for a given application operation cycle. This may help to classify power converter duty cycles and improve power converter design for specific applications in terms of reliability.

8.2 Recommendations for Future Research

This dissertation research has developed new cost-effective real-time thermal models that are more accurate than the traditional TEC models, a method for real-time monitoring of the major aging processes, and a weak point aging mode analysis method. These models and methods, however, need to be further improved for more complex scenarios in current or future real-world applications.

As Si IGBT modules usually operate in a temperature range of a few tens of degrees, e.g., 70-125 ºC in electric vehicle applications, temperature effects on materials' thermal properties are negligible. The thermal models developed are linear models, which neglect the materials' nonlinearities. However, SiC IGBT may be commercially available in the future. The SiC IGBT-based power converter may operate in a much wider temperature range, as the maximum junction temperature can be 250 °C or higher. For this scenario, it is suggested that research is needed to study the potential impact of the

nonlinearities of the materials' thermal properties on the SiC IGBT device's thermal behavior. Nonlinear thermal models can be built by adding a scheme to update the thermal models' parameters at different device temperatures.

In this dissertation research, an implementation of the health monitoring method uses two thermocouples (one placed at a relatively hot spot and the other placed at a relatively cold spot at the bottom surface of the baseplate) for each switch of the IGBT module. For a 3-phase power inverter, 12 thermocouples will be used. However, the number of thermocouples can be reduced; and their locations can be optimized for a more effective implementation in real-world applications. It is recommended that a sensitivity analysis be conducted of the changes in the values of equivalent thermal resistances to the aging processes of different weak points in an inverter module. Another approach to reducing the cost of temperature sensors is to take advantage of low-cost, large-area printed organic temperature sensors on flexible substrates, e.g., [85]-[88]. An organic temperature sensor array may be placed in the thermal grease between an IGBT module and a cold plate. This approach can realize 2D case temperature sensing in real-world applications and collect enough information for a more detailed analysis of the device's health status.

The weak point analysis in the frequency domain can be advantageous in aging mode analysis with respect to the time-domain cycle counting methods, especially when considering computational costs. Unlike the time-domain methods, the proposed method cannot provide a specific lifetime prediction for each weak point of an IGBT module. Because this method doesn't provide a histogram of temperature cycles, therefore, it cannot use the N_f cycling curves of the IGBT module. So far, the bottleneck weak

point(s) are roughly determined by observing the power loss frequency spectra. It is recommended that, in a future work, damage indicators be extracted from the temperature spectra for each of the weak points to quantifiably compare their severities. If this can be achieved, rules for power converter duty classification in terms of the aging modes of the "standard" IGBT module can be further established. The duty classification can benefit power converter design. As the aging mode of IGBT modules for a typical duty cycle can be known before power converter production, the design of the IGBT modules can be modified to reduce the thermal stress at the bottleneck weak point(s) to prolong the lifetime of the power converter. This can lead to a cost-effective, field-oriented, reliable design for power converters.

Appendix

Suppose that the *i*th layer is subdivided into N_{sub} sublayers with the same thickness and is not the thick baseplate layer. Then the heat conduction areas on the top and bottom surfaces, $A(z_{i,top})$ and $A(z_{i,bottom})$, respectively, of the layer are very close, i.e.,

$$A(z_{i,top}) \approx A(z_{i,bottom}) \tag{A.1}$$

Then the lumped-capacitance approximation error of each sublayer, $CE_{lc,i,sub}$, can be calculated by multiplying $c_{v,i} \cdot A(z_{i,top})$ by the temperature distribution approximation error of the sublayer, i.e., a triangle shadow area in Fig. A.1.

$$CE_{lc,i,sub} \approx c_{v,i} A(z_{i,top}) \cdot \frac{\frac{1}{2N_{sub}}[T(z_{i,top}) - T(z_{i,bottom})]}{T_j - T_c} \cdot \frac{1}{N_{sub}} (z_{i,bottom} - z_{i,top})$$

$$\approx \frac{1}{2{N_{sub}}^2} \frac{R_{th,i}}{R_{th,jc}} C_{th,i} \tag{A.2}$$

where the difference between the actual and estimated temperatures at a position is normalized in terms of $(T_j - T_c)$. Then, $CE_{lc,i}$ is the sum of $CE_{lc,i,sub}$ of all the sublayers,

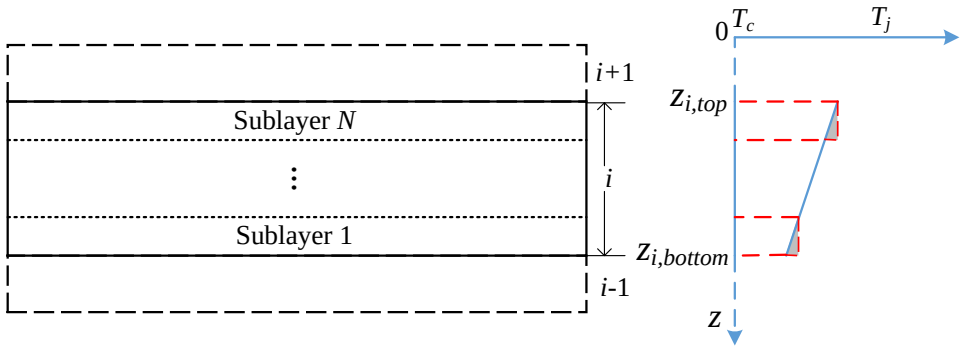


Fig. A.1: The temperature distribution approximation error of the *i*th layer subdivided into *N* sublayers.

i.e., $CE_{lc,i} = N_{sub} \cdot CE_{lc,i,sub}$, which leads to (3.3).

Let Q_i be the amount of heat stored in the ith layer. Then, the amount of heat stored in the ith layer when $(T_j - T_c)$ is raised by 1 ºC, i.e., $Q_i/(T_j - T_c)$, can be calculated as follows:

$$\begin{aligned}
\frac{Q_i}{T_j - T_c} &= \int_{z_{i,top}}^{z_{i,bottom}} \frac{T(z) - T_j}{T_j - T_c} c_v A(z) dz \\
&= \int_{z_{i,top}}^{z_{i,bottom}} \frac{T(z_{i,top}) - T_c}{T_j - T_c} c_v A(z) dz - \int_{z_{i,top}}^{z_{i,bottom}} \frac{T(z_{i,top}) - T(z)}{T_j - T_c} c_v A(z) dz \\
&\approx \frac{\sum_{j=1}^{i} R_{th,j}}{R_{th,jc}} C_{th,i} - \frac{\frac{1}{2} R_{th,j}}{R_{th,jc}} C_{th,i} \\
&= \frac{1}{R_{th,jc}} C_{th,i} \left(\sum_{j=1}^{i} R_{th,j} - \frac{1}{2} R_{th,i} \right)
\end{aligned} \tag{A.3}$$

By adding the heat stored in all the layers, the equation (3.4) for calculating $C_{th,tot}$ is then obtained.

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