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Thermal Comparison of Polycrystalline Diamond and AlN in Power Semiconductor Device Packages

Brandon M. Guenther
University of Nebraska - Lincoln

THERMAL COMPARISON OF POLYCRYSTALLINE DIAMOND AND ALN IN POWER SEMICONDUCTOR DEVICE PACKAGES

by

Brandon M. Guenther

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THERMAL COMPARISON OF POLYCRYSTALLINE DIAMOND AND ALN IN POWER SEMICONDUCTOR DEVICE PACKAGES

Brandon M. Guenther, M.S.

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Adviser: Jerry L. Hudgins

The desire for improved thermal management in power semiconductor device packaging is becoming increasingly important due to the progression towards implementing wide-bandgap semiconductor (WBG) materials, such as silicon carbide (SiC) and gallium nitride (GaN). These semiconductor materials have the capability of operating at much higher voltages, temperatures, and frequencies compared to standard silicon-based devices. However, utilizing this enhanced operating region will induce larger thermomechanical stress within the package structure as a consequence of operating at higher junction temperatures around 250-300 °C. To handle the higher and improved operating characteristics from the WBG semiconductors, the current package technology is modified by increasing heat flow through its layers. This modification will improve reliability and operating lifetime of device packages in high power applications.

The focus of this research was on enhancing the thermal performance of the direct bond copper (DBC) substrate in a standard package design by considering the implementation of polycrystalline diamond (PCD) films as a replacement for the commonly used DBC (AlN) substrates. The use of these PCD films in a standard device package has been examined in detail using an emissivity-calibrated thermal (IR) imaging

camera experiment that measures and compares the top surface temperature profiles of a commercial module package and two PCD films (Co-PCD and Cu-PCD).

The results from this thermal experiment showed that both of the PCD films reached steady state considerably faster than the AlN substrate. The accelerated top surface temperature profiles of the PCD films demonstrated a faster thermal transient response time, an increased heat flow, and lower thermal resistance that can potentially handle the high operating characteristics of WBG semiconductors. In addition, the Co-PCD film displayed a faster thermal transient response time compared to the Cu-PCD film. The resulting thermal analysis on PCD films can be used to aid future research pertaining to dielectric breakdown strength tests, studying lateral heat flow, ways of interconnection into a device package, and mechanical behavior under thermomechanical stress within a package.

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NOMENCLATURE

A	Surface area, m^2
A_{hi}	Effective cross-sectional surface area for i^{th} layer (heat spreading) of device package, m^2
c_i	Specific heat capacity for i^{th} layer of device package, J/kg*K
$C_{thermal}$ & C_i	Thermal capacitance of surface/region and thermal capacitance for i^{th} layer of device package, J/K
$C_{i(CE)}$	Thermal capacitance for i^{th} layer of device package from Cauer-equivalent RC circuit, J/K
d_i	Thickness for i^{th} layer of device package, m
$\frac{dT}{dx}$	Temperature gradient across a surface or region, K/m
E_C	Conduction band energy, eV
E_V	Valence band energy, eV
h	Convective heat transfer coefficient, W/m^2K
i and n	Indexes for placement and number of material layers in a device package, respectively
I	Current through a wire or resistor of an electrical circuit, A
k & k_i	Thermal conductivity of material and thermal conductivity for i^{th} layer of device package, W/m**.**K
L	Length, m
L_{PCD}	Length of PCD films, mm

L_1 & L_2	Length of baseplate/DBC substrate and copper/solder layers, respectively, cm
P_D	Input power dissipation, W
q	Heat flux, W
Q_{hp}	Heat dissipation through all material layers of Powerex package (Cauer-equivalent RC circuit), W
$Q_{hp,new}$	Heat dissipation through only DBC substrate of Powerex package (DBC Cauer RC circuit), W
R_{c1}	Constriction resistance for heat flow between baseplate and solder layers of Powerex package, K/W
R_{e1}	Edge effects resistance for heat flow across the solder layer of Powerex package, K/W
$R_{electrical}$	Electrical resistance through a wire of an electrical circuit, Ω
$R_{thermal}$ & R_i	Thermal resistance of surface/region and thermal resistance for i^{th} layer of device package, K/W
$R_{i(CC)}$	Thermal resistance for i^{th} layer of device package from calculated Cauer RC circuit, K/W
$R_{i(CE)}$	Thermal resistance for i^{th} layer of device package from Cauer-equivalent RC circuit, K/W
R_{hs}	Thermal resistance between heat sink and surrounding environment (air), K/W
R_{j-a}	Thermal resistance for junction-to-ambient of device package, K/W
R_{j-c}	Thermal resistance for junction-to-case of device package, K/W

t	Period of time, s
$T_{ambient}$ (T_a)	Temperature of environmental conditions, °F or °C
T_{atm}	Atmospheric temperature of environment (camera setting), °F or °C
T_A & T_B	Temperatures on opposing sides of a layer or region, °F or °C
$T_A(t)$ & $T_B(t)$	Temperatures on opposing sides of a layer or region as function of time, °F or °C
$T_{AB}(t)$	Temperature profile of an equivalent thermal RC network as function of time, °F or °C
T_{bp}	Temperature at top surface of baseplate for Powerex package, °F or °C
$T_{bp(CC)}$	Temperature at top surface of baseplate for Powerex package from calculated Cauer RC circuit, °F or °C
$T_{bp}(t)$	Temperature at top surface of baseplate for Powerex package as function of time, °F or °C
T_{case} (T_c)	Temperature at bottom of device package (Powerex package), °F or °C
$T_{case(CC)}$	Temperature at bottom of device package for Powerex package from calculated Cauer RC circuit, °F or °C
$T_{case}(t)$	Temperature at bottom of the device package for Powerex package as function of time, °F or °C
$T_{case,new}(t)$	New temperature at bottom surface of DBC substrate as function of time (DBC Cauer RC circuit), °F or °C
T_{dbc}	Temperature at top surface of the AlN layer for Powerex package, °F or °C

$T_{dbc}(t)$	Temperature at top surface of AlN layer for Powerex package as function of time, °F or °C
$T_{dbc,new}(t)$	New temperature at top surface of AlN layer as function of time (DBC Cauer RC circuit), °F or °C
$T_{drop,aln}$	Temperature drop across ceramic layer (AlN) in Powerex package, °F or °C
$T_{drop,bp}$	Temperature drop across baseplate layer in Powerex package, °F or °C
$T_{drop,bp(CC)}$	Temperature drop across baseplate layer in Powerex package from calculated Cauer RC circuit, °F or °C
$T_{drop,cu}$	Temperature drop across copper layers in Powerex package, °F or °C
$T_{drop,sol}$	Temperature drop across solder layer in Powerex package, °F or °C
$T_{drop,sol(CC)}$	Temperature drop across solder layer in Powerex package from calculated Cauer RC circuit, °F or °C
T_j	Temperature of junction/device, °F or °C
$T_{j,peak}$	Maximum temperature of junction/device, °F or °C
T_{obj}	Apparent temperature measurement from thermal (IR) imaging camera, °F or °C
$T_{reference}$	Temperature at top copper layer of DBC substrate (Cauer-equivalent RC circuit), °F or °C
$T_{reference,new}$	New temperature at top copper layer of DBC substrate (DBC Cauer RC circuit), °F or °C
T_{refl}	Reflective temperature of surroundings (camera setting), °F or °C

T_{sol}	Temperature at top surface of solder layer (for baseplate connection) for Powerex package, °F or °C
$T_{sol}(t)$	Temperature at top surface of solder layer (for baseplate connection) for Powerex package as function of time, °F or °C
T_x	Temperature at any location on a device package below junction temperature, °F or °C
V_A & V_B	Voltages on opposing nodes of an electrical circuit, V
V_{hi}	Effective volume for i^{th} layer (heat spreading) of device package, m^3
W_{atm}	Radiation power of emission from the atmosphere, W
W_{obj}	Radiation power of emission from an object, W
W_{PCD}	Width of PCD films, mm
W_{refl}	Radiation power of reflected emission from ambient sources, W
W_1 & W_2	Width of baseplate/DBC substrate and copper/solder layers respectively, cm
W_3	Width difference between respective layers, cm
$Z_{th(j-c)}$	Transient thermal impedance from junction-to-case of a device package, K/W
$Z_{th(j-x)}$	Transient thermal impedance from junction-to-any location below the junction of device package, K/W
ΔT_{AB}	Temperature difference between a layer/region, °F or °C
ΔV_{AB}	Voltage difference between two nodes of an electrical circuit, V
ε	Emissivity of a material or surface
ρ_i	Mass density for i^{th} layer of device package, kg/m^3

τ	Transmittance of a material or surface
τ_i	Time constant for i^{th} layer of a device package, s
AC	Alternating current
AlN	Aluminum nitride
AlSiC	Aluminum silicon carbide
BJT	Bipolar junction transistor
CC	Calculated Cauer RC circuit
CE	Cauer-equivalent RC circuit
CF	Carbon fiber
Co	Cobalt
Co-PCD	Polycrystalline diamond film coated with cobalt (top surface)
CO_2	Carbon dioxide
CTE	Coefficient of thermal expansion
Cu	Copper
Cu-PCD	Polycrystalline diamond film coated with copper (top and bottom surfaces)
CVD	Chemical vapor deposition
DBC	Direct bond copper
DC	Direct current
EM	Emissivity
GaN	Gallium nitride
FEA	Finite element analysis
HP-75C	Hot plate temperature at 75 °C

HP-150C	Hot plate temperature at 150 °C
HP-200C	Hot plate temperature at 200 °C
HVIGBT	High voltage insulated gate bipolar transistor
IGBT	Insulated gate bipolar transistor
IR	Infrared
IGBTMOD	Insulated gate bipolar transistor module
MMC	Metal matrix composite
MOSFET	Metal-oxide-semiconductor field-effect transistor
NETD	Noise equivalent temperature difference
PbSn	Lead-tin alloy
PCD	Polycrystalline diamond
Si	Silicon
SiC	Silicon carbide
S.S.	Steady state
WBG	Wide bandgap semiconductor

CHAPTER 1

BACKGROUND

1.1 Background of Power Modules

A majority of power electronics today utilize power semiconductor devices to operate and control a variety of applications. These devices behave as switches in a system to convert power from AC-to-DC (rectifier), DC-to-DC, DC-to-AC (inverter), or AC-to-AC, depending on the application. Many applications use devices packaged as modules. A power module is a physical containment structure that encloses single or multiple power semiconductor devices. Besides protecting these devices from environmental conditions, power modules provide excellent thermal management, electrical isolation and interconnection, and mechanical support. Maintaining these factors is the key for power semiconductor devices to achieve and maintain their full operational potential.

One priority of research in power modules is focused on the package design and its characteristics related to thermal performance. The thermal behavior of a package is of importance because it is the leading cause of device failures in power converter systems. Specifically, proper thermal management for a power semiconductor device involves keeping its junction temperature below its designed maximum during its operation. This is accomplished by removing heat dissipated from the device as quickly and efficiently as possible.

The design of the module is based on the amount and type of power semiconductor devices/chips held within. Due to the wide selection of power semiconductor devices (diodes, thyristors, metal-oxide-semiconductor field-effect

transistors (MOSFETs), bipolar junction transistors (BJTs), insulated-gate bipolar transistors (IGBTs), etc.), there is a large range of possible configurations, voltage and current ratings, and allowed power dissipation values.

Most of the power semiconductor devices are fabricated using silicon. Over the past 15 years, the use of silicon carbide (SiC) power devices has increased with improvements in some of the operating characteristics, as compared to silicon-based devices. Another wide-bandgap semiconductor material being developed for power electronics applications is gallium nitride (GaN). These materials have energy bandgaps in the range of 2-4 eV compared to the standard 1.12 eV (at room temperature) for silicon, as shown in Figure 1.1. Larger energy bandgaps allow devices to operate in higher temperatures and under higher electric fields. Listed in Table 1.1 are some of the advantages of wide bandgap semiconductors, specifically SiC, and their impact on power electronic converter systems (x symbol used in this table represents “times more than Si”) [1].

Figure 1.1. Energy bandgap comparison of SiC/GaN v. Si.

Table 1.1. Important properties of SiC devices.

Properties SiC Versus Si	Performance of SiC Devices	Impact on Power Circuit
Breakdown Field (10x)	Lower ON-State Voltage (2-3x)	Higher Efficiency of Circuit
Thinner Epitaxial Layers (10-20x)	Faster Switching Speeds (100-1,000x)	Compact Circuits
Bandgap (3x)	Lower Leakage Currents (up to 10^4x)	Higher Acceptable Temperatures
Higher Thermal Conductivity (3.3-4.5 W/m.K v. 1.5 W/m.K)	Higher Chip Temperatures (250-300 °C v. 125 °C)	Higher Pulsed Power
Melting Point (2x)	Higher-Temperature Operation (3x)	Higher Continuous Current Densities

However, there is a lack of available package materials and designs to take full advantage of the potentially enhanced operating region for wide bandgap devices because the current technology is based on optimizing performance of silicon parts.

1.2 Package Design of Power Modules

The design of the package for power modules is essential in sustaining excellent thermal and electrical characteristics. The standard package design used for silicon-based devices provides low thermal resistance, high electric field isolation, and minimal variations in the coefficient of thermal expansion (CTE) to minimize stress and strain between material layers. The standard module consists of four fundamental material regions: the semiconductor die (device), the direct-bond copper (DBC) substrate, solder layers, and the baseplate (copper (Cu) or aluminum silicon carbide (AlSiC) metal matrix composite). The exact construction of this package can be seen in Figure 1.2.

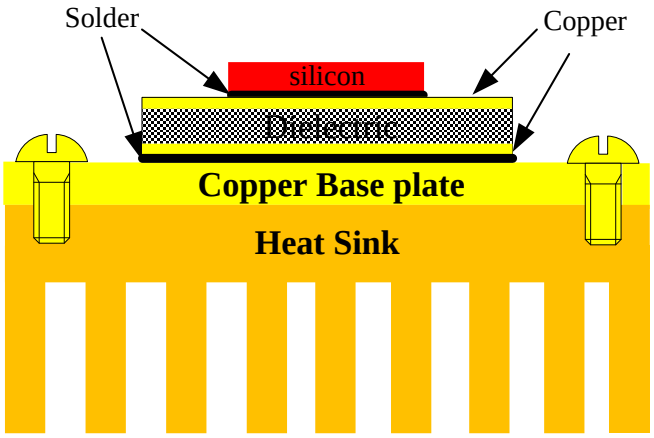

Figure 1.2. Power semiconductor device package structure [2].

As shown in Figure 1.2, the semiconductor die is attached directly to the DBC substrate by a thin solder layer. This die acts as a heat source when the device is turned-on and operational. Typically this area is referred to as the "active area" of the package. The DBC substrate provides electrical isolation between the semiconductor die and baseplate while further providing moderate thermal conductivity. It consists of a ceramic electrical insulator that is sandwiched between two pure Cu layers. Generally the ceramic isolator in most packages is aluminum nitride (AlN).

The baseplate is the final package material layer and consists of a metal that provides large heat dissipation in both the vertical and lateral directions while providing mechanical stability. Further, the baseplate of the package is typically attached to a heat sink to further enhance the heat dissipation.

1.3 Failures of a Device Package

Modules often fail due to thermal/power cycling events. This occurs during normal operating conditions when the temperature of the semiconductor die experiences enormous swings from their minimum to maximum values during short conduction pulses, as shown below in Figure 1.3.

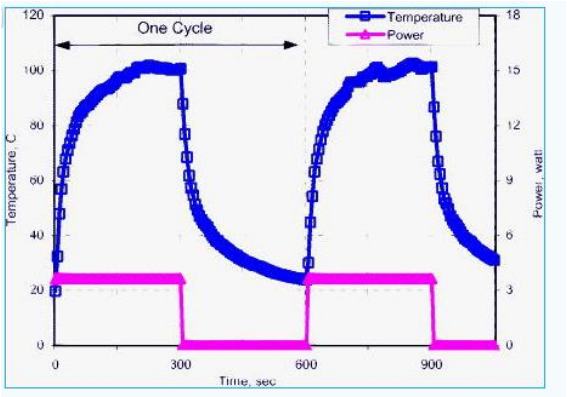

Figure 1.3. Example of a thermal/power cycling event experienced by a device package [3].

During heating and cooling of the device, these dissimilar materials expand and contract at different rates due to their respective CTEs. This difference causes thermomechanical stress in the die attachment, DBC substrate, and baseplate of the power semiconductor device package. Silicon carbide and gallium nitride devices that can potentially operate above 200 °C junction temperatures will induce larger thermomechanical stresses that cannot be tolerated using conventional module package technology.

1.4 Enhancing Thermal Performance of DBC Substrate

Solder, contact pads, and wirebond technology will continue to be used as an interconnection of material layers and microelectronics in modules for the foreseeable future. The baseplate design already uses minimal material to maintain structural

integrity of the package. Therefore, thermal performance can be greatly enhanced by new material systems to replace the DBC while maintaining the current use of interconnection technology and baseplate designs.

A standard DBC substrate consists of a ceramic (AlN) layer surrounded by bonded copper layers on its top and bottom surfaces, as seen in Figure 1.4.

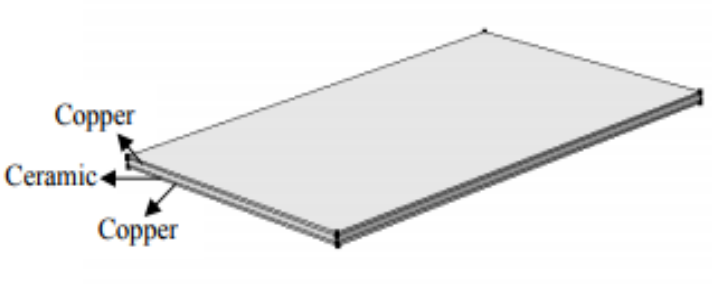

Figure 1.4. Standard DBC substrate used in a device package.

Improvement in the DBC substrate involves considering different material choices for the ceramic layers. This is the primary focus of this thesis. Specifically, it focuses on changing the ceramic layer to a material that has exceptional thermal behavior while keeping similar or better electrical breakdown properties, such as AlN. This work investigates polycrystalline diamond (PCD) as a replacement for AlN. Polycrystalline diamond is fabricated using a carbon dioxide (CO_2) laser to induce carbon deposition from an acetylene flame [5]. This type of material possesses great toughness, long durability, high dielectric breakdown strength, and according to [6], it has the highest thermal conductivity available for any engineering material.

Bibliography for Chapter 1

[1] R. Singh and S. Sundaresan, "Fulfilling the Promise of High-Temperature Operation with Silicon Carbide Devices: Eliminating bulky thermal management systems with SJTS," *IEEE Power Electronics Magazine*, Vol. 2, No. 1, pp. 27-35, Mar. 2015.

[2] B. Du, J. L. Hudgins, E. Santi, A. T. Bryant, P. R. Palmer and H. A. Mantooth, "Transient Electrothermal Simulation of Power Semiconductor Devices," in *IEEE Transactions on Power Electronics*, Vol. 25, No. 1, pp. 237-248, Jan. 2010..

[3] S. B. Park, R. Joshi, I. Ahmed and S. Chung, "Comparative Studies on Solder Joint Reliability of Plastic and Ceramic Ball Grid Array Packages of the Same Form Factor Under Power and Accelerated Thermal Cycling," *ASME Journal of Electronic Packaging*, Vol. 130, No. 4, pp. 041004-041004-10, Nov. 2008.

[4] L. Xu, Y. Zhou and S. Liu, "DBC substrate in Si- and SiC-based power electronics modules: Design, fabrication and failure analysis," *2013 IEEE 63rd Electronic Components and Technology Conference*, Las Vegas, NV, pp. 1341-1345, 2013.

[5] T. McKindra, S. Patil, M.J. O'Keefe, Z.Q. Xie and Y.F. Lu, "Characterization of diamond thin films deposited by a CO_2 laser-assisted combustion-flame method," *Materials Characterization,* Vo. 61, No. 6, pp. 661-667, Mar. 2010.

[6] "What is PCD?" *US Synthetic Bearings.* 2014. http://ussbearings.com/bearings_site/reserach_article/947/.

CHAPTER 2

EXPERIMENTAL PACKAGE DESIGNS

2.1 Introduction

This chapter introduces relevant layers of two module package designs that will be compared for their thermal management qualities. The first package design originates from a Powerex IGBT module (CM1800HC-34N). This package was deconstructed from its original form to ensure an adequate comparison with the other design. The second package design consists of PCD films that were fabricated by a combustion flame chemical vapor deposition (CVD) process. These films are compared to the DBC substrate of the module package referenced above. Then in the final section, a direct comparison will be made between the two experimental package designs based on their respective theoretical advantages and disadvantages towards improvement of thermal management.

2.2 Powerex IGBTMOD Module

Powerex is a power semiconductor manufacturer. They manufacturer a variety of products related to IGBTs, HVIGBTS, intelligent power modules, rectifiers, thyristors, custom power modules and assemblies. The particular module chosen for this research was the Single IGBTMOD™ HVIGBT Module, shown in Figure 2.1. This module operates at a maximum of 1800 A/1700 V and is primarily utilized in converter applications. It encloses multiple IGBT's each with an anti-parallel diode. The IGBT module was modified in order to directly compare it with the diamond insulating layer.

Figure 2.1. Single IGBTMOD HVIGBT Power Module [1].

2.2.1 Deconstruction Procedure

The deconstruction procedure of the IGBT power module began by removing the black plastic cover. Figure 2.2 shows the top view of the uncovered power module.

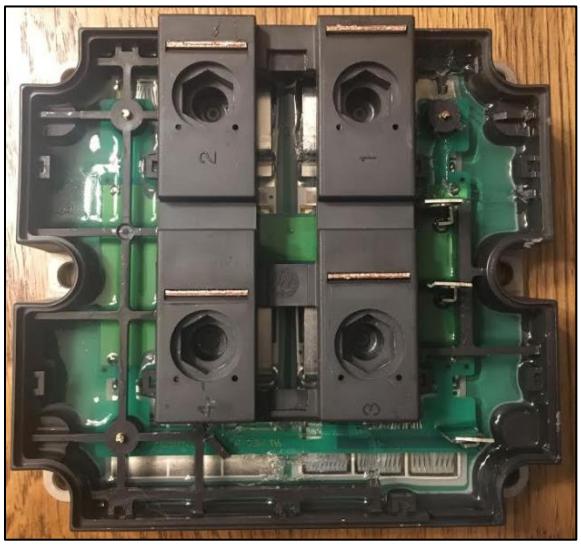

Figure 2.2. Top view of uncovered power module.

After removal of the black plastic cover and associated plastic border, the silicone gel that surrounds the entire interior of the power module was removed by using xylene. Figure 2.3 demonstrates the power module removed from the silicone gel.

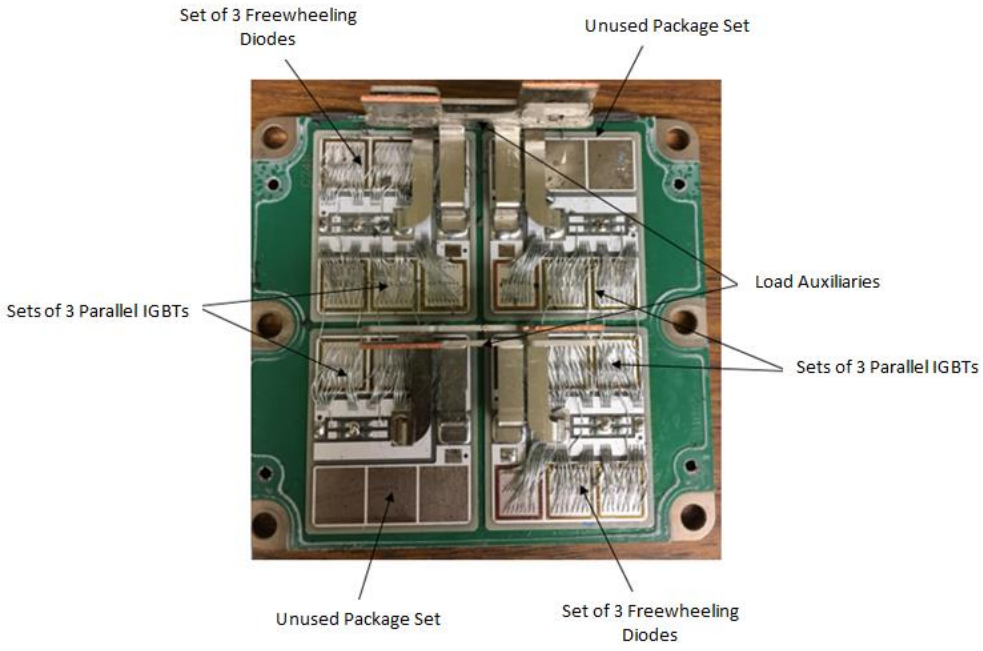

Figure 2.3. Top view of power module without silicone gel.

Next, a Dremel circular saw and miter saw (both with diamond-impregnated blades) were used to cut through portions of the power module. Portions of the baseplate and DBC were obtained for thermal performance testing of the Powerex package, as shown in Figure 2.4.

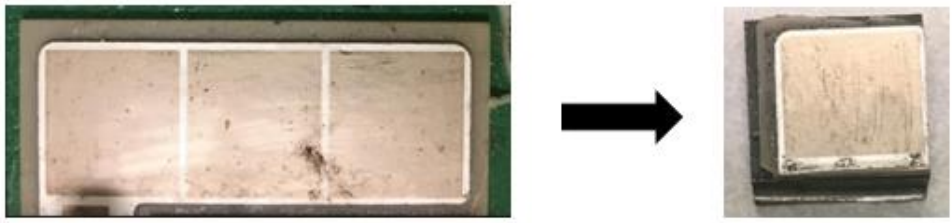

Figure 2.4. Conversion from unused package set (left) to single device package (right).

2.2.2 Structure and Layout of Powerex Package

This Powerex package consists of a top layer tinned with solder, a DBC substrate, an interconnecting solder layer, and a baseplate. As the tinned solder layer is miniscule compared to the other layers, it can be ignored in further analysis. Therefore, the DBC

substrate, interconnecting solder layer, and baseplate of the package are of main concern. Figure 2.5 is a top and cross-sectional view of these layers within the package.

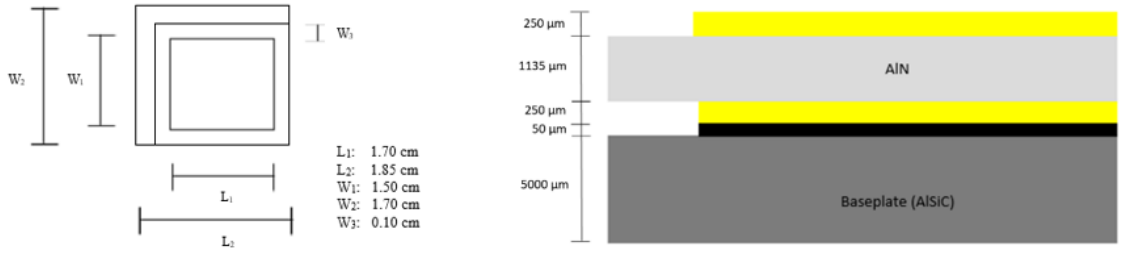

Figure 2.5. Top (left) and cross-sectional (right) view of Powerex package.

As shown in the Figure 2.5 above, this package's DBC substrate was composed of Cu sintered to AlN. The baseplate for this package was constructed of a metal matrix composite alloy known as aluminum silicon carbide metal matrix composite (AlSiC MMC). Metal matrix composites are being utilized more in baseplates and in other regions of a power semiconductor device package due to their controlled variability in material properties. Table 2.1 displays a few of these important material properties for AlSiC and other layers of the Powerex package.

Table 2.1. Material properties of layers in Powerex package.

Parameter	**Copper (Cu)**	**Aluminum Nitride (AlN)**	**Solder (PbSn)**	**AlSiC MMC**
Thermal Conductivity (W/mK)	401	180	50	175
Specific Heat Capacity (J/kgK)	385	800	173	781
Thermal Diffusivity (mm^2/s)	$1.17*10^{-4}$	$0.69*10^{-4}$	$0.34*10^{-4}$	$0.75*10^{-4}$
CTE (ppm/K)	17.0	4.5	23.0–29.0	4.0–21.0
Dielectric Strength (kV/mm)	-	17	-	-
Density (kg/m^3)	8933	3260	8600	3000

2.3 Polycrystalline Diamond Films

Research over the years has continued to expand to find ways for improving electronic packaging. One of the topics with an insufficient amount of research is the inclusion of diamond into a package. Diamond should be of interest because it possesses the highest thermal conductivity of any material available. There are other quality material properties that diamond maintains, but none is as important as thermal conductivity for packaging. This property alone solves the demand for greater heat dissipation in electronic packaging. For that reason, the implementation of diamonds into power semiconductor device packages needs further investigation.

The specific type of diamond chosen for this research was PCD. The Laser Assisted Nano Engineering Lab (LANE) at the University of Nebraska-Lincoln has fabricated two PCD films that can potentially replace the DBC substrate of the standard power semiconductor device packages.

2.3.1 Fabrication of PCD Films

The fabrication processes for both PCD films were completed by depositing PCD films on bulk copper/carbon adaptive composite materials using combustion flame CVD [2]. First, the copper/carbon-fiber (CF) substrate was created by the densification technique shown in Figure 2.6. This technique produces a substrate with tunable Cu and CF volume fractions. The volume percentage of CF is an important factor in determining the CTE. The higher the carbon content, the better match of CTEs between the substrate and the diamond film deposited.

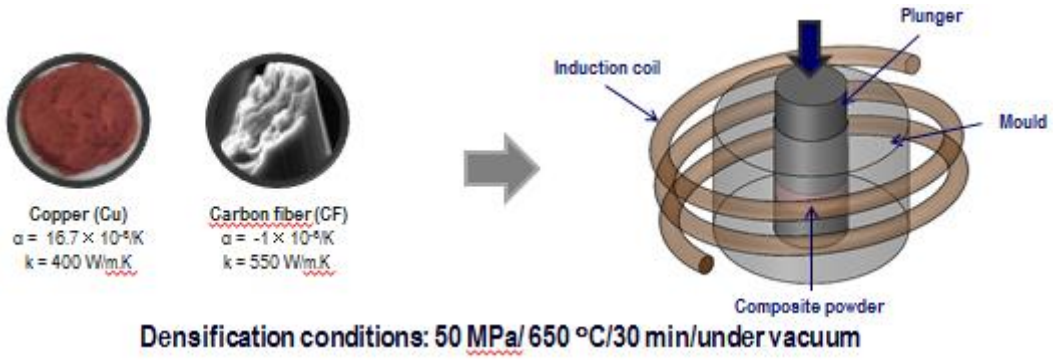

Figure 2.6. Densification technique used to create the copper/carbon-fiber substrates.

Once the substrate is formulated, PCD films are deposited on it using combustion flame CVD, as shown in Figure 2.7. When using this approach, it is important to note that the substrate temperature, cooling system, and substrate distance from the inner flame are crucial parameters for controlling the diamond deposition rate and diamond quality. In addition, the PCD film thickness is proportionally related to the length of the deposition times. As the deposition time increases, the grain size and the film thickness increase.

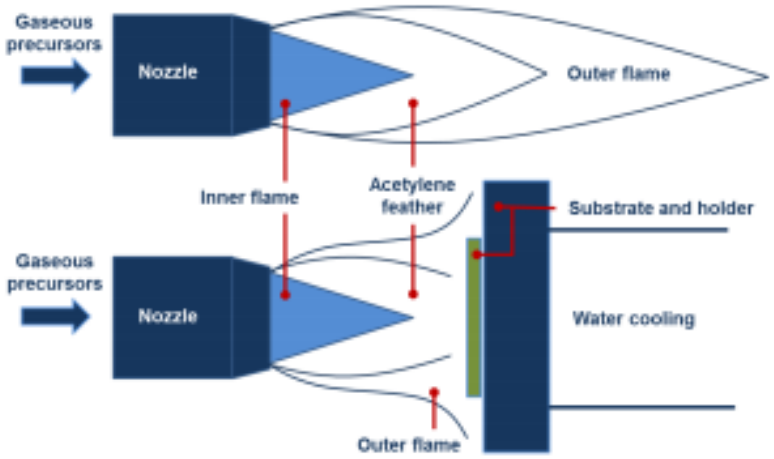

Figure 2.7. Demonstration of the combustion flame CVD used on the PCD films [3].

Once the diamond films reach a desired thickness, they are peeled off of the composite substrate using a mechanical procedure, as shown in Figure 2.8. Once this

procedure is executed, the PCD films are ready to be tested as potential DBC substrate replacements. The final product of the PCD films can be seen in Figure 2.9.

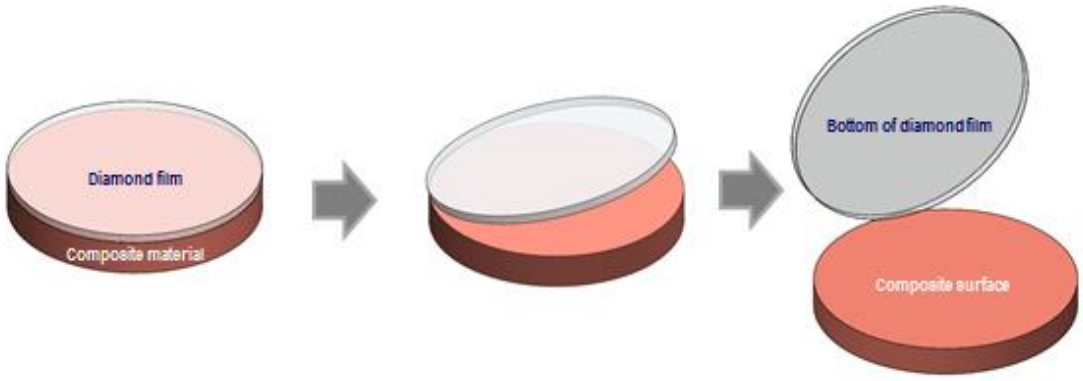

Figure 2.8. Mechanical procedure for removal of PCD films from composite surface.

Figure 2.9. Images of PCD Films (Left: Co-PCD, Right: Cu-PCD).

2.3.2 Structure and Layout of PCD Films

The fabrication process developed by LANE generates two different PCD films. One of those PCD films is coated only on the top surface with cobalt (Co-PCD) while the other sample is coated on its top and bottom surface with copper (Cu-PCD). A top and cross-sectional view of Co-PCD and Cu-PCD films with each of their dimensions is shown in Figures 2.10 and 2.11, respectively.

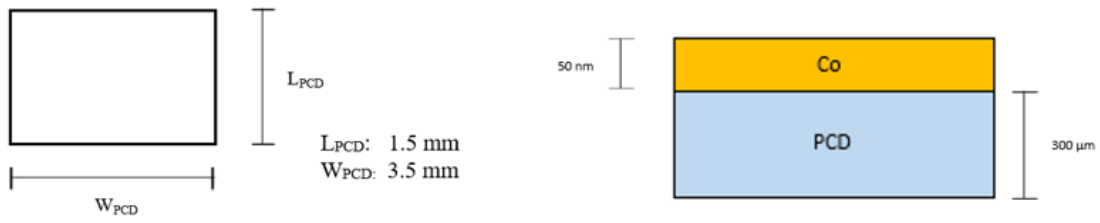

Figure 2.10. Top (left) and cross-sectional (right) views of Co-PCD film.

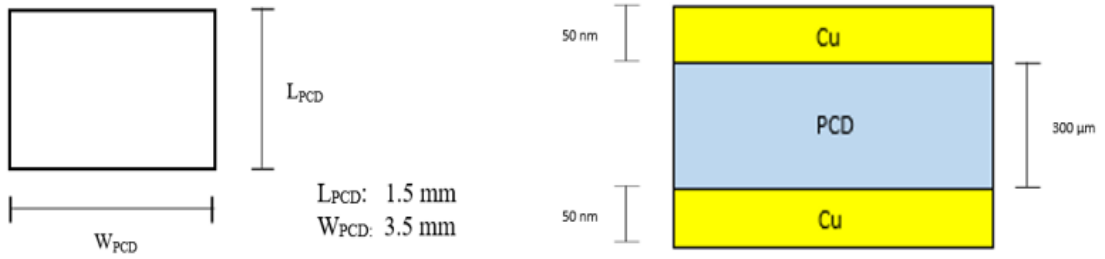

Figure 2.11. Top (left) and cross-sectional (right) views of Cu-PCD film.

This smaller size for the PCD films as the DBC substrate is achievable due to the much improved material properties that PCD possesses as the new ceramic material. As stated early, diamond has one of the highest measured thermal conductivities of any known material. Generally, this value varies between 1000 to 2000 W/m*K depending on the deposition process and grain boundary effects in its fabrication [4].

Another significant material property of diamond is the dielectric breakdown strength. The dielectric breakdown strength measures the ability of an insulator to withstand a certain maximum breakdown voltage (electric field) without allowing itself to become electrically conductive. For PCD this value ranges from 10 kV/mm to 0.6-1 MV/mm. According to [4], this wide range for the dielectric breakdown strength is due to the Poole-Frenkel effect (ordinarily between 10-100 kV/mm). These two material properties, along with the others, are a major reason why PCD is being explored as a

replacement material in power semiconductor device packages. Table 2.2 lists all of these important material properties for both PCD films. The implementation of these films as the DBC substrate has the potential to enhance the thermal, electrical, and mechanical performance for electronic packaging.

Table 2.2. Material properties of PCD films.

Parameter	**Polycrystalline Diamond (PCD)**	**Copper (Cu)**	**Cobalt (Co)**
Thermal Conductivity (W/mK)	1540	401	99.2
Specific Heat Capacity (J/kgK)	520	385	421
Thermal Diffusivity (m^2/s)	$0.846*10^{-3}$	$1.17*10^{-4}$	$2.66*10^{-5}$
CTE (ppm/K)	1.0	17.0	12.0
Dielectric Strength (kV/mm)	10 - 100,000	-	-
Density (kg/m^3)	3500	8933	8862

2.4 Potential Problems with PCD Films

With the experimental package designs introduced in the previous sections, further analysis was conducted on the PCD films for their respective advantages and potential problems if implemented as a replacement of the DBC substrate in the IGBT package. For a comparison between the two package designs, the solder and baseplate layers of the IGBT module will be excluded from the final results. Thus, only the electrically insulating substrate of the IGBT module will be directly compared with the PCD films.

There are still potential problem areas when using a material like PCD in a power semiconductor device package. For instance, one of the primary reasons PCD has limited

usage in electronic packaging is due to its extremely high cost. Roughly, PCD substrates cost about $10 per cubic millimeter. That price point is considerably higher than the process to manufacture AIN substrates. According to [5], the cost factor for PCD is three times greater than conventional AlN substrates. Consequently, most companies will select the lower-priced option for the capacity to mass produce components.

Another major concern with PCD substrates lies with their mechanical reliability when embedded into a package. Polycrystalline diamond possesses a CTE of 1.0 ppm/K, considerably lower than other materials typically used in power device packaging. The CTE mismatch between these different material layers can cause failures. As simulation results demonstrated in [6], a polycrystalline diamond system exhibited poor mechanical reliability in terms of high thermal stress and low safety factor (<1) in solder and top/bottom copper metallization layers, when benchmarked against an AlN system. The safety factor corresponds to the ratio of allowable stress to actual stress; thus, having a safety factor of less than 1 indicates a likely failure.

However, this outcome can be managed by paying close attention to the thickness of the PCD compared to the other layers in the substrate. As shown in Figure 2.12, the maximum thermal stress is reduced when the PCD's thickness is greater than the thickness of the other layers within the substrate. Therefore, it is crucial to find an appropriate balance of thicknesses between PCD and the other layers. For example, an acceptable assumption is a thickness ratio of 2:1 for polycrystalline diamond to copper layer thickness.

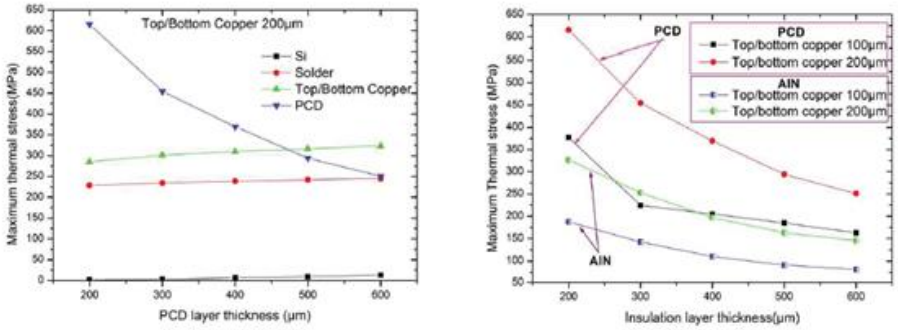

Figure 2.12. Thermal stress graphs of PCD and other material layers v. thickness of layers in a device package [6].

The final complication of using PCD films as the substitute for the DBC substrate is the attachment of the PCD films to the power semiconductor device and baseplate. The PCD fabrication process typically leaves behind rough top and bottom surfaces on the PCD films. As a result, these films are difficult to connect to other layers in a package. Additionally, the use of solder as an interconnection layer cannot be directly applied to PCD films. So an additional layer has to be applied on the polycrystalline diamond surface (very thin layer) in order to smooth the surface. This layer is usually a material that possesses a high thermal conductivity. Its purpose is to fill in the cracks on the PCD surface and increase the effective contact surface area.

Bibliography for Chapter 2

[1] Mitsubishi HVIGBT Module (Model Number: CM1800HC-34N) Datasheet, Revision 4. *Mitsubishi Electric.* Jul. 2005. https://www.mitsubishielectric-mesh.com/products/pdf/cm1800hc-34n_e.pdf.

[2] C. Azina, M.M. Wang, E. Feuillet, L. Constantin, B. Mortaigne, P.M. Geffroy, Y. F. Lu and J. F. Silvain, "Improved adhesion of polycrystalline diamond films on copper/carbon composite surfaces due to in situ formation of mechanical gripping sites," *Surface and Coatings Technology,* Vol. 321, p. 1-7, Jul. 2017.

[3] J. Amussen and D.K. Reinhard. "*Diamond Films Handbook.*" CRC Press Reference, 2002.

[4] B. Huang and D.K. Reinhard, "Electric field-dependent conductivity of polycrystalline diamond thin films," *American Institute of Physics*, Letter 59, 1991.

[5] M. Balakrishnan, M. R. Sweet and E. M. Narayanan, "Comparison of the thermal properties of polycrystalline diamond and aluminum nitride substrates," 2013 *Industrial Electronics Society Conference (IECON 2013)*, Vienna, Nov. 2013.

[6] M. Balakrishnan, M. R. Sweet and E. M. Narayanan, "Thermal Cycling Reliability of Polycrystalline Diamond and Aluminum Nitride Substrates," *International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM),* Ischia, Jun. 2014.

CHAPTER 3

HEAT TRANSFER ANALYSIS

3.1 Introduction

Thermal management by a power semiconductor device package is an essential component in the reliability of power semiconductor devices used in high power applications. Hence, this chapter's focus is on the terminology, characteristics, and model representations of heat transfer through a power semiconductor device package.

3.2 Characteristics of Heat Transfer

Heat transfer is the transference of heat from a place of high temperature to a place of low temperature. This thermal transport of heat can only occur by three possible mechanisms: conduction, convection, and radiation. Conduction is the movement (diffusion) of heat through a solid due to a temperature difference. While convection and radiation describe transmission of heat through fluid/air or electromagnetic radiation, respectively. For the purpose of this research, convection and radiation can be neglected due to the consideration of heat transfer solely within the package. As a result, heat conduction becomes the predominant heat transport mechanism for improvement of thermal management. Heat conduction through any solid can further be described by its two response states: steady-state and transient heat transfer.

3.2.1 Steady-State Heat Transfer

Once a system is exposed to a temperature differential, a temperature profile will emerge due to the transference of heat. At the beginning, this temperature profile changes with respect to distance and time. Eventually, the system will reach a point

where the heat entering and leaving becomes balanced. At this juncture, the temperature profile of the system stops changing; and the system has reached steady state. An example of steady-state heat transfer through a power semiconductor device package is illustrated in Figure 3.1 with the assumption that heat flows primarily in only one direction (x), from top to bottom.

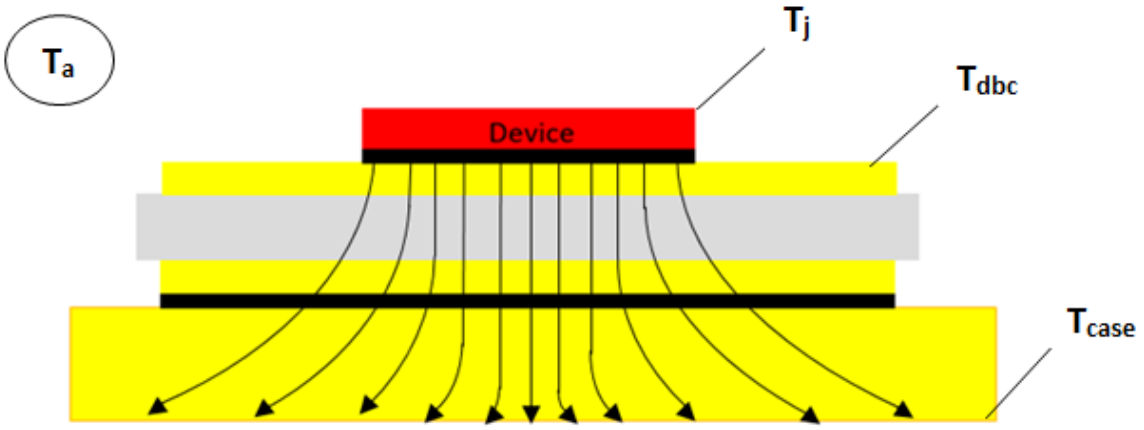

Figure 3.1. 1-D heat conduction through a power semiconductor device package (T_j: temperature of the device (junction temperature), T_{dbc}: temperature of top surface of DBC substrate, T_{case} or T_c: temperature at bottom of package, T_a: ambient temperature).

Steady-state heat transfer is an important component in the design process for determining the desired parameters, such as temperature, thermal resistance, and thermal capacitance, for each layer of a power semiconductor device package. Together, these parameters characterize heat flow within the package along with establishing maximum limits that it can tolerate. A general equation that relates some of these parameters to steady-state heat transfer can be seen in Equation 3.1. This equation, derived from Fourier's Law, relates the temperature difference between two surfaces, heat flux, length, and surface area. In this equation, q represents the heat flux, k is the thermal conductivity, A is the surface area, $\frac{dT}{dx}$ is the temperature gradient, T_A and T_B represent temperatures on opposing sides, and L is the length. The negative sign in this equation is related to the direction of heat transfer.

$$q = -kA\frac{dT}{dx} = \frac{-kA(T_A - T_B)}{L} \tag{3.1}$$

Thermal resistance is the parameter to focus on due to its significant effect on thermal management. This parameter essentially describes the resistance of a material to the flow of heat energy. Maintaining quality thermal management in a package is accomplished by providing as low a thermal resistance for each layer as is possible. Depending on what is being calculated, there are different forms of thermal resistance that exist based on the layers of interest. From Figure 3.1, the junction temperature can be determined from various points on the package, such as junction-to-ambient (*Rj-a*) and junction-to-case (*Rj-c*).

There is a method for calculating thermal resistance along with a layer's thermal capacitance. Thermal capacitance is a function of the temperature rise associated with a given quantity of applied energy [1]. It measures the capability of a material to accumulate heat. Both the thermal resistance and capacitance can be calculated based on the material properties and associated physical dimensions. The approximation of these quantities can be seen in Equations 3.2 and 3.3. In Equation 3.2, the thermal resistance is derived from Fourier's Law of heat conduction equation. While in Equation 3.3, thermal capacitance depends on heat dissipation and the temperature increase during a specified time period (*t*). Based on these equations, the selection of material and dimensions for the package plays a critical role in successful thermal management.

$$R_{thermal} = \frac{T_A - T_B}{q} = \frac{L}{kA} \tag{3.2}$$

$$C_{thermal} = \frac{qt}{T_A - T_B} \tag{3.3}$$

3.2.2 Transient Heat Transfer

Studying the transient effects of heat transfer is also imperative. Represented in Equation 3.4 and 3.5 are the respective time constant (τ_i) and the temperature profile of an equivalent thermal RC network ($T_{AB}(t)$), due to thermal resistance and capacitance for all material layers of a package (i layers). In Equation 3.4, R_i and C_i are the thermal resistance and capacitance of a defined layer. In Equation 3.5, power dissipation is represented as $P_{D,}$ period of time as t, and $T_A(t)$ and $T_B(t)$ are the transient temperatures of the opposing sides.

$$\tau_i = R_i C_i \tag{3.4}$$

$$T_{AB}(t) = (T_A(t) - T_B(t)) = R_i P_D (1 - e^{(-t/\tau_i)}) \tag{3.5}$$

A parameter often used to represent the transient behavior of a power semiconductor device and its package is determined by calculating the transient thermal impedance ($Z_{th(j\text{-}x)}$). Transient thermal impedance is the thermal analog to a driving point impedance for electrical circuits. The thermal impedance depends upon the thermal resistance and heat capacity of the materials in the system under study. The thermal impedance measures the time evolution of temperature from the location of the heat source (semiconductor die) to an external point on the case surface (at the interface where a heat sink would be attached). An equation for $Z_{th(j\text{-}x)}$ is shown in Equation 3.6, where $T_{j,peak}$ is the maximum junction temperature allowed; and T_x is any temperature spot selected on the package below the junction temperature.

$$Z_{th(j-x)} = \frac{\Delta T_{max}}{P_D} = \frac{(T_{j,peak} - T_x)}{P_D} \tag{3.6}$$

This $Z_{th(j-x)}$ parameter can be visualized in a transient thermal impedance curve, as seen in Figure 3.2. These graphs typically have numerous curves related to the different heat power pulse levels that are input. Generally, the y-axis for these types of graphs displays the $Z_{th(j-x)}$ values while the x-axis displays the time duration of a rectangular pulse of input power (heat). Therefore, based on the amount of power dissipated (P_D) and the desired location on the package to determine the associated $Z_{th(j-x)}$ and T_x, a calculation of the peak junction temperature ($T_{j,peak}$) can be determined for any period of time, as seen in Equation 3.7.

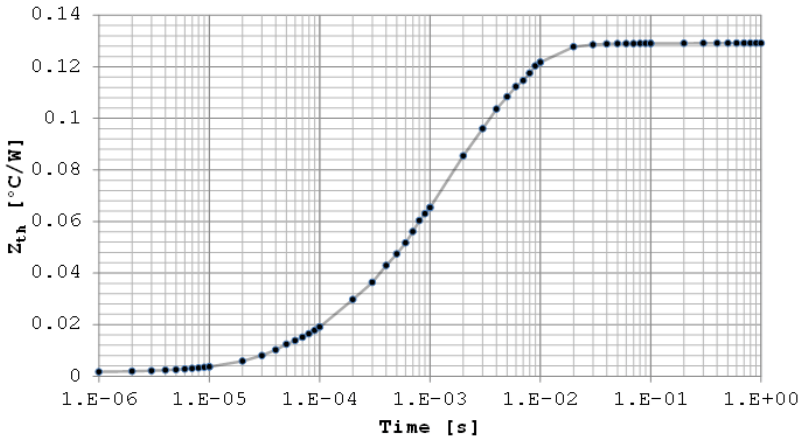

Figure 3.2. Example of transient thermal impedance curve experienced by a device package [2].

$$T_{j,peak} = Z_{th(j-x)}P_D + T_x \tag{3.7}$$

3.3 Equivalent Thermal Resistor-Capacitor (RC) Circuits

To model the thermal behavior in one dimension, the R_i and C_i of a package can be configured as an electrical circuit. Figure 3.3 demonstrates the similarities between variables of the electrical domain (voltage, current) to the thermal domain (temperature, heat).

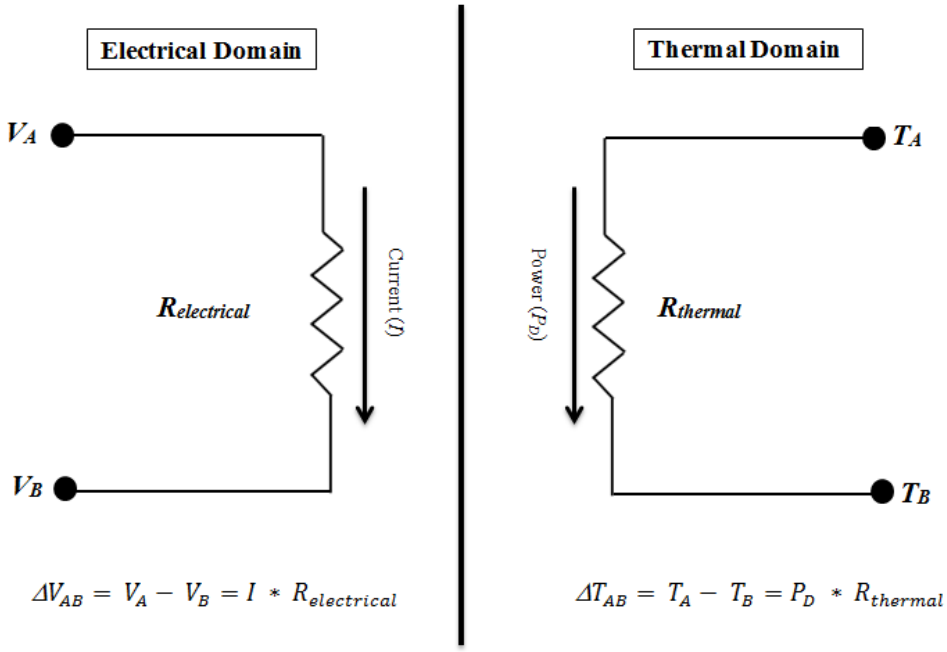

Figure 3.3. Fundamental relationships in electrical and thermal domains.

There are two different methods for modeling thermal behavior as an electrical circuit. Equivalent thermal RC circuits are represented as either a Foster or a Cauer network topology. Each of these thermal topologies has its own associated set of advantages and disadvantages. The Foster model consists of an electrical circuit that shows only the behavioral characteristics of a package design. Each layer of the package in this model is represented by parallel combination of thermal resistances (R_i) and capacitances (C_i), where i represents each material layer of a package. A schematic of the Foster-equivalent RC thermal network is depicted in Figure 3.4. The use of a fourth order network is typical for the power semiconductor industry.

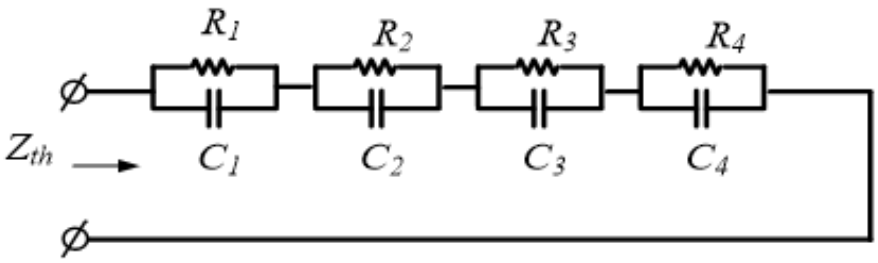

Figure 3.4. Foster-equivalent RC thermal network.

To calculate the RC elements of this thermal network, a curve fitting approach is applied to the experimental thermal impedance data that results in a sum of exponential terms [3]. The equation for this 4th order impedance is given in Equation 3.8, and is a least squares fit to experimental data. In this equation, $Z_{th(j\text{-}c)}$ is the transient thermal impedance for the junction-to-case region (standard region utilized), n is the number of package layers, and R_i and τ_i are the thermal resistance and corresponding time constant of each layer. Figure 3.5 displays this approach by displaying different experimental $Zth_{(j\text{-}c)}$ curves based on collection of R_i and C_i values.

The Foster RC components do not correlate directly with the physical parameters of a package's materials or geometry. As a result, the physical interpretation of where the heat flows and the time evolution of heat propagation through the package are not available.

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i[1 - e^{(-t/\tau_i)}] \tag{3.8}$$

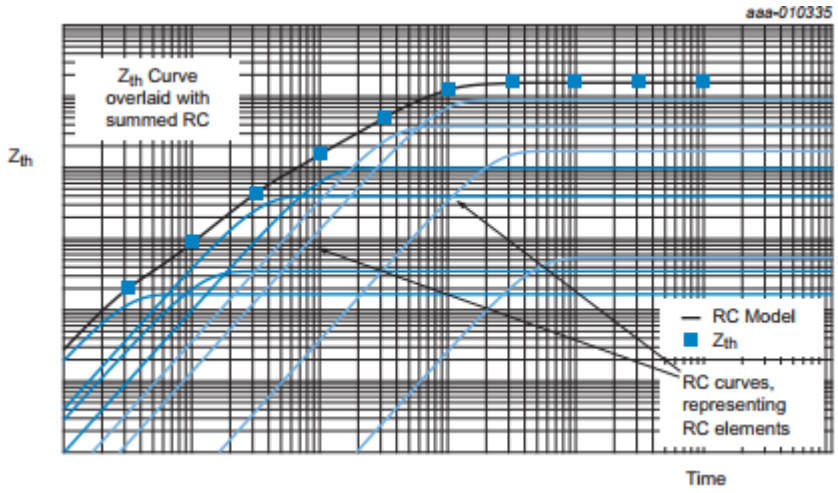

Figure 3.5: Different transient thermal impedance curves based on Ri and Ci values [4].

For this reason, a different model (topology) is desired. The Cauer topology more closely fits the geometric distribution of materials in a typical package. In this model, the RC elements are assigned for each material layer of the package. Hence, the entire package structure can be geometrically represented by the electrical circuit as shown in Figure 3.6.

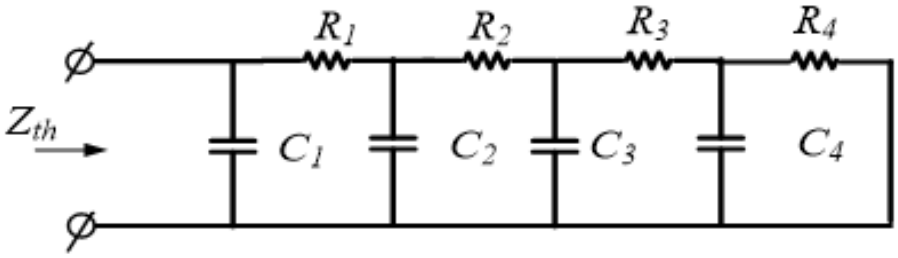

Figure 3.6: Cauer RC thermal network.

The calculation of the thermal resistance and capacitance for each layer in the Cauer thermal network can be obtained in Equations 3.9 and 3.10 respectively. In Equation 3.9, the thermal resistance is defined by the layer thickness (d_i), the effective cross-sectional surface area (A_{hi}), and the thermal conductivity (k_i) of each layer.

Computation of an effective cross-sectional surface area can be done using FEA analysis. Approximations can also be derived to avoid the complexity of FEA analysis.

A first-order approximation can be used for heat spreading through each layer based on an estimated spreading angle of 45° from a vertical center axis (originating at the heat source) for conductors and 0° for insulators. With this approximation, adequate results are obtainable and the complicated FEA analysis can be avoided. In addition, thermal conductivity is not a constant parameter and fluctuates in materials based on temperature. Generally, the temperature range experienced by a power semiconductor device package ranges from 25-400 °C. This temperature span creates little variation of thermal conductivities in the materials of a package structure [5]. Therefore, the thermal conductivities for each material can be assumed constant.

$$R_i = \frac{d_i}{k_i A_{hi}} \tag{3.9}$$

$$C_i = c_i \rho_i V_{hi} \tag{3.10}$$

In Equation 3.10, the thermal capacitance is calculated based on the specific heat capacity (c_i), the mass density (p_i), and its effective volume (V_{hi}) for each layer. The effective volume is a component of the effective cross-sectional surface area (A_{hi}) multiplied by the layer thickness (d_i). Similarly with thermal conductivity, the specific heat capacity and density are assumed constant even with temperature changes within the package.

Furthermore, the use of the Cauer model allows a heat sink to be attached to a power semiconductor device package for calculation purposes as well. If a heatsink were attached to a power semiconductor device package, the thermal resistance can be obtained based on convective heat transfer. Equation 3.11 represents this thermal

resistance based on thermal exchange between heat sink and surrounding environment (air). Typically, this is a nonlinear resistance because the convection heat transfer is a combination of natural and forced convection, which are nonlinear functions of temperature difference [3]. Therefore, the heat sink's thermal resistance is denoted by its surface area exposed to air (A_{hi}) and the convective heat transfer coefficient (h).

$$R_{hs} = \frac{1}{hA_{hi}} \tag{3.11}$$

No matter which thermal network is chosen, the thermal behavior of a power semiconductor device package allows for calculation of the junction temperature (T_j) and other temperatures in various material layers (T_{dbc}, T_{sol}, T_{bp}, and T_c). Where T_{sol} is the temperature at the top of the solder layer and T_{bp} is the temperature at the top of the baseplate.

Bibliography for Chapter 3

[1] "*Basic Principles of Thermal Analysis for Semiconductor Systems*." Free Scale Semiconductor Inc., 2008. Free Scale. Web. https://cache.freescale.com/files/analog/doc/white_paper/BasicThermalWP.pdf

[2] G. Petrone, C. Barbagallo and M. Scionti, "Thermo-Mechanical Analysis and Fatigue Life Prediction for an Electronic Surface-Mounted Device (SMD)," *COSMOL Conference*, Oct. 2015.

[3] Gachovska, Tanya, et al. "Transient Electro-Thermal Modeling of Bipolar Semiconductor Devices." Morgan & Claypool Publishers, 2013.

[4] "*AN11261 Using RC Thermal Models.*" NXP Semiconductors, 2014. Web. https://assets.nexperia.com/documents/application-note/AN11261.pdf

[5] R. Wu, H. Wang, K. Ma, P. Ghimire, F. Iannuzzo and F. Blaabjerg, "A temperature-dependent thermal model of IGBT modules suitable for circuit-level simulations," *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, pp. 2901-2908, Nov. 2014.

CHAPTER 4

EXPERIMENTAL SETUP FOR THERMAL MEASUREMENTS

4.1 Introduction

An experiment was executed to verify that the use of PCD films as a replacement for the DBC substrate in power semiconductor device packages would improve thermal performance. This experiment involved using a hot plate as the heat source and two different temperature measurement devices to accurately capture and record the time evolution of the top surface temperatures of the Powerex package and the PCD films as they increased above room temperature to the steady-state temperature of the hot plate. The temperature measurement devices used in the experiment were a thermal (infrared (IR) imaging) camera and a thermocouple. Each of these provides a different approach to measuring the temperature of a surface over time, and each has its own experimental setup and procedures that will be described thoroughly in the following sections.

4.2 Experimental Setup and Procedure

The basis of this experiment is to apply a uniform heat source to both package material systems and compare the heat conduction properties. A comparison was made of the distinct temperature profiles of the top surface for both systems. The heat source selected is a Thermo Scientific™ Super-Nuova™ Multi-Position Digital Stirring Hot Plate (Model SP135935) which provides the necessary temperature range to accommodate the testing requirements. This hot plate was used to apply heat to the bottom surface of the test parts.

Some of the specifications for the hot plate are provided in Table 4.1. There are two issues that arise with this hot plate: the inaccuracy in the temperature across its surface and fluctuation of the temperature. The accuracy of the hot plate can be ± 10 °C off from the digital setting established by the user at any one spot on the hot plate. Therefore, the temperature of the hot plate varies at different locations across the surface. Additionally, the hot plate fluctuates at ±2 °C periodically throughout a trial.

Table 4.1. Heating specifications for the Thermo Scientific hot plate [1].

Features	**Measurements**
Temperature Range	1 °C – 370 °C (34 °F – 698 °F)
Heat-Up Time to Within 5 °C of Maximum Temperature (Unloaded Top Plate)	8 Minutes
Accuracy of Temperature Display v. Actual Average Temperature of a 2 in. Diameter at Center of Top Plate	± 10.0 °C
Temperature Stability at Center of Top Plate Surface	± 2.0 °C

Figure 4.1 shows the hot plate and corresponding experimental test pieces (center of photo). The hot plate was turned on and set to the appropriate temperature. When the hot plate stabilized at the set temperature, the test pieces were placed on the hot plate surface using pliers or tweezers. Placement of the test pieces on the same location of the hot plate surface helped to mitigate variations from one test to another, as seen in Figure 4.2. The experiments were performed in a room with minimal air flow. The surfaces of all of the test parts were as smooth and polished as possible to accommodate good surface contact between the test parts and the hot plate.

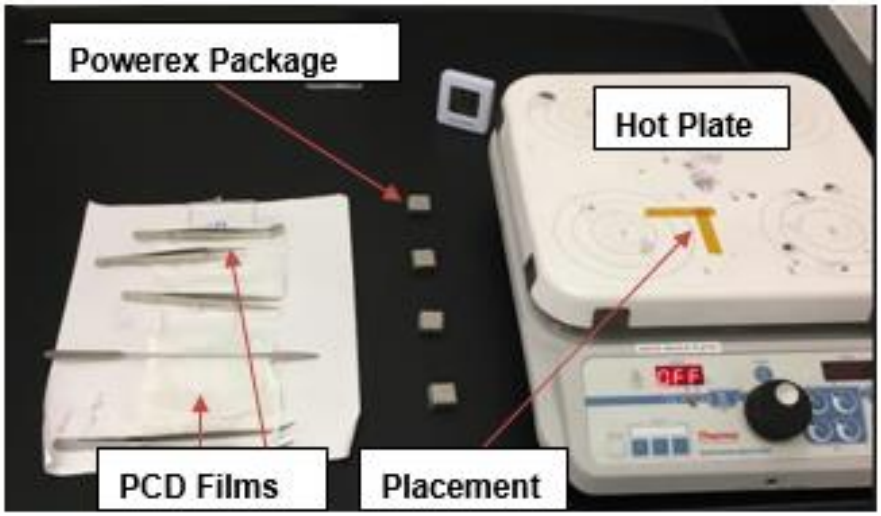

Figure 4.1. Hot plate and test pieces used for the heating experiment.

After placement of the test piece, a temperature measurement device was used to monitor the change in temperature of the top surface until a steady-state temperature was reached.

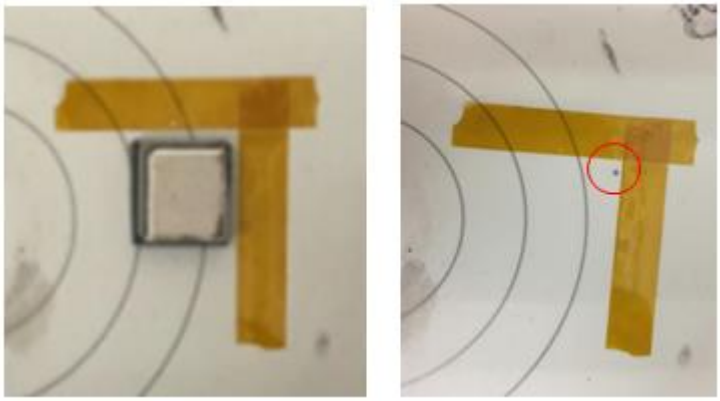

Figure 4.2. Placement of DBC test piece (left) and the PCD test pieces (right, inside circle).

For the experimental procedure, the specific hot plate temperatures selected for each of the package designs are provided in Table 4.2. The reason different temperatures were used is that the test pieces were significantly different in size and density.

Table 4.2. Hot plate temperatures used for package designs.

Package Designs	Temperature Setting
Powerex	150 °C and 200 °C
Co-PCD	75 °C and 100 °C
Cu-PCD	75 °C and 100 °C

4.3 Measurement of the Top Surface Temperature Profile

Once a test piece was placed on the hot plate, a thermal camera and thermocouples were used together to determine the temperature profiles of these material systems. The absolute temperature reading from the camera required calibration of its settings. The thermocouples helped to ensure values of the temperature were known.

4.3.1 Thermal (IR) Imaging Camera Measurement

4.3.1.1 Background

A thermal imaging camera measures the temperature of a surface by reading the amount of infrared radiation that is emitted from an object. The general temperature measurement using this type of camera calculates the apparent temperature (T_{obj}) of an object based on three incoming radiation power terms: emission from the object (W_{obj}), reflected emission from ambient sources (W_{refl}), and emission from the atmosphere (W_{atm}). Based on the emissivity (ε) and the transmittance (τ) for each of these terms, a thermal imaging camera can calculate the approximate apparent temperature of a surface. A schematic representation of this measurement formula is shown in Figure 4.3.

Thermal imaging cameras of the type used, possess a wide temperature range, low thermal sensitivity, high temperature resolution, and fast frame rate capability, all of which made it very useful in this application. In particular, the fast frame rate and low

thermal sensitivity were essential for measuring the temperature of the smaller PCD films. The camera selected for this experiment was the FLIR E60 which has the ability to take both thermal (IR) images and videos. In addition, the FLIR E60 was integrated with FLIR software for enhanced analysis of the collected temperature data. The full list of specifications for the FLIR E60 camera are provided in Table 4.3.

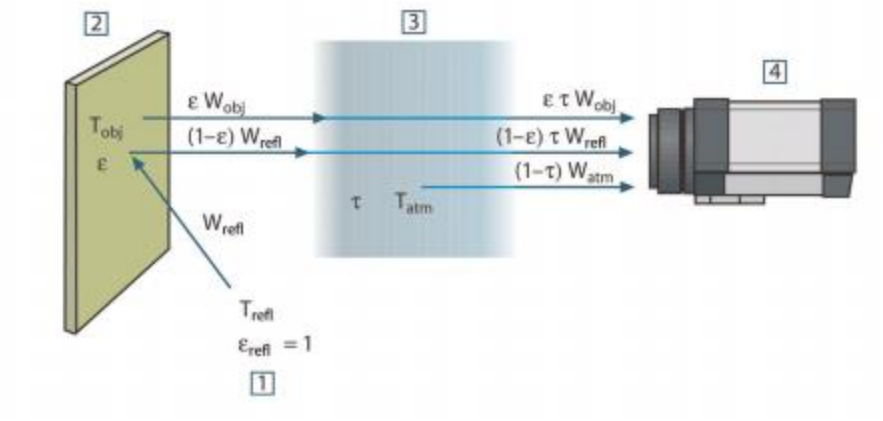

Figure 4.3. Schematic representation of measurement formula (1 = surroundings, 2 = object, 3 = atmosphere, 4 = camera) [2].

Table 4.3. Specifications for FLIR E60 thermal (IR) imaging camera [3].

Features	Measurements
Temperature Range	-20 °C to 650 °C (-4 °F to 1202 °F)
Thermal Sensitivity (Noise Equivalent Temperature Difference (NETD))	<0.05 at 30 °C
Measurement Accuracy	±2 °C or ±2% of reading
Spectral Range	7.5 to 13 µm
Frame Rate	60 Hz

4.3.1.2 Experimental Setup and Camera Settings

The experimental setup of the hot plate and the thermal imaging camera is shown in Figure 4.4. The camera captured the full transient temperature profile of the DBC and

PCD test pieces by recording a video. In order to obtain accurate temperature readings, several parameters and settings were considered. For instance, the height, angle, and focus of the camera with respect to the hot plate all have an effect on the output temperature. Specifically, the height and angle should be far enough away from the hot plate to avoid hot plate radiation while the object of interest should be in focus to create a clear thermal image. For a proper temperature measurement, the desired height should be at least six inches away from the hot plate; and the angle, with respect to horizontal, should be around 45°.

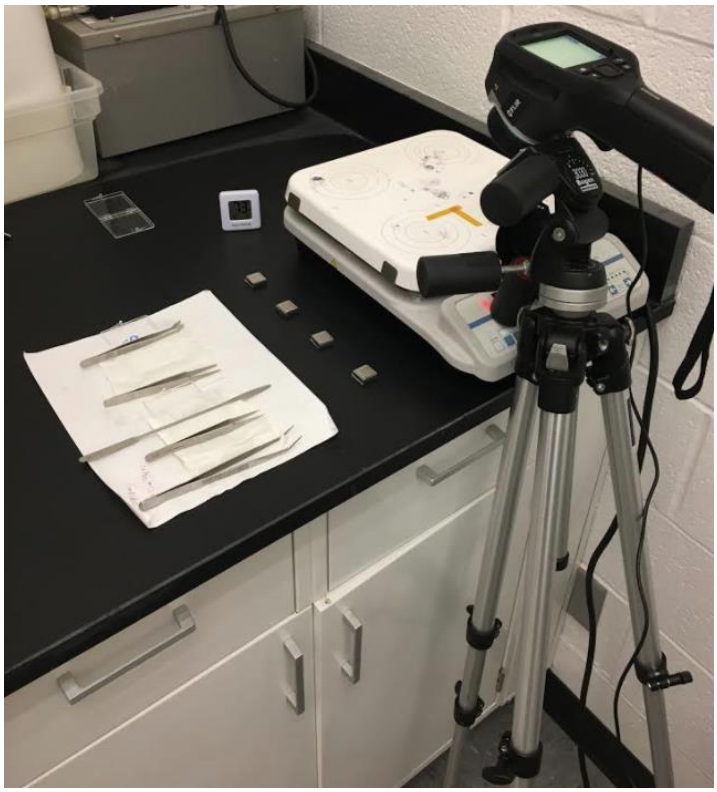

Figure 4.4. Thermal (IR) imaging camera experimental setup.

The camera's settings of atmospheric temperature (T_{atm}), reflective temperature (T_{refl}), and emissivity (ε) are critical. As mentioned earlier, each of these parameter settings directly impacts the resulting measurement used by the camera to calculate the

apparent temperature. Atmospheric temperature represents the temperature of the surrounding atmosphere. This setting was determined by using an AcuRite® Digital Indoor Thermometer (Model 00307W) to capture the exact room temperature between the camera and the target object. The reflective temperature compensates for the radiation that is reflected from the target object. This setting becomes crucial if the target object has a low emissivity and appears to be reflective, like most metals. The reflective temperature was measured by the reflector method, as shown in Figure 4.5. In this figure, there is a picture of the experimental setup on the left and a thermal image of the aluminum foil on the right. This method consists of placing a sheet of crumpled aluminum foil in front of the target. Aluminum has an immensely low emissivity of 0.02 and is extremely reflective, making it the most effective material to measure reflective temperature. The emissivity of the FLIR E60 camera was set to 1.00, and the distance away from the object was set to 0 ft. The average temperature over a large area of the aluminum foil was measured to determine an average reflective temperature.

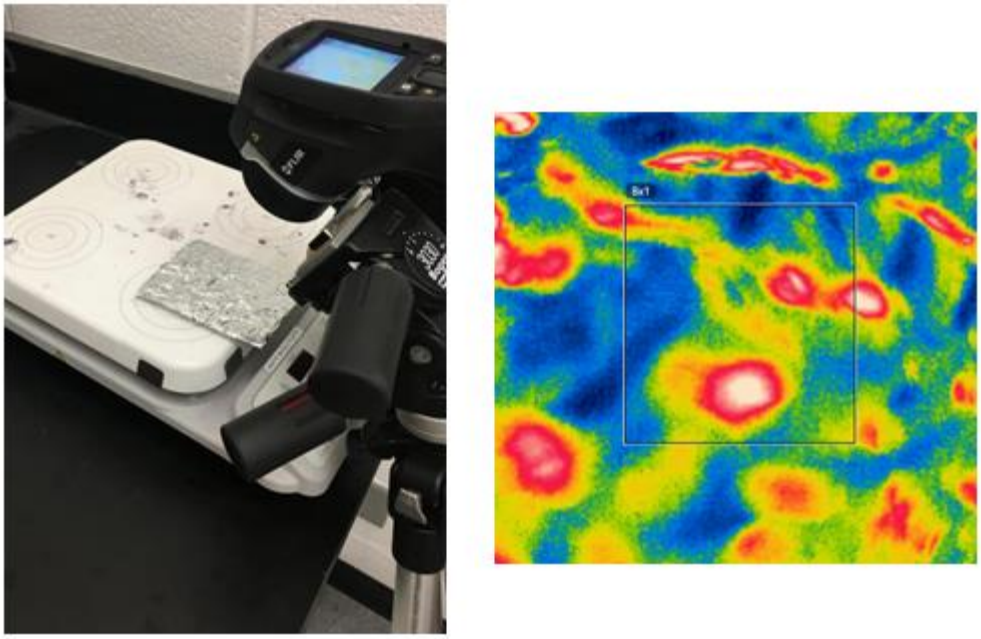

Figure 4.5. Reflector method for measuring of the reflective temperature setting.

The final camera setting of importance is emissivity. Emissivity is the measure of how much radiation is emitted from an object compared to that from a perfect blackbody of the same temperature. The value of emissivity ranges from 0 to 1 with a low emissivity setting corresponding to highly reflective materials, such as most metals, and a high emissivity setting corresponding to low reflective materials. This setting is critical due to the camera's inability to detect emissivity of objects to calculate the true temperature. These cameras can only calculate the "apparent temperature" of objects, which means that this temperature is computed as a function of both temperature and emissivity [4].

In addition, there is a different value of emissivity for every material. Therefore, when measuring an object's temperature with multiple materials, the emissivity will be different for each material in the image. This correlates to the Powerex test piece that resulted in approximately four emissivity values that were needed for the correct

temperature to be computed at each layer. The PCD films consisted of a PCD substrate coated with either cobalt or copper. The thickness of these coated layers was relatively small, in the nanometer range. For this reason, the coated layers were neglected. The emissivity of PCD is relatively unknown, with very few studies published. Generally, the emissivity of diamond is related to its quality and fabrication process. As a result, PCD maintains a high emissivity value in most cases. According to [5-8], the ranges of emissivity for materials used in the Powerex piece and PCD are shown in Table 4.4.

Table 4.4. Emissivity values for Powerex package and PCD films.

Experimental Package Designs	Material Layers	Emissivity
Powerex piece	Cu	0.77−0.87
	AlN	0.86−0.96
	AlSiC MMC	0.83−0.96
PCD Films	PCD	0.63, 0.85−0.95

Emissivities are sensitive to temperature variations and, thus, time during the transient measurements. Therefore, an approach was used to determine the behavior of emissivity vs. time. This approach utilized small thermocouples to properly measure the true temperature of the surface. This true temperature value was then used to calibrate the emissivity values to correctly portray the temperature profiles measured by the FLIR E60.

4.3.1.3 Experimental Procedure

The atmospheric temperature, reflective temperature, and emissivity values for the camera were set to the desired values, as shown in Table 4.5. The atmospheric and reflective temperatures were determined by experimentation with the hot plate temperature. The emissivity was set to the default value of 0.95 for the Powerex part,

while several emissivity values were used for the PCD films due to the small size of the PCD films compared to the thermocouples. The size of these thermocouple sensors can negatively impact the true temperature measurement of the PCD films and cause inaccuracies in the readings. Additionally, PCD has a high emissivity value that will generate small temperature variations when recorded by the camera. Once the emissivity value is above 0.85, the measured temperature marginally changes if the emissivity is increased further. Under these circumstances, the PCD films were only represented by a range of emissivity values, represented earlier in Table 4.4.

Table 4.5. FLIR E60 camera parameter settings used in heating experiment for both package designs.

Camera Settings	**Powerex Package**		**PCD Films**	
Hot Plate Temperature	150 °C	200 °C	75 °C	100 °C
Emissivity	0.95	0.95	0.63, 0.85–0.95	0.63, 0.85–0.95
Reflective Temperature	76.0 °F	76.0 °F	76.0 °F	76.0 °F
Distance from Camera	0.5 ft	0.5 ft	0.5 ft	0.5 ft
Atmospheric Temperature	95.3 °F	108.7 °F	84.0 °F	87.5 °F

The Powerex part was tested at hot plate temperatures of 150 °C and 200 °C, whereas the PCD films were measured at lower temperatures of 75 °C and 100 °C. The placement of the each package design on the hot plate and spot targets can be seen in Figure 4.6, as a thermal image from the FLIR E60. For the Powerex part, four pieces of similar design were tested at the stated hot plate temperatures of 150 °C and 200 °C for 30 minutes and 25 minutes, respectively. At the end of each trial, the results from the four module test parts were averaged together to get an appropriate representation of the top surface temperature over time. For the PCD films, one of each design (Co-PCD and Cu-PCD) was tested at two different hot plate temperatures for 2-minute cycles each.

Multiple trials were then executed for each package design to prove consistency with their temperature profiles. Data analysis from the multiple trials for each package design were analyzed and modified by utilizing FLIR Tools software. Individual trials were then averaged together to get a precise temperature profile for each package design. The top surface temperature profile for the Powerex part can be seen below in Figure 4.7.

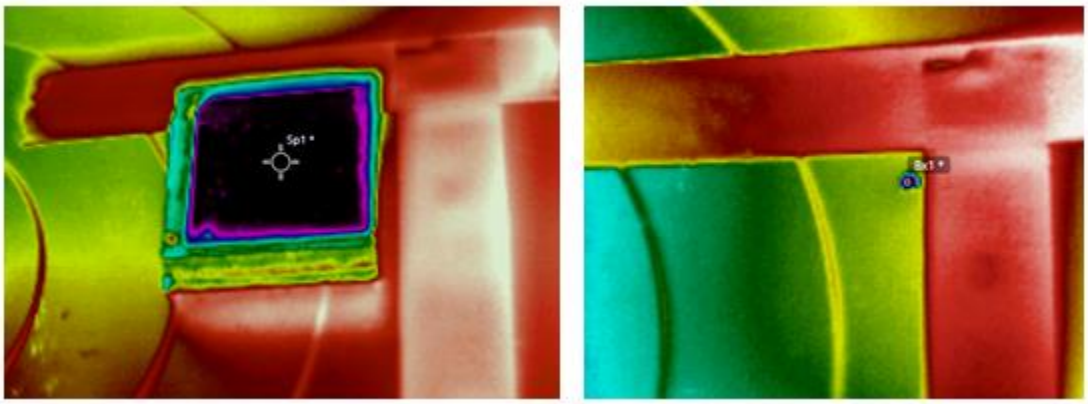

Figure 4.6. Thermal (IR) images of Powerex part (left) and PCD films (right).

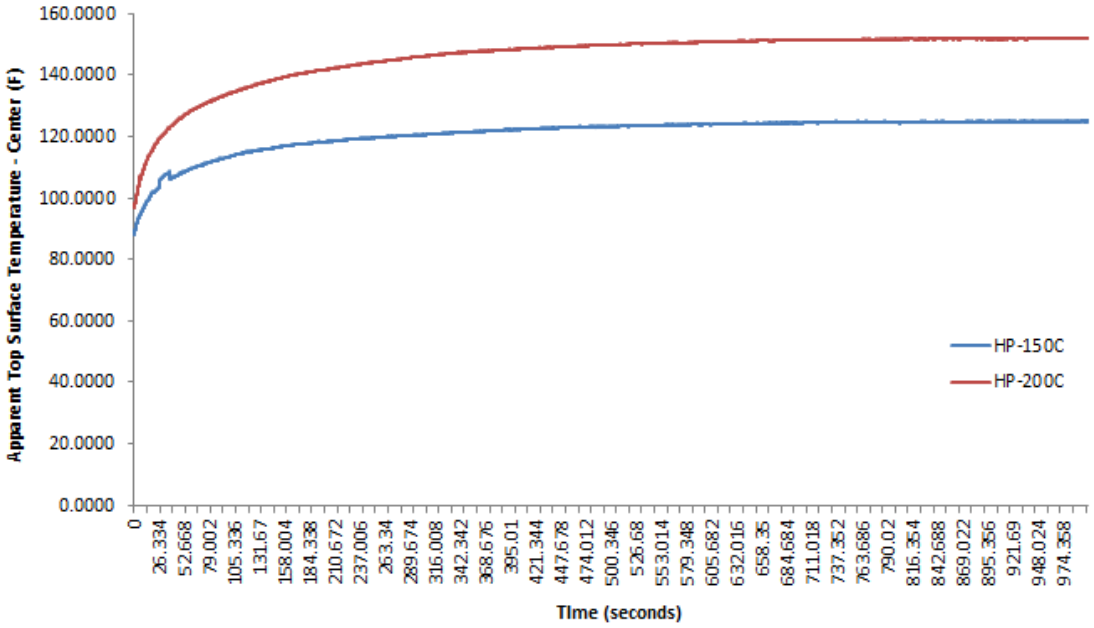

Figure 4.7. Thermal camera measurement of apparent top surface temperature profile of Powerex parts at hot plate temperatures of 150 °C and 200 °C.

4.3.2 Thermocouple Measurements

A digital thermometer, Model HH-23 Microprocessor Thermometer (Model LSI-120-821), was used to convert the voltage of each thermocouple to its equivalent temperature. The thermocouple selected for this work was a Type K (chromel-alumel). Table 4.6 shows the specifications for the digital thermometer using a Type K thermocouple.

Table 4.6. Specifications for digital thermometer with Type K thermocouple [9].

Features	Measurements
Temperature Range	-200 °C to 1372 °C (-328 °F to 2502 °F)
Temperature Resolution	0.1/1 °C or °F
Overall Accuracy	±(0.1% rdg + 0.6 °C /1.0 °F)

Each test part was connected to a thermocouple by Teflon™ tape as seen in Figure 4.8. Heating experiments were done as before with the thermal imaging camera to measure the temperature profile of the top surface.

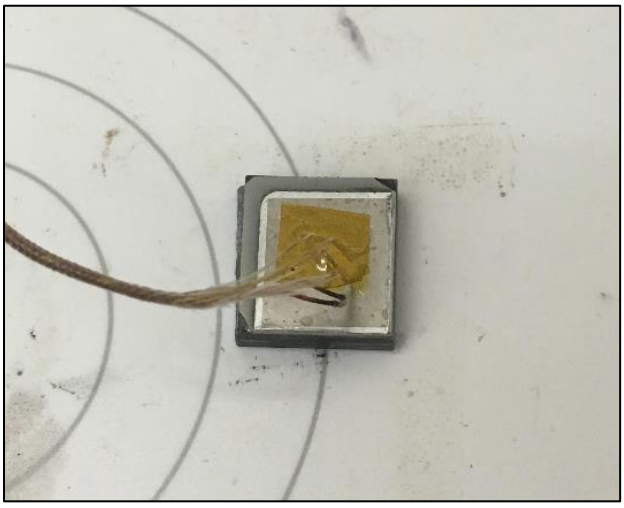

Figure 4.8. Interconnection of thermocouple sensor and top surface of Powerex package using Teflon tape.

The results from the thermocouple experiments on the Powerex parts are shown in Figure 4.9. These results were obtained by recording the initial rise time of the true surface temperature for the first 3 minutes every 10 seconds. After 3 minutes, the temperature data was recorded every 30 seconds. Multiple trials were completed and averaged together to create the true temperature profile for both hot plate temperatures of 150 °C and 200 °C. This temperature profile was then compared with the apparent temperature profile taken by the thermal imaging camera to approximate the emissivity values as they change with time.

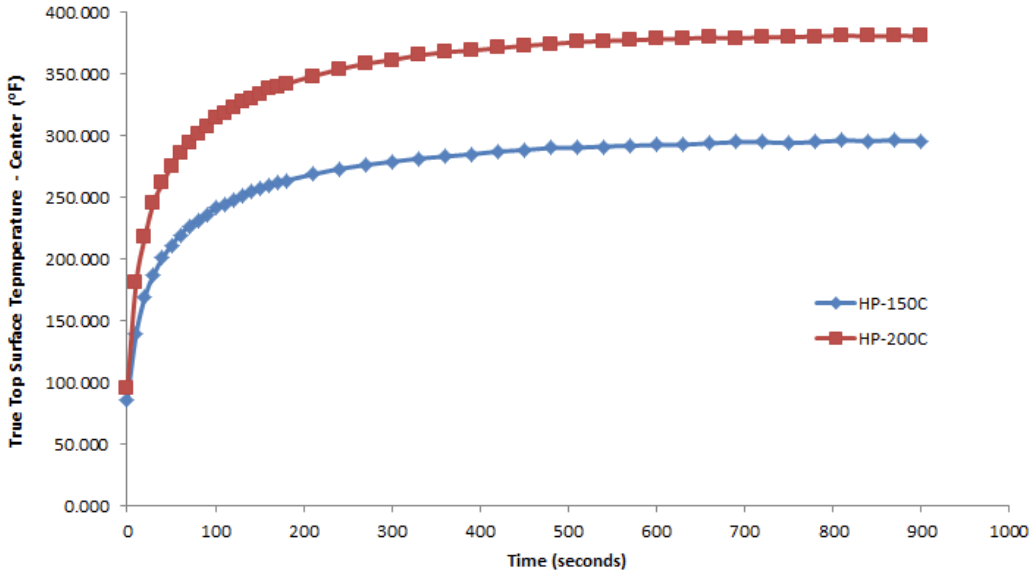

Figure 4.9. Digital thermometer measurement of true temperature profile of Powerex parts.

4.3.3 Emissivity Calibration of Thermal (IR) Imaging Camera

The FLIR E60 camera has the capability of integrating with the FLIR Tools software for in-depth analysis on thermal (IR) images and videos. This software was utilized to analyze videos of the apparent temperature profile from the camera and change the emissivity values accordingly. The emissivity values were adjusted at each data point taken from the thermocouple experiments until the apparent temperature, from Figure

4.7, matched the true temperature of the top surface. Table 4.7 displays the new emissivity values as they change with time (temperature) for the two hot plate temperatures. Note that the emissivity becomes constant after 3 minutes (small temperature changes arise). A plot of the data in Table 4.7 is provided in Figure 4.10.

Table 4.7. Adjusted emissivity values for thermal (IR) imaging camera over entire transient period.

Time (s)	HP-200C Emissivity	HP-150C Emissivity
0	0.95	0.95
1	0.74	0.82
2	0.61	0.61
3	0.52	0.52
4	0.45	0.44
5	0.40	0.38
6	0.36	0.36
7	0.33	0.32
8	0.30	0.31
9	0.28	0.28
10	0.26	0.26
20	0.22	0.20
30	0.19	0.19
40	0.18	0.18
50	0.18	0.17
60	0.17	0.16
70	0.17	0.16
80	0.17	0.16
90	0.16	0.16
100	0.16	0.16
110	0.16	0.16
120	0.16	0.15
130	0.16	0.15
140	0.16	0.15
150	0.16	0.15
160	0.16	0.15
170	0.16	0.15
180	0.16	0.15

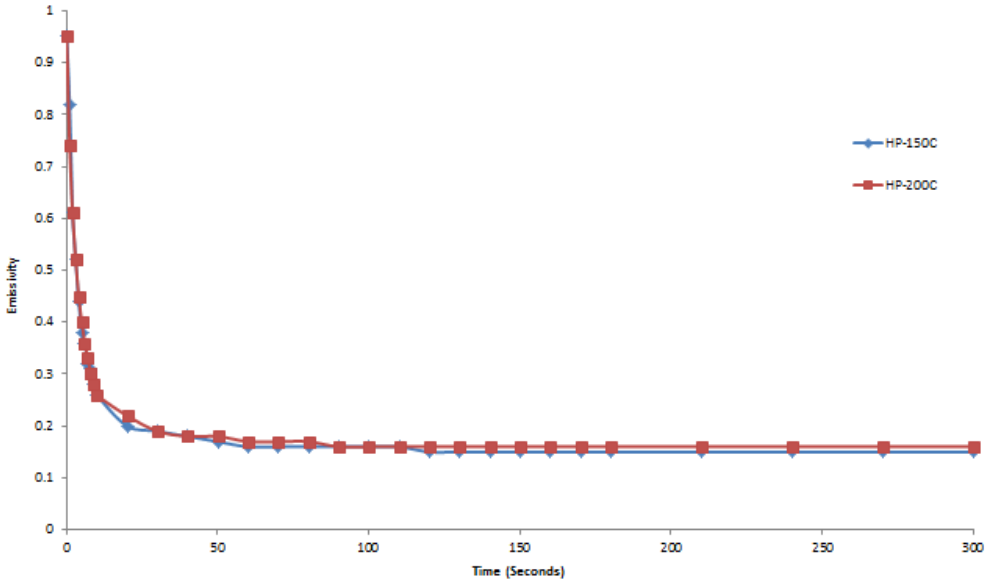

Figure 4.10. Top surface material behavior of emissivity v. time.

Knowing the emissivity changed as a function of time (temperature), the image data (Powerex parts) was recalibrated and plotted in Figures 4.11 and 4.12 for hot plate temperatures of 150 °C and 200 °C, respectively. Also shown in Figure 4.11 and Figure 4.12 are the outputs from the thermocouple measurements and the uncalibrated images (emissivity set to default value of 0.95). This emissivity-calibrated temperature profile now accurately represents the top surface temperature of the Powerex package over its entire transient period.

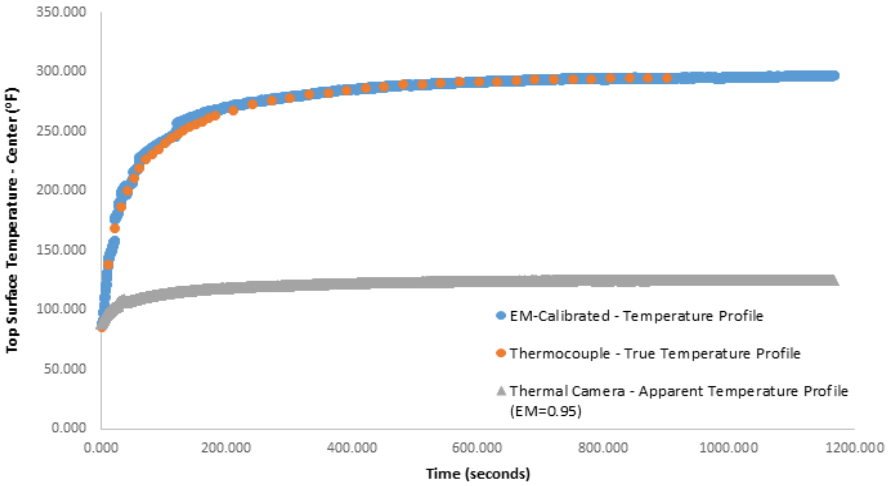

Figure 4.11. Comparison of top surface temperature profiles at hot plate temperature of 150 °C.

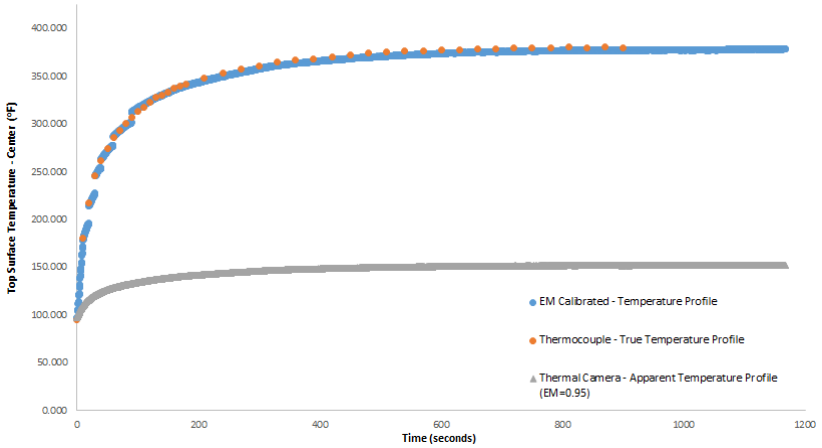

Figure 4.12. Comparison of top surface temperature profiles at hot plate temperature of 200 °C.

Bibliography for Chapter 4

[1] Thermo Scientific Super-Nuova Multi-Place Stirrer and Stirring Hot Plates Operation Manual and Part List Series 1359 and 1360. *ThermoFisher Scientific.* Apr.2010.https://assets.thermofisher.com/TFS-Assets/LED/manuals/D01663~.pdf.

[2] User's Manual FLIR Exx Series. *FLIR Systems, Inc.* 2013. http://m.markertek.com/Attachments/Manuals/Flir/E60-Manual.pdf.

[3] FLIR E-Series Datasheet. *FLIR Systems, Inc.* 2013. https://www.flir-direct.com/pdfs/cache/www.flir-direct.com/e60/datasheet/e60-datasheet.pdf.

[4] "Emissivity in the Infrared – Effects of Emissivity." *Optotherm Thermal Imaging.* 2018. https://www.optotherm.com/emiss-effects.htm.

[5] Table of Total Emissivity. *OMEGA Engineering, Inc*. 2018. https://www.omega.com/temperature/Z/pdf/z088-089.pdf.

[6] Table of Emissivity of Various Surfaces for Infrared Thermometry. *Mikron Instrument Company, Inc.* 2018. http://www.czlazio.com/tecnica/Tabella%20delle%20Emissivit%C3%A0.pdf.

[7] O. Riou, P. Logerais, V. Froger, J. Durastanti and A. Bouteville, "Thermal study of an aluminum nitride ceramic heater for spray CVD on glass substrates by quantitative thermography," *Quantitative Infrared Thermography Journal,* Vol. 10, No. 2, pp. 159-171, Sept. 2015.

[8] M. P. Seigal, T A. Friedmann, J.P. Sullivan, J. Mikkalson, F. Dominguez, "Diamond and Diamond-Like Carbon Films for Advanced Electronic Application," *Unlimited Release,* Mar. 1996.

[9] HH-21, HH-22 and HH-23 Handheld Microprocessor Digital Thermometer User's Guide. *OMEGA Engineering, Inc.* 1996. https://www.omega.com/manuals/manualpdf/M0739.pdf

CHAPTER 5

MODELING OF POWEREX PACKAGE

5.1 Introduction

The calibrated transient temperature behaviors of the Powerex package include the large thermal RC time constants of both the baseplate and solder layers. Hence, an appropriate equivalent thermal circuit was needed to correctly describe the effects of the baseplate and solder regions. Modification of the equivalent circuit could then be done to remove the baseplate and solder layers, leaving only the DBC section of the package for direct comparison to the PCD films.

5.2 Construction of Cauer-Equivalent RC Circuit

The modeling of the DBC layers commenced by creating a Foster-Equivalent RC circuit that reflected the transient behavior of the emissivity calibrated top surface temperature. This approach accurately computed the time constants required to characterize this temperature profile. From this circuit, a topology conversion was made from the Foster-equivalent RC circuit to a Cauer-equivalent RC circuit. The transformation between circuit topologies is necessary in order for the each material layer of the Powerex package to be physically represented by electrical components.

5.2.1 Foster-Equivalent RC Circuit

The creation of the Foster circuit begins by computing the necessary thermal resistors and capacitors based on applying an exponential fourth order fit using the Curve Fitting Tool in MATLAB. The equation implemented is shown in Equation 5.1, where $T_{dbc}(t)$ is the temperature profile at the top surface of the Powerex package, n is the

number of layers in the package, R_i is the thermal resistance for the i^{th} layer, τ_i is the time constant for the i^{th} layer, and t is the time duration of the experiment. This Curve Fitting Tool approximates eight coefficients (R_i and τ_i) that best embody the temperature profile of the top surface. Figure 5.1 and Figure 5.2 show the corresponding results for the fourth order exponential fits of the temperature data for each hot plate temperature.

$$T_{dbc}(t) = \sum_{i=1}^{n} R_{th,i}\left(1 - e^{-\frac{t}{\tau_i}}\right) \tag{5.1}$$

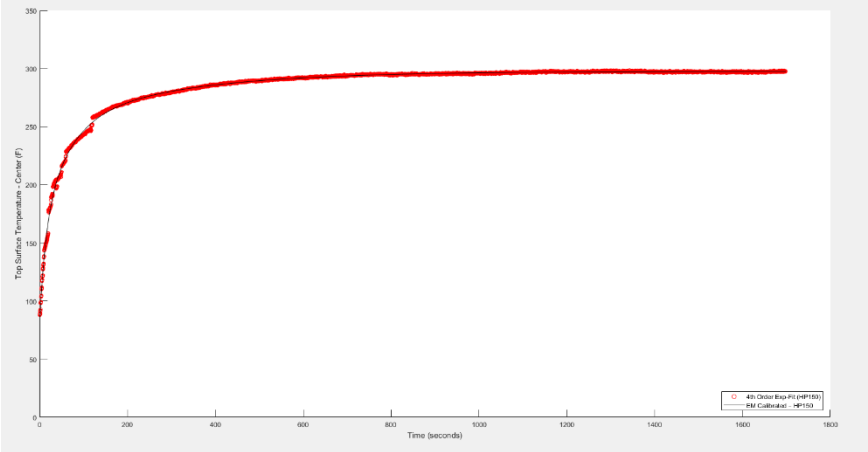

Figure 5.1. Fourth order exponential fit of transient surface temperature of Powerex package for a hot plate at 150 °C.

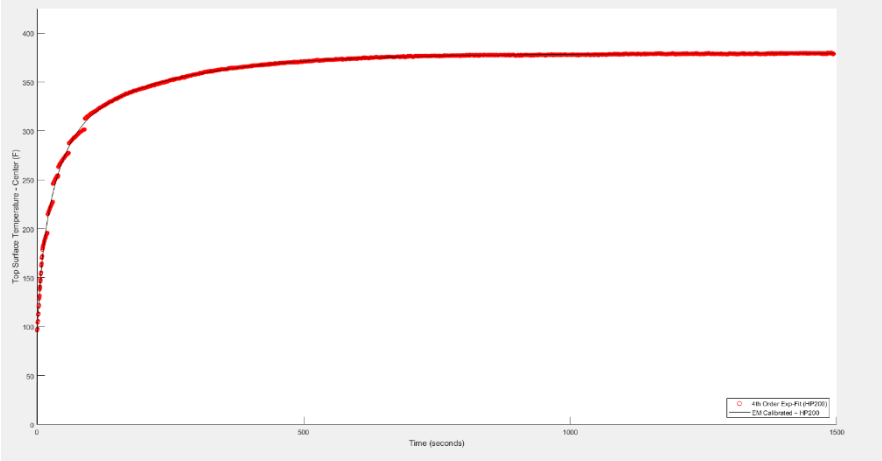

Figure 5.2. Fourth order exponential fit of transient surface temperature of Powerex package for a hot plate at 200 °C.

The eight coefficients for each temperature experiment are given below in Table 5.1. An electrical circuit representation of the fourth order Foster-Equivalent RC model is shown below in Figure 5.3. The two boundary conditions in this circuit are Q_{hp} and $T_{reference}$ which represent the heat dissipation and top copper layer temperature, respectively.

Table 5.1. Circuit parameters from fourth order exponential fit of the Foster RC circuit.

Circuit Parameters	**Powerex Parts (HP-150C)**	**Powerex Parts (HP-200C)**
Resistors (K/W)		
R_1	93.25	89.84
R_2	72.08	145.4
R_3	82.46	52.73
R_4	49.77	90.99
Time Constants (s)		
τ_1	57.76	0.00111
τ_2	12.97	35.6
τ_3	0.0007281	7.406
τ_4	274.2	203.8
Capacitors (J/K)		
C_1	0.61941	1.23553e-05
C_2	0.17994	0.24484
C_3	8.82973e-06	0.14045
C_4	5.50934	2.23981

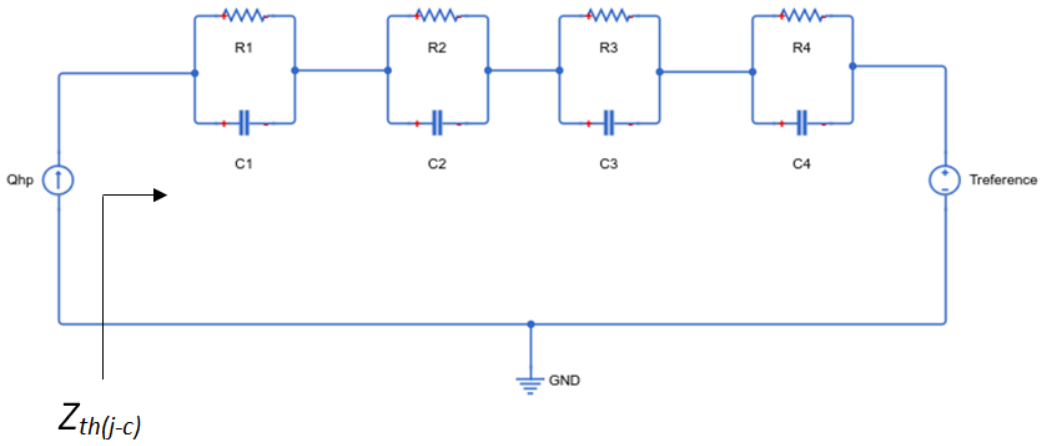

Figure 5.3. Electrical schematic of Foster-equivalent RC model.

5.2.2 Conversion from Foster to Cauer RC Circuit

The Foster-network is converted to a Cauer topology as described in [1] from pages 59-63 in Appendix A. The new thermal resistances and capacitances for the Cauer network are displayed in Table 5.2. The corresponding circuit is shown in Figure 5.4. Once more Q_{hp} and $T_{reference}$ represent heat dissipation and the top surface copper layer temperature respectively while $T_{ambient}$ serves as the room temperature (73 °F or 23 °C). This fourth order ladder network more closely represents the physical system of package materials in the Powerex package.

Table 5.2. Circuit components for Cauer RC circuit.

Circuit Parameters	Powerex Parts (HP-150C)	Powerex parts (HP-200C)
Resistors (K/W)		
$R_{1(CE)}$	82.4707	89.8654
$R_{2(CE)}$	118.2863	125.1081
$R_{3(CE)}$	69.6306	108.4042
$R_{4(CE)}$	27.1725	55.5823
Capacitors (J/K)		
$C_{1(CE)}$	8.8292e-06	1.2354e-05
$C_{2(CE)}$	0.1360	0.08926
$C_{3(CE)}$	0.7563	0.2456
$_{4(CE)}$	8.9231	3.2516

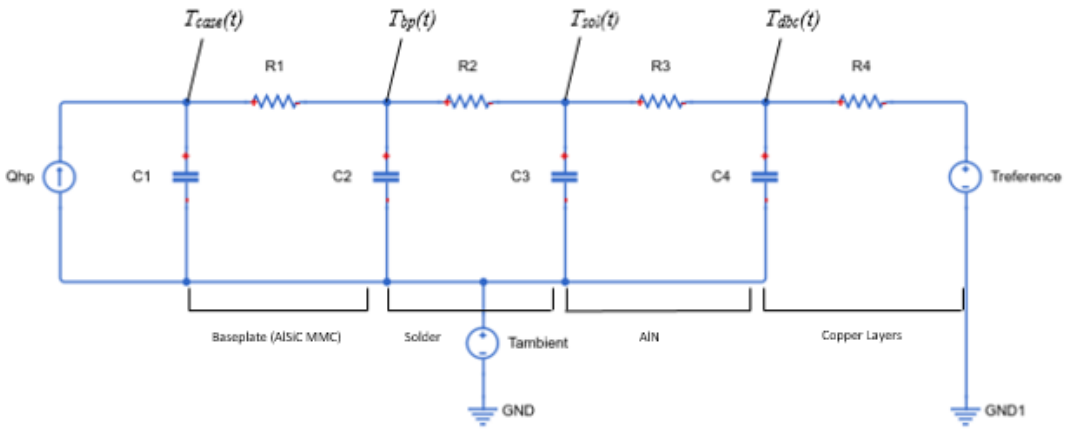

Figure 5.4. Electrical schematic of Cauer RC circuit.

5.3 Modification of Cauer RC Circuit

The Cauer circuit developed produced thermal resistors and capacitors that represent the material layers of the Powerex package. This circuit does not account for lateral heat spreading, constriction, and edge effects. In addition, the part from the Powerex package is asymmetric due to the way in which the test piece was acquired from the full module. Figure 5.5 shows the structure used in the testing and shows an area where the lateral effects, listed above, influence the thermal behavior from a purely one-dimensional description. In this figure, the arrows in the hot plate represent heat energy into the test piece.

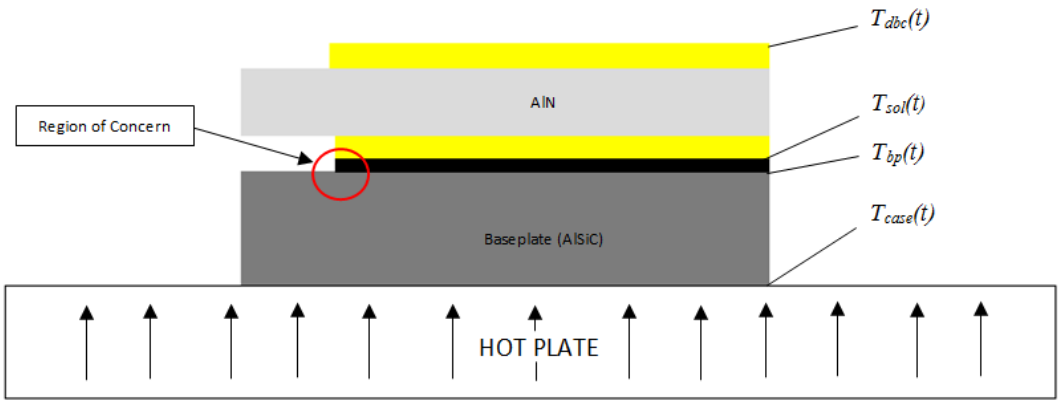

Figure 5.5. Schematic representation of thermal experiment with Powerex piece (Temperatures represented as function of time, $T_{dbc}(t)$: top surface temperature profile of Powerex package, $T_{bp}(t)$: temperature profile at top of baseplate, $T_{sol}(t)$: temperature profile at top of solder layer, and $T_{case}(t)$: temperature profile at bottom of Powerex package).

For a more direct comparison of performance to the PCD pieces, the DBC section of the Powerex piece must be isolated in the model (and associated test data). A similar Cauer thermal network, created from calculated parameters based on material properties

and geometries, is developed. This calculated network can provide insight into removal of the baseplate and solder sections, leaving only the DBC section.

5.3.1 Calculated Cauer RC Circuit

Each layer of the Powerex package was measured to ascertain its corresponding dimensions of length, width, and height. Typically, heat is generated from a small area (power semiconductor device) and spreads outward to the other layers that are dimensionally larger. In these experiments, however, the baseplate was heated first and was nearly the same size (surface area) as the other layers, thus the effect of heat spreading can be ignored.

The material properties, as given in Table 2.1, were used along with the geometric values to calculate the thermal resistance of each layer. The solder layer thickness was hard to determine without significantly better microscopy than was used. For this reason, it was challenging to distinguish a value of thermal resistance. A similar issue was related to the exact baseplate (MMC) and solder (PbSn) composition percentages, thus allowing only a range of thermal resistances to be estimated. Table 5.3 displays the resultant thermal resistance ranges for the solder layer and the baseplate.

Table 5.3. Variation of material properties for baseplate and solder layer.

Material	**Solder (PbSn)**	**Baseplate (AlSiC MMC)**
Thermal Conductivity (W/m**.**K)	35 – 66	120 – 205
Thickness (μm)	50 – 100	5000
Surface Area (m^2)	2.55e-04	3.145e-04
Thermal Resistance (K/W)	0.00297 – 0.0112	0.0776 – 0.133

For the purpose of the calculated Cauer network, the baseplate's thermal conductivity and the solder's thermal conductivity and thickness were approximated within their ranges based on the standard values used in other references. From [2-3], a baseplate thermal conductivity of 175 W/m*K and solder thermal conductivity of 50 W/m*K and thickness of 100 μm was selected. With all the parameters determined, Equation 3.9 was used to calculate the thermal resistance for each layer. Table 5.4 shows all the thermal resistance values for this particular circuit. The calculated Cauer RC circuit is topologically identical to the Cauer circuit shown in Figure 5.4.

Table 5.4. Thermal resistances of calculated Cauer RC circuit.

Thermal Resistances	Calculated Value (K/W)
$R_{1(CC)}$	0.09085
$R_{2(CC)}$	0.00784
$R_{3(CC)}$	0.01383
$R_{4(CC)}$	0.00489

5.3.2 Comparison between Measured and Calculated Cauer RC Thermal Networks

Further analysis comparing the measured and calculated elements of the thermal networks demonstrated that additional modifications were necessary. Table 5.5 displays the steady state simulation results for the experimental and calculated networks. The corresponding circuit utilized is depicted in Figure 5.6. Each of the circuit components were implemented into the simulation from values listed in Table 5.2 and 5.4 for experimental and calculated networks, respectively. The boundary conditions of Q_{hp} and $T_{reference}$ for each network were estimated to get the desired temperature at the top surface (T_{dbc}) to match the results from the thermal experiment and to match the known hot plate temperature.

Table 5.5. Initial steady state comparison of both Cauer circuits (CE and CC).

Measurements	HP-150C Analysis		HP-200C Analysis	
	Exp. (CE)	Calc. (CC)	Exp. (CE)	Calc. (CC)
S.S Temperatures (°F)				
T_{case}	302.27	302.32 (150 °C)	392.27	392.04 (200 °C)
T_{bp}	300.90	298.45	388.66	381.74
T_{sol}	298.93	298.12	383.63	380.85
T_{dbc}	297.77	297.53	379.27	379.28
$T_{reference}$	297.32	297.32	377.04	378.73
$T_{ambient}$	73.0	73.0	73.0	73.0
Temperature Drops (°F)				
$T_{drop,bp}$	1.37	3.87	3.61	10.3
$T_{drop,sol}$	1.97	0.33	5.03	0.89
$T_{drop,aln}$	1.16	0.59	4.36	1.57
$T_{drop,cu}$	0.45	0.21	2.23	0.55

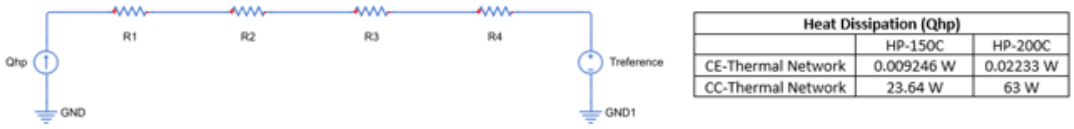

Figure 5.6. Initial electrical schematic for steady state analysis.

5.3.3 Modifications to Cauer-Equivalent RC Circuit

The discrepancies between the results of the experimental and calculated temperature values from Table 5.5 indicated that refinement of the model was necessary to account for neglected constriction of the heat flow from the baseplate into the DBC region and edge effects. All calculations in this section were executed in temperature units of Kelvin (K), then converted to Fahrenheit (°F) shown in the following tables.

5.3.3.1 Addition of Constriction Resistance (R_{c1})

An additional resistance was added at the baseplate node to account for the narrowing of the heat flow path from the baseplate into the solder and DBC layers. This additional resistance is shown as R_{c1} in Figure 5.7. Its value was determined by matching the temperature drop ($T_{drop,bp(CC)}$), given in Table 5.5, associated with the hot plate temperature ($T_{case(CC)}$) to the baseplate temperature ($T_{bp(CC)}$). This resulted in an increase in both the boundary conditions as shown in Figure 5.7.

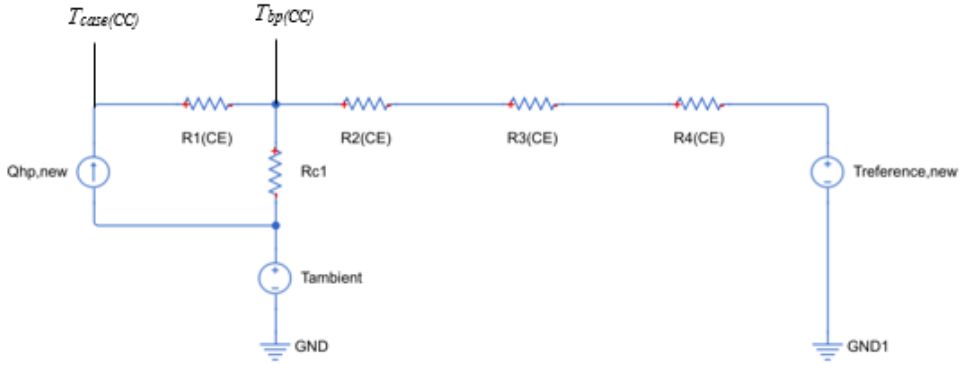

Figure 5.7. Electrical schematic (Steady State) of experimental thermal network with constriction resistance, R_{c1}.

5.3.3.2 Addition of Edge Effect Resistance (R_{e1})

Once the constriction resistance was obtained, an edge-effect resistance for other layers was computed. A modification to $R_{2(CE)}$ in the network was done by adding a parallel resistance thus reducing the equivalent resistance between nodes. This additional resistance was determined by the circuit schematic shown in Figure 5.8. With the expected temperature drop of the solder layer known ($T_{drop,sol(CC)}$), Equations 5.2-5.5 were used in sequential order to compute the resistance value for R_{e1}.

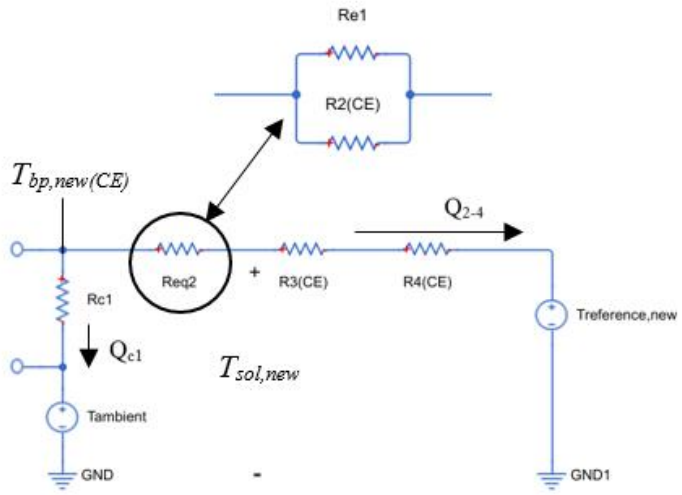

Figure 5.8. Thermal network (Steady State) with implementation of edge-effects through addition of R_{e1} into the network.

$$T_{sol,new} = T_{bp,new(CE)} - T_{drop,sol(CC)} \tag{5.2}$$

$$Q_{2-4} = Q_{hp,new} - Q_{c1} = Q_{hp,new} - \frac{T_{bp,new(CE)} - T_{ambient}}{R_{c1}} \tag{5.3}$$

$$R_{eq2} = \frac{T_{drop,sol(CC)}}{Q_{2-4}} \tag{5.4}$$

$$R_{e1} = \frac{R_{2(CE)} R_{eq2}}{R_{2(CE)} - R_{eq2}} \tag{5.5}$$

5.3.3.3 Results of R_{c1} and R_{e1} Modifications

Figure 5.9 displays the configuration of the modified circuit with their corresponding boundary conditions. Some final small adjustments to other circuit components were made for a better fit to the temperature data.

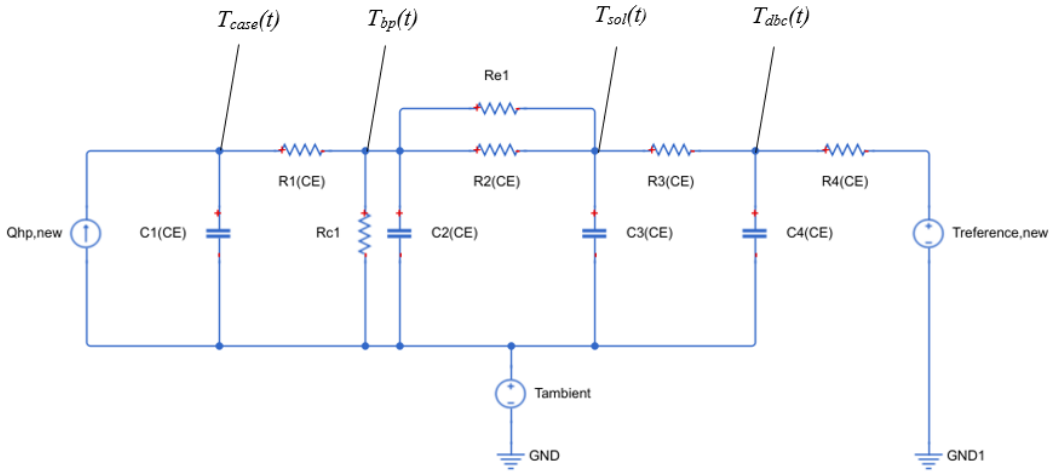

Figure 5.9. Schematic of modified Cauer RC circuit.

Table 5.6 displays the steady state simulation results using the network of Figure 5.9. Furthermore, the updated circuit components that generated these accurate temperatures are provided in Table 5.7. In comparison to Table 5.2, the thermal capacitances of $C_{3(CE)}$ and $C_{4(CE)}$ were increased along with $R_{4(CE)}$ being reduced to match the top surface temperature from the thermal experiment (T_{dbc}).

Table 5.6. Final steady state simulation with implementation of R_{c1} and R_{e1}.

Measurements	**HP-150C Analysis**		**HP-200C Analysis**	
	Mod Exp. (CE)	Calc. (CC)	Mod Exp. (CE)	Calc. (CC)
S.S Temperatures (°F)				
T_{case}	302.2	302.32 (150 °C)	391.65	392.04 (200 °C)
T_{bp}	298.33	298.45	381.35	381.74
T_{sol}	297.99	298.12	380.42	380.85
T_{dbc}	297.61	297.53	379.26	379.28
$T_{reference}$	297.56	297.32	378.99	378.73
$T_{ambient}$	73.0	73.0	73.0	73.0
Temperature Drops (°F)				
$T_{drop,bp}$	3.87	3.87	10.3	10.3
$T_{drop,sol}$	0.34	0.33	0.93	0.89
$T_{drop,aln}$	0.38	0.59	1.16	1.57
$T_{drop,cu}$	0.05	0.21	0.27	0.55

Table 5.7. Circuit components for the modified Cauer circuit.

Circuit Parameters	Powerex Parts (HP-150C)	Powerex Parts (HP-200C)
Thermal Resistances (K/W)		
$R_{1(CE)}$	82.4707	89.8654
$R_{2(CE)}$	118.2863	125.1081
$R_{3(CE)}$	69.6306	108.4042
$R_{4(CE)}$	8.75	25.0
R_{c1}	5430	2965
R_{e1}	130	280
Thermal Capacitances (J/K)		
$C_{1(CE)}$	8.8292e-06	1.2354e-05
$C_{2(CE)}$	0.1360	0.08926
$C_{3(CE)}$	5.00	1.75
$C_{4(CE)}$	6.35	1.85

Using the circuit of Figure 5.9 as a description of the Powerex test piece, Figures 5.10 and 5.11 show the de-convolved internal transient temperature profiles of each material node at the two hot plate temperatures from the experimental results.

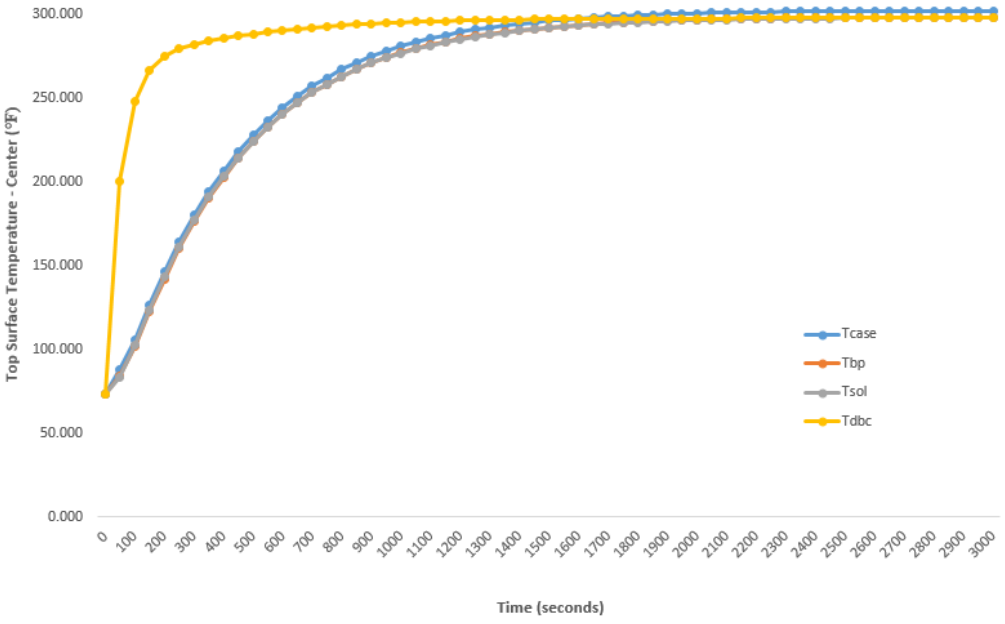

Figure 5.10. Temperature profiles for each material layer in Powerex package at hot plate temperature of 150 °C (HP-150C).

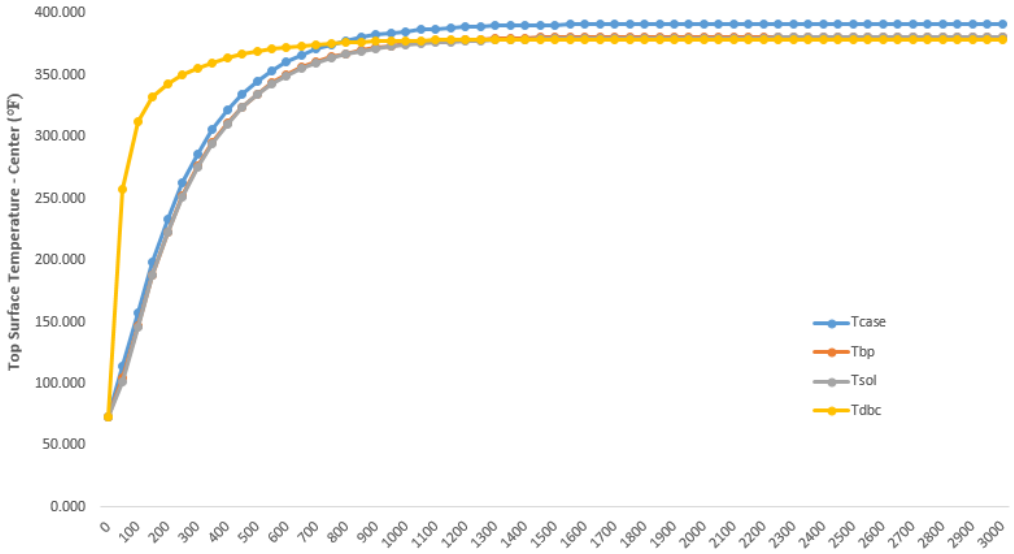

Figure 5.11. Temperature profiles for each material layer in Powerex package at hot plate temperature of 200 °C (HP-200C)

A comparison between the emissivity-calibrated thermal imaging camera and modified Cauer RC circuit results for the top surface temperature profile (T_{dbc}) are provided in Figure 5.12. The thermal experimentation and Cauer RC circuit were equivalent in behavior for both hot plate temperatures. This outcome validated that this circuit precisely models the thermal behavior taking place within the Powerex package. With the modified Cauer-network established, some of the layers in this circuit were removed for a comparison between the Powerex and PCD test pieces.

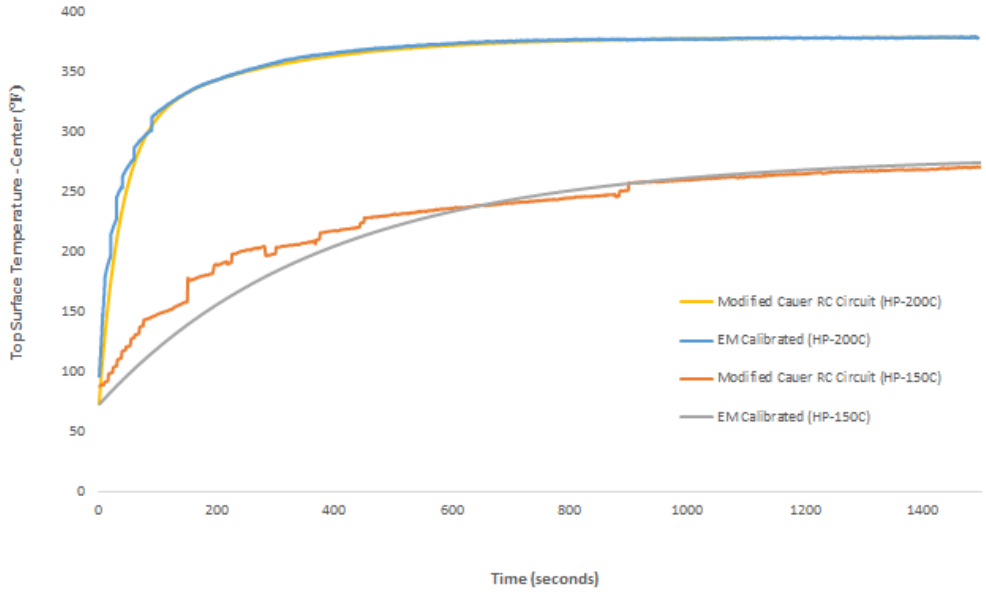

Figure 5.12. Comparison between EM-calibrated camera and Cauer RC model temperature profiles (T_{dbc}) for Powerex piece.

5.4 DBC Cauer RC Circuit

The baseplate and solder layers of the Powerex test piece can be removed from the developed Cauer RC circuit and thus the effects on the heat flow can be correspondingly removed. This leaves just the DBC section in the circuit (diagram shown in Figure 5.13) for a direct comparison to the PCD test pieces.

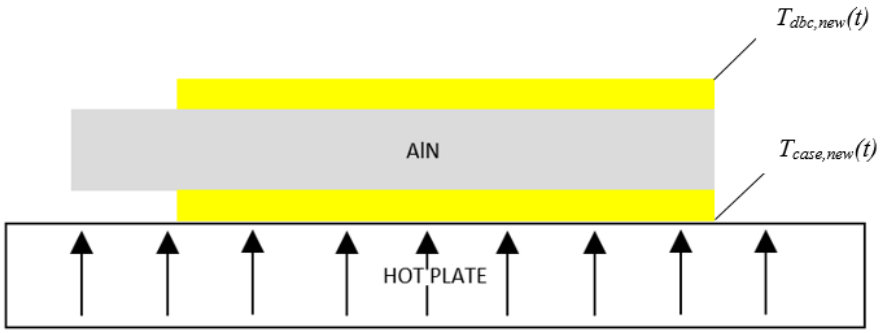

Figure 5.13. Demonstrating theoretical thermal experiment with DBC substrate ($T_{dbc,new}(t)$: new top surface temperature profile representing DBC substrate as function of time and $T_{case,new}(t)$: new bottom temperature profile of DBC substrate as function of time).

The reduced circuit model is provided in Figure 5.14 with new temperature labels for each layer. The thermal resistor and capacitor values for the AlN and copper layers remain unchanged and were shown previously in Table 5.7. In addition, the heat dissipation ($Q_{hp,new}$) for this new circuit was decreased to a lower value in order to maintain the exact hot plate temperature at the bottom of the DBC substrate. The other boundary condition concerning the reference temperature ($T_{reference,new}$) was increased due to the expected additional influx of heat. Simulation results for the top surface temperature profiles for the DBC-only circuit, at the two hot plate test temperatures, are displayed in Figure 5.15.

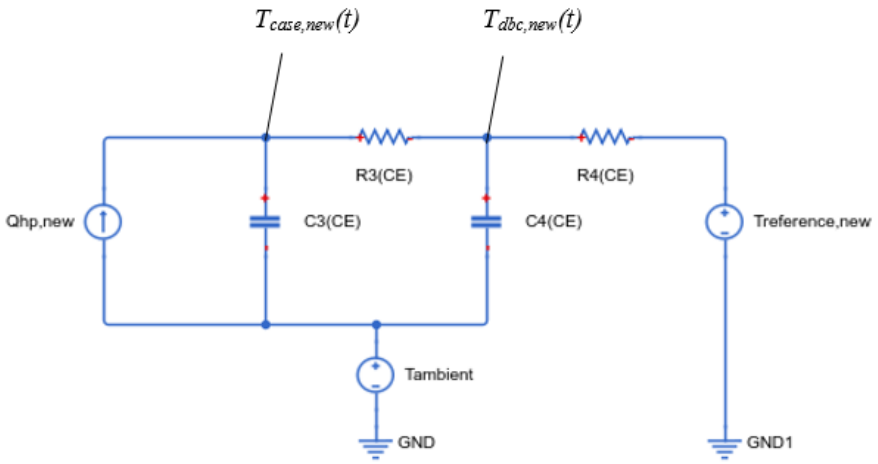

Figure 5.14. Electrical schematic of DBC-only Cauer RC circuit.

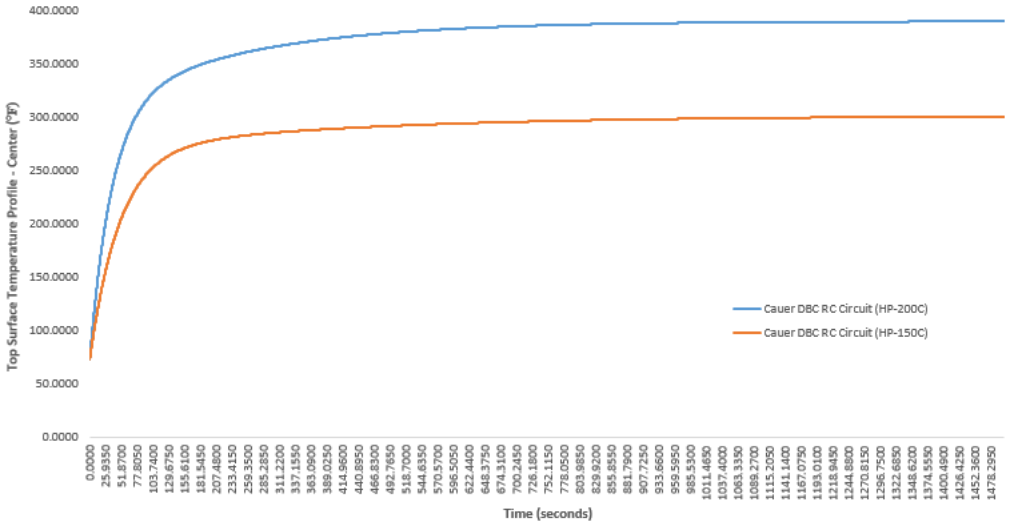

Figure 5.15. DBC-only Cauer RC circuit new temperature profiles.

Bibliography for Chapter 5

[1] Gachovska, Tanya, et al. "Transient Electro-Thermal Modeling of Bipolar Semiconductor Devices." Morgan & Claypool Publishers, 2013.

[2] J. Wilson, "Thermal Conductivity of Solders," *Materials, Compounds, Adhesives, Substrates Technical Data*, Vol. 12, No. 3, 2006.

[3] M. Occhionero, R. Hay, R. Adams and K. Fennessy, "Aluminum Silicon Carbide (AlSiC) For Cost-Effective Thermal Management And Functional Microelectronic Packaging Design Solutions," *Ceramic Process Systems Crop.* Oct. 2011.

CHAPTER 6

RESULTS AND DISCUSSION

6.1 Calibration of Emissivity for Co-PCD and Cu-PCD Films

Two types of metal contacts were deposited on the PCD samples. One type of sample consisted of a layer of cobalt on one surface of the PCD (Co-PCD). The other type sample was fabricated by depositing copper on both the upper and lower surfaces of the PCD (Cu-PCD). Data was shown for a hot plate temperature of 75 ºC, though similar results were obtained with experiments using a hot plate temperature of 100 ºC.

The results from the heating experiments for both Co-PCD and Cu-PCD films at different emissivity values for the temperature setting of 75 °C were provided in Figures 6.1 and 6.2, respectively. The temperature profiles measured at the center of these samples were created by averaging the profiles of 7 and 9 different trial runs for Co-PCD and Cu-PCD, respectively. The range of emissivity used for the temperature profiles in the figures were between 0.85-0.95, with the value of 0.63 determined invalid due it generating a steady state temperature above the hot plate temperature. From examining these figures, the steady state temperature increased as the emissivity was decreased. In addition, changing the emissivity had no effect on the speed at which the top surface reached a steady state temperature.

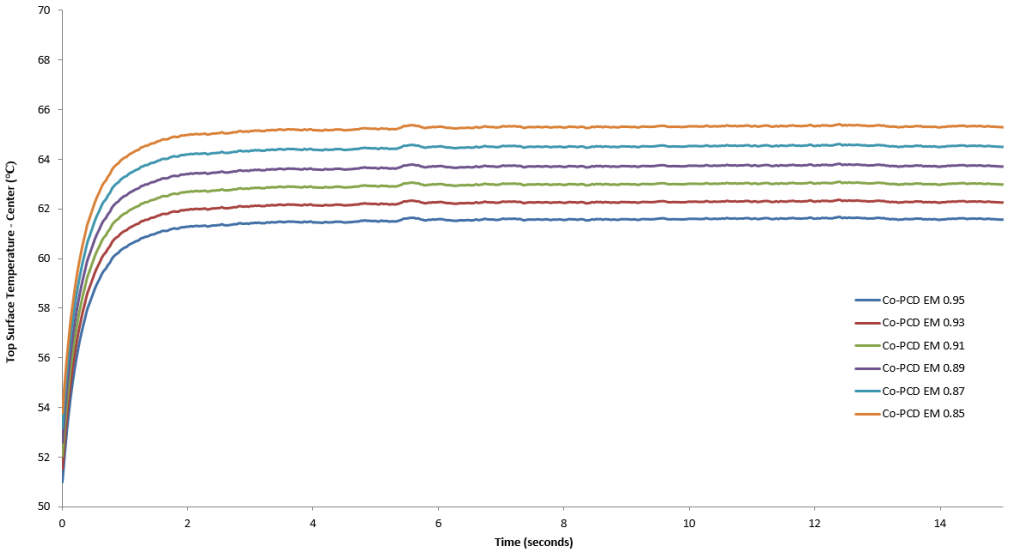

Figure 6.1. HP-75C Co-PCD films top surface temperature profiles at differing emissivities.

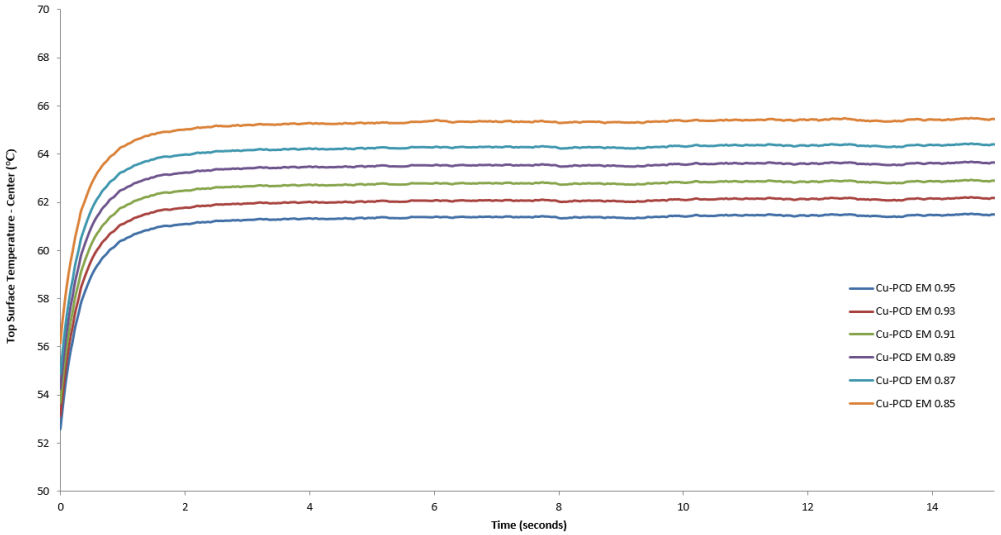

Figure 6.2. HP-75C Cu-PCD film top surface temperature profiles at differing emissivities**.**

Due to the unknown emissivity of polycrystalline diamond, the steady state temperature and temperature differential between the final temperature and the hot plate for both PCD films has no definite value. The specified temperature ranges of these two parameters are depicted in Table 6.1 and 6.2 for each PCD film. The temperature differential assumes that the hot plate remains constant (no fluctuations) at 75 °C

throughout each trial. From the experiment, the Co-PCD film settled at a lower temperature compared to Cu-PCD film for almost every emissivity. The resulting steady state temperatures have a variation between emissivity values (0.85-0.95) of 3.74 °C and 3.96 °C for the Co-PCD and Cu-PCD films, respectively. This temperature span for both PCD films was relatively small. Therefore, an accurate representation of the top surface temperature profile was obtainable utilizing one of the emissivity values. Selecting an emissivity in this range can approximate a temperature on the surface of polycrystalline diamond at any point in time with minimal error.

The temperature differential across these films ranged from 9.70-13.45 °C for Co-PCD and 9.52-13.49 °C for Cu-PCD. Evaluating the temperature drop at each emissivity, the Co-PCD film had a slightly less temperature difference (0.04-0.05 °C) across its thickness compared to the Cu-PCD film. This correlated to the Co-PCD film having a lower thermal resistance compared to Cu-PCD film. This may indicate that the cobalt coated polycrystalline diamond might have a better surface adhesion than copper on PCD.

Table 6.1. Experimental results of Co-PCD film.

Emissivity	**Steady State Temperature (°C)**	**Temperature Differential (°C)**
0.95	61.55	13.45
0.93	62.24	12.76
0.91	62.96	12.04
0.89	63.71	11.29
0.87	64.49	10.51
0.85	65.30	9.70

Table 6.2. Experimental results of Cu-PCD film.

Emissivity	Steady State Temperature (°C)	Temperature Differential (°C)
0.95	61.51	13.49
0.93	62.20	12.80
0.91	62.92	12.08
0.89	63.67	11.33
0.87	64.44	10.56
0.85	65.48	9.52

With the Co-PCD sample having a lower thermal resistance than Cu-PCD, the Co-PCD film's top surface should reach a steady state temperature in a shorter time. Figure 6.3 demonstrated this with a comparison of the top surface temperature profiles between the Co-PCD and Cu-PCD samples. The temperature data in this figure was normalized so that the emissivity value has no impact on the results. The data indicated that the Co-PCD sample is about three times faster with respect to the temperature rise than the Cu-PCD sample. Approximately, the Co-PCD sample reached steady state at 5.41 seconds and the Cu-PCD sample arrived at 14.52 seconds.

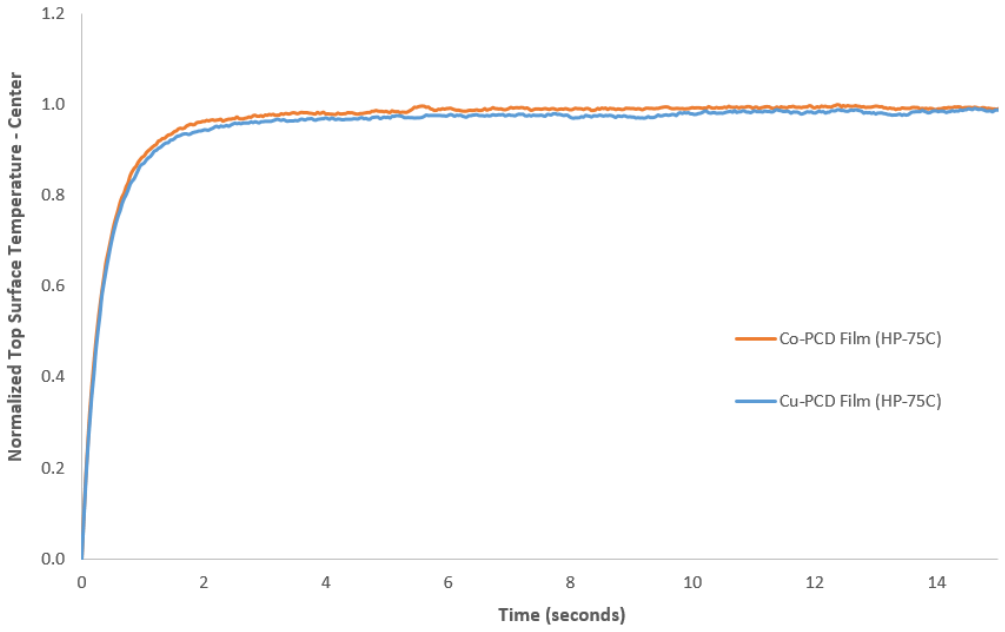

Figure 6.3. Normalized top surface temperature profiles of PCD samples.

In general, copper's thermal conductivity is three times greater than cobalt. Despite this large disparity in thermal conductivity, the cobalt-PCD sample still possessed an overall lower thermal resistance. As a result, this outcome correlated to cobalt's interconnections qualities with polycrystalline diamond outperforming copper's superior material properties.

6.2 AlN Substrate (DBC) of Powerex Sample Compared to the PCD Samples

The DBC section of the Powerex test samples were analyzed based on the two hot plate temperatures of 150 °C and 200 °C. Figure 6.4 displayed their respective normalized top surface temperature profiles measured at the center of the AlN substrate (DBC). Both of the temperature profiles were related to the simulation results utilizing the modified Cauer RC circuit previously described in chapter 5. The time responses depicted in Figure 6.4 indicated that the AlN substrate reached steady state (99% of final value) at approximately 17.5 minutes and 13.0 minutes for hot plate temperatures of 150

°C and 200 °C, respectively. The difference in these response times corresponded to an increase in heat dissipation from the raised hot plate temperature.

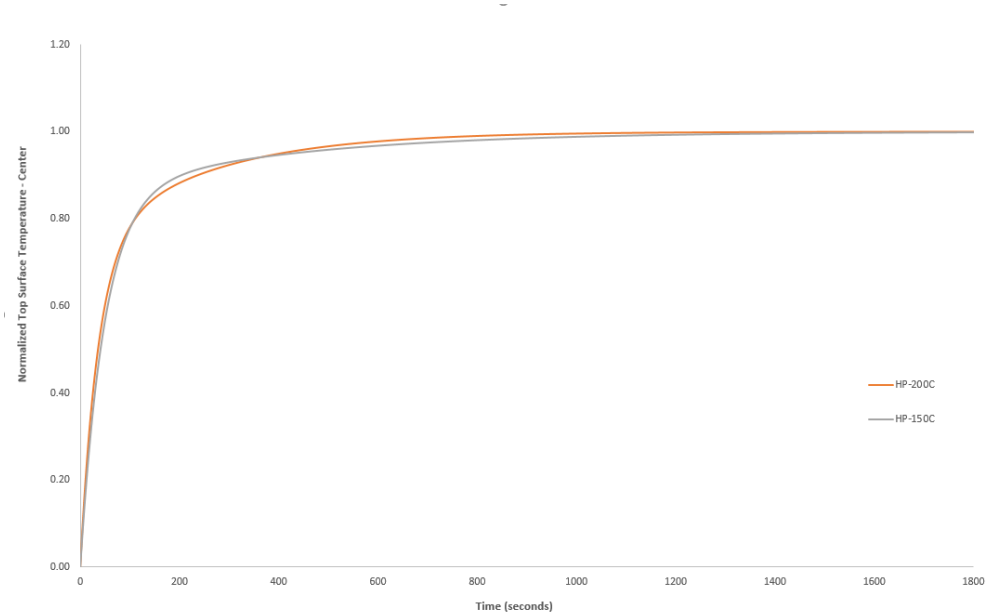

Figure 6.4. Normalized temperature profiles of DBC section of Powerex samples.

A comparison between the standard DBC section of the Powerex samples and the Co-PCD and Cu-PCD samples is provided in Figure 6.5. Noticeably, both PCD samples approached steady state considerably faster than the DBC (AlN). If implemented into the standard power semiconductor device package replacing the AlN substrate, the PCD films would possibly improve the transient heat flow by a factor of 50 to 150 times (Cu-PCD and Co-PCD, respectively).

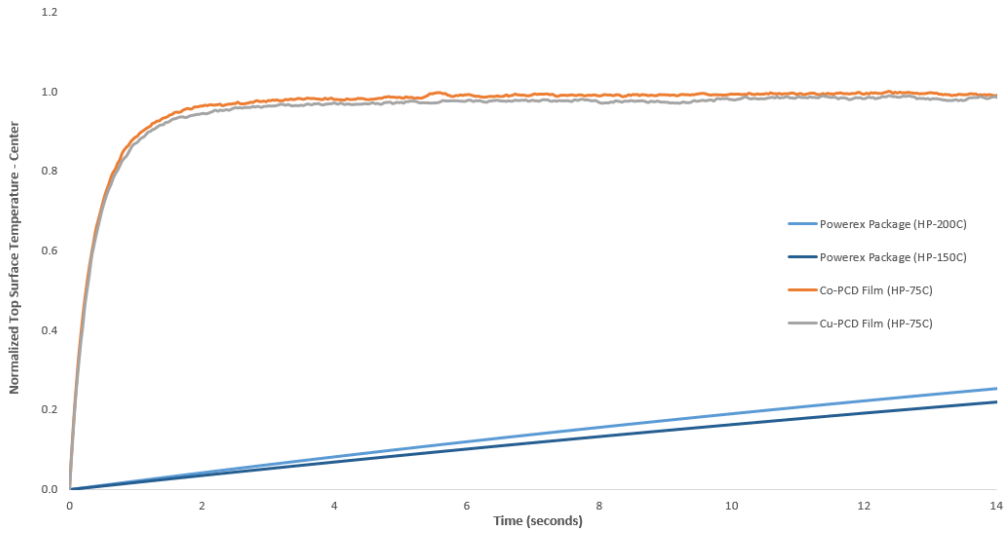

Figure 6.5. Normalized temperature profiles of samples over a 15-second time interval.

A different view of the comparable performance of the samples is represented in Figure 6.6. The transient temperature response of the DBC section was renormalized to a standard scale of 0 to 0.2. This range was selected because at 0.2 of the steady state value, the DBC section reached the equivalent hot plate temperature utilized in the PCD experiments (75 °C). The AlN substrate reached 75 °C at 17.75 seconds for the hot plate at 200 °C and 30.50 seconds for hot plate at 150 °C (not fully shown in Figure 6.6).

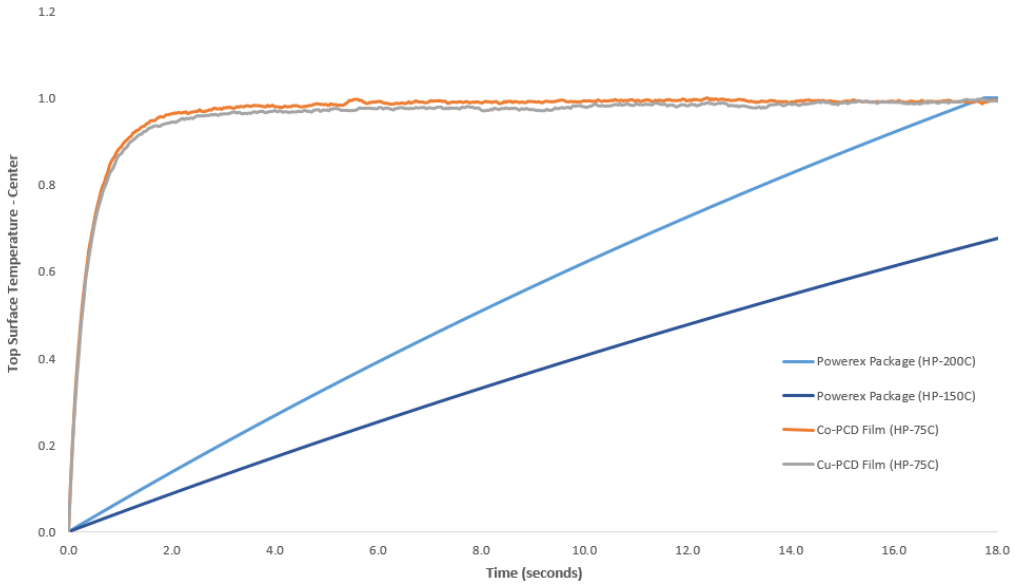

Figure 6.6. Renormalized temperature profile of the DBC section compared to the two types of PCD samples.

Considering all these factors, both the Co-PCD and Cu-PCD samples possessed much improved thermal characteristics compared to the DBC section of a standard power semiconductor device package.

CHAPTER 7

CONCLUSION AND OUTLOOK

New materials (polycrystalline diamond, PCD) that could serve as the layer for electrical isolation while improving heat flow from the semiconductor to the case, in power semiconductor packages, was compared to the existing package technology of the direct-bond copper (DBC) substrate consisting of sintered copper onto AlN dielectric. The PCD materials offer the opportunity to operate wide bandgap (WBG) semiconductors at higher breakdown voltages and at higher junction temperatures than achievable using silicon.

Heat flow measurements were performed using an emissivity-calibrated thermal (IR) imaging camera. Samples from a commercially available power module were used and compared to the PCD samples. Results from the commercial module had to be de-convolved to exclude the effects of the baseplate and solder layers that were not present in the PCD samples. The final comparison showed that the PCD material was clearly superior in thermal performance as compared to the commercial package materials (DBC). Two types of PCD samples were tested. One sample was coated with cobalt (Co-PCD) on its top surface only and the other was coated with copper (Cu-PCD) on its top and bottom surfaces. The final comparative results are repeated in Figure 7.1 (same as Figure 6.6). These results indicate the great promise that PCD has to improve power device packaging.

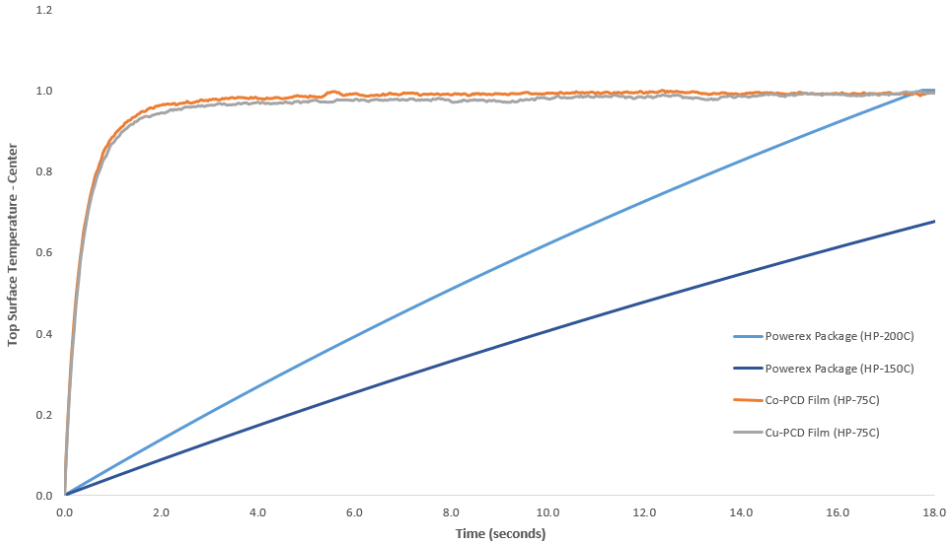

Figure 7.1. Penultimate results comparing the relative temperature rise of the top surface of samples heated from below at constant temperature.

Deeper analysis between the two types of PCD samples revealed that the Co-PCD film has a thermal transient response time three times faster than the Cu-PCD film. This likely indicates that the adhesion between polycrystalline diamond and cobalt is better than with copper. Therefore, the Co-PCD film is potentially a better option, though more tests are needed to confirm the adhesion qualities and more importantly, whether the metal-PCD interface can withstand the rigors of thermal cycling seen in commercial electronic packages.

Other areas of interest for future research would be performing dielectric breakdown strength tests, studying lateral heat flow, ways of interconnection into a standard package structure, and examining mechanical behavior exhibited under thermomechanical stress within a package. The lateral heat flow through and across the PCD samples requires further study. Examining lateral heat flow to determine if heat is spreading evenly across these materials or if hot spots develop in certain areas. Another research thrust would be

determining the interface and connectivity among the PCD films with a theoretical baseplate and power semiconductor device. These connections are crucial for smooth transition of heat flow between the different layers. If there is air gaps in between these layers the heat transfer is slowed down drastically. The current technology uses solder or contact pads as an interconnection material for the baseplate and device, however, these methods may not work with polycrystalline diamond due to its rough and rigid surface. The stress and strain that occurs, as captured by the material system of CTE's, should also be examined in terms of entirely new materials for other package layers to enhance the overall performance and reliability of the PCD layer in addition to the entire package.