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Design and Optimization of a Novel Monolithic Spring for High-Frequency Press-Pack SiC FET Modules

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DESIGN AND OPTIMIZATION OF A NOVEL MONOLITHIC SPRING FOR HIGH-FREQUENCY PRESS-PACK SIC FET MODULES

by

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Silicon Carbide (SiC) Field-Effect Transistor (FET) modules lead the way in power electronics, being superior in efficiency and robustness for high-frequency applications. The shift towards SiC from traditional silicon (Si)-based devices is driven by its superior thermal conductivity, higher electric field strength, and operational efficiency at elevated temperatures. These features are critical for the development of next-generation, grid-oriented power converters aimed at enhancing the reliability and sustainability of power systems. This research focuses on high-frequency press-pack (HFPP) SiC FET modules, addressing the primary challenge of miniaturizing SiC FET dies without compromising performance, through an innovative press-contact design essential for increased high-frequency efficiency.

The objective of the research is to develop and validate a novel monolithic spring (MS) for HFPP SiC FET modules, aiming to surpass conventional press-pack (PP) limitations. By machining airgap slits from a beryllium–copper block, the proposed MS design seeks to achieve optimal mechanical and electrical performance, targeting a linear spring constant, minimal stray inductance, and enhanced high-frequency body resistance. This approach combines theoretical modeling, finite element analysis (FEA) simulations, and experimental validation to overcome the inefficiencies of existing designs, thereby advancing HFPP SiC module technology and supporting the broader adoption of SiC FET

in power systems. Additionally, FEA simulations are employed to contrast the novel MS design with traditional Si-based transistors, highlighting the MS's advanced performance and efficiency in high-frequency applications. The research signifies a vital step towards improving the performance and sustainability of electrical grids worldwide, demonstrating the potential of SiC technology in transforming power conversion systems.

Table of Contents

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PREFACE

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LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

AC	Alternating current
BeCu	Beryllium-copper
CAD	Computer-aided-design
DC	Direct current
DS	Disc springs
EDM	Electrical discharge machining
FACTS	Flexible AC transmission systems
FEA	Finite element analysis
HVDC	High-voltage direct current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-commutated Thyristors
LPP	Lamped press-pack
MOSFET	Metal–oxide–semiconductor field-effect transistor
MS	Monolithic spring
MV	Medium voltage
PP	Press-pack
SCFM	Short-circuit failure mode
SCR	Silicon-controlled rectifier
Si	Silicon
SiC	Silicon Carbide
3D	Three-dimensional

CHAPTER 1. INTRODUCTION

Emerging medium-voltage (MV) grid-oriented power converters are constantly searching for advanced power modules which have high-current capacity, low conduction losses, and high switching frequency. These advancements lead to improved distribution efficiency and better grid resiliency [1]. Moreover, when the voltage of the converter goes above operational limits, short-circuit failure mode (SCFM) as a backup plan is necessary to ensure safety and reliability. Press-pack (PP) silicon-controlled rectifiers (SCRs), silicon (Si-) based Integrated Gate-Commutated Thyristors (IGCTs), and Si based Insulated Gate Bipolar Transistor (IGBTs) are some of the examples of power modules that share similar features suitable for the traditional power distribution systems. However, these components encounter certain limitations, e.g., unavoidable resistive and inductive losses, due to the voltage drop across the module and positive inductance value of the module. Another limitation of Si-based PP modules lies in the distribution of force across the transistor dies. Uneven pressure distribution can lead to variable resistivity within the die, which in turn causes excessive heat dissipation. This increased heat can negatively affect the module's reliability. In [2], researchers have focused on improving this force distribution in half-bridge IGBT PP module to enhance overall reliability. Furthermore, these Si-based PP modules are restricted by their maximum carrying capacity and the maximum frequency at which they can operate effectively. The current rating and switching frequency are critical factors that can greatly impact the performance and efficiency of power distribution systems.

1.1 Literature review

Current PP IGBT modules are a good starting point for design due to their similarity with Silicon Carbide (SiC) Field-Effect Transistors (FETs). Yet, developing SiC FET modules is a lot more challenging, due to two reasons. 1) The SiC FET parts, including the die and the pads, are significantly smaller. The size of SiC FET parts is only about half to a fifth the size of these parts in IGBT chips, given the limitations in manufacturing that are essential to reduce imperfections during the wafer production phase [3]. This small size makes it difficult to achieve sufficient electrical contact for the source and gate pads, which is essential for the reliability. 2) The physical properties of the PP IBGT modules, specifically their stray inductance (typically 150–300 nH) and resistance when using stainless-steel disc springs (DSs), are suitable only for lower switching frequencies, up to 1 kHz [4]. Nevertheless, these structural properties are suboptimal for SiC FETs, given that these transistors are engineered for more rapid switching capabilities, and are up to 10 times quicker than their IGBT counterparts.

Despite the advantages of SiC over IGBT, the described challenges have been addressed in the literature. In [5], “fuzz buttons” have been proposed to improve the advantageous properties of SiC in power modules. Fuzz buttons have been introduced as a solution to establish connections in the compact SiC modules. However, the implementation of fuzz buttons presents several technical difficulties. The proposed model suffers from a limited current carrying capacity, which is not ideal for high-power applications; a high stray inductance, leading to decrease in efficiency at higher frequencies; and a high electrical resistance, which can create cooling problems and can reduce robustness in the long run. In the pursuit of reducing stray inductance, the

introduction of a SiC power module utilizing a sandwiched press-pack architecture was suggested [6]. This configuration aimed to optimize the module's performance by minimizing stray inductance within its operational circuitry. However, this innovative approach introduced significant complexities, particularly in the fabrication of the busbar. Ensuring effective and consistent contact emerged as a formidable challenge alongside the required pressure between the gate pin and the gate pad. Therefore, manufacturing process becomes the point of interest due to the strong relationship between mechanical precision and electrical efficiency in advanced power module design.

The thermal management of PP SiC FET modules is also a critical aspect, particularly due to the thermomechanical stress introduced by temperature fluctuations. As operational temperatures rise, the PP SiC FET modules, along with other components, experience thermal expansion. Given the heterogeneous nature of the PP module, which composes of various material, wherein the disc springs, typically manufactured from high-quality spring steel, and the semiconductor elements exhibit distinct coefficients of thermal expansion, differential expansion is inevitable. This discrepancy in expansion rates can lead to increase in pressure on the semiconductor devices and other components, attempting to compensate the thermal expansion of the adjacent materials [7]. Such an increase in pressure may result in an increase of the clamping force within the press-pack module, which could affect the module's structural integrity and performance over time.

Another research has been conducted to investigate disc spring (DS) based PP SiC IGBT and SiC metal–oxide–semiconductor field-effect transistor (MOSFET) devices [8]. Required pressure and reliable contact within the device is ensured by DS-based packaging. The research highlights that the DS based PP module provides an effective solution for the

challenges typically associated with conventional soldered packaging, such as series connection difficulties and reliability issues, making it a suitable choice for SiC IGBT and SiC MOSFET modules operation at higher voltage ratings. It has been also noted that the voltage required to supply the same current value decreases as the temperature of the spring module decreases. Therefore, it is possible to lower the power consumption as a result of reduced operating temperature of the module, which can be achieved by decreasing the thermal resistance of the spring module.

In examining the effects of thermal resistance on mechanical stress distribution on the semiconductor dies, two articles present innovative approaches for PP technology. These studies focus on DS based PP SiC IGBT and SiC MOSFET devices and try to achieve uniform thermal stress on the transistor dies. In [9], the use of elastic half-space theory to better comprehend mechanical stress distribution under the current lamped-PP (LPP) technologies are introduced. This method redistributes the pressing loads and helps to even out stress distribution across the transistor dies. Z. Dou et al. [10] have created a prototype utilizing the method in [9]. The prototype adjusts the pressure across the transistor dies. Therefore, it is possible to directly compare the thermal distribution of the module. It is concluded from both articles that as the temperature on the transistor dies increases, average leg stress ($\sigma_{leg,avg}$) will increase. This relationship underscores the importance of balanced stress distribution in PP to ensure high reliability when faced with higher thermal stresses. These insights emphasize the importance of design process in the packaging of semiconductor devices to maintain consistent performance under varying thermal conditions. Increased stress can lead to exceeding the standard operation conditions and reducing durability. A novel monolithic spring (MS) design will lower the

thermal resistance within the PP module, thereby enhancing the overall efficiency of press-pack SiC FET modules.

The vertical deflection of the novel MS design is enabled with interleaved slit cuts implemented to the body. The MS body can be cut using various manufacturing techniques such as wire electrical discharge machining (EDM), laser cutting [11], abrasive water jet, and plasma cutting [12]. While the precision of these manufacturing processes can be decreased to ±10 μm, this fine precision comes at an increased cost. However, it is important to clarify that this research will not include an analysis of the manufacturing process, since such discussions are beyond the scope of this thesis.

1.2 Research objectives

With the light of the previous research conducted on PP modules, this research work is targeted to:

1. Introduce a novel MS constructed from a beryllium-copper (BeCu) block, superior to the previous work by its high yield strength, specifically designed to address the challenges of press-contact and parasitic elements in HFPP SiC FET modules.
2. Optimize the MS design using FEA such that the MS fulfills the specified deflection distance, spring constant, and uniform distribution of pressure on the dies, which will decrease the parasitic and resistive losses of the module.
3. Manufacture and test the MS design to verify FEA results and conduct failure test on the MS to test its robustness.

The research objectives of this thesis can be expanded, including the engineering of a layered MS structure with apertures for vertical deflection and a consistent spring force vs. deflection constant. The MS design comprise of four legs that enable sintering the body of the MS onto SiC FET dies. The whole design and optimization process of the MS alongside the design parameters and the optimization objectives is described in the following chapter.

CHAPTER 2. DESIGN AND OPTIMIZATION OF PROPOSED MS STRUCTURE

As the industry advances, PP IGBT technology has increased suitability for high-voltage direct current (HVDC) and flexible AC transmission systems (FACTS) due to their increased current ratings and inherent short-circuit failure mode [13]. However, the initial models of PP IGBT modules faced significant challenges in uniform distribution of pressure across the transistor dies. These early rigid-type designs have suffered from non-uniform distribution of pressure, which can adversely affect the modules' performance and robustness [13]. To reduce the adverse effects of the given challenge, Hitachi Energy (previously ABB Semiconductors) has manufactured a compliant-type PP IGBT (StakPak in Figure 2.1) in 2001 [4]. The StakPak configuration employs serial connected DS assembly to apply required contact pressure on each IGBT chip. Nonetheless, DS-based architecture is accompanied by several disadvantages. 1) A single stainless-steel disc offers a limited range of deflection [14]. As a result, each PP module is composed of multi-layered series-stacked discs so that a required summed deflection is met. This multi-layered structure increases the total height and weight of each module. 2) There exist additional copper current paths patched at two sides because stainless steel DS assembly has higher resistive loss compared to the other assembly components. However, these current paths

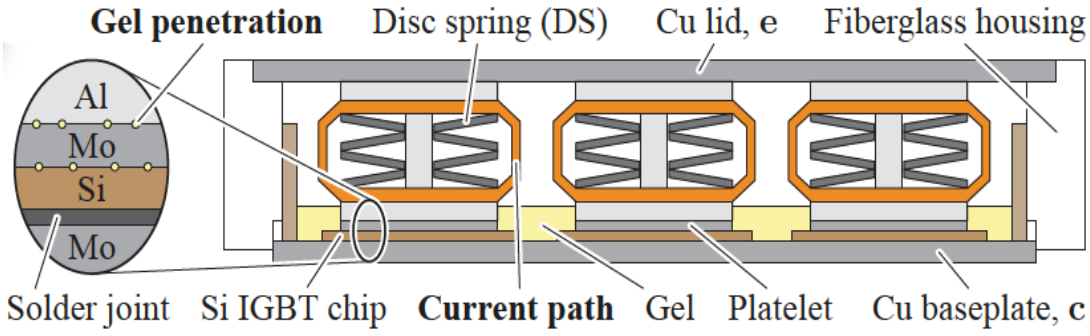


Figure 2.1. Cross-section view of DS-based HFPP switch cell (Benchmark Hitachi StakPak™).

results in two extra dry-contact surfaces, whose resistance is significantly higher than the remaining assembly elements. Also, the PP cross-section area for vertical current conduction is further reduced. 3) The heat transfer efficiency across the DS assembly significantly reduces, reaching only 13.6% of the thermal conductivity possible through the baseplate. This reduction is primarily because of the existence of air gaps within the assembly, which adversely affects the effectiveness of the module's double-sided cooling mechanism. This limitation underscores a critical challenge in the design process, where the applied cooling strategy is compromised by the module structure and material selection of the DS assembly. 4) Over time, the internal dry contact surfaces experienced a gel-penetration issue, which poses challenges to the integrity and robustness of these surfaces. Taken into consideration these challenges, the HFPP switch cell (Figure 2.2) includes a proposed MS design replacing the DS assembles within the PP structure. The proposed MS is manufactured from BeCu block and interleaved laser-cut slits are added to the design. Four Ag-coated legs and a polished top surface features three essential advantages alongside the proposed laser-cut design. 1) A spring with the exact spring constant can be created by designing the shape and size of the slits, while decreasing the resistance at high frequencies, without causing an unwanted increase in stray inductance. 2) The legs of the MS are coated and shaped for direct attachment to the source pads of PP modules accommodating various sizes of SiC FET dies. This versatility enables the proposed MS model to be utilized in various device configurations. 3) Firmly attaching the MS to the device ensures that the junction temperature across the dies remains uniform and increases adjacent thermal capacitance, which smooths out the variation in junction temperature under transient power losses (e.g., short-circuit fault).

2.1 Proposed MS structure and modeling

In this subchapter, the proposed MS design is represented while defining its design parameters. As shown in Figure 2.3, the MS has been designed with a cubic structure. Prior to finalizing the design of MS, a cylindrical version of the MS was also evaluated for comparison to the cubical design, which has better performance.

The cylindrical model has not been included in this thesis due to its relative inferiority to the cubic design. The design of the spring is specifically modelled to allow for deflection along the z-axis, as illustrated in Figure 2.3, which is a three-dimensional (3D) visualization of the MS. The proposed MS design features several horizontal layers, each consist of evenly cut slits, which gives MS deflection capabilities. The bottom surface of the MS is attached to four transistor legs coated with Ag (Figure 2.4), which transfers the clamping force to the transistor dies. The design parameters of the transistor legs are given as *a* and *b*, being the width and length of the transistor die contact, respectively. Airgap slits are cut through the body of the MS on each horizontal layer by defining two perpendicular planes, as shown in Figure 2.6. To create the required pattern which enables vertical deflection, these perpendicular planes alternate orientation on successive layers and each is rotated by 45° around the z-axis. This rotation strategy creates airgap slits along the corner edges of the MS, enabling the MS to vertically deflect.

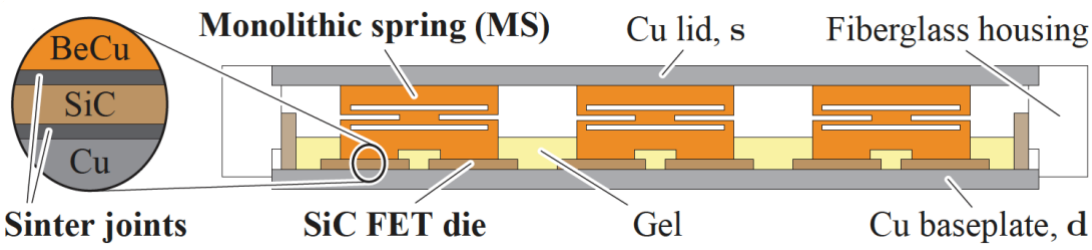


Figure 2.2. Cross-section view of the proposed HFPP switch cell.

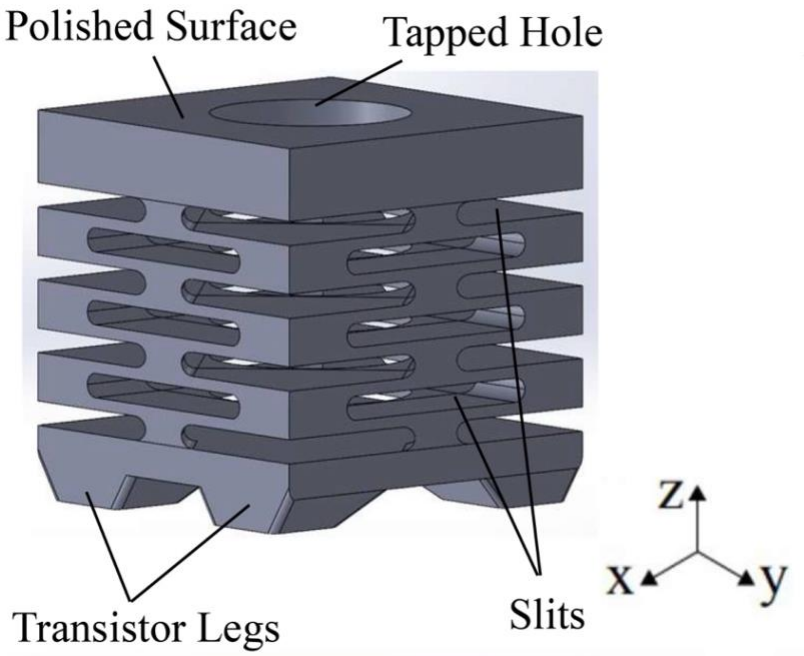


Figure 2.3. The proposed MS rendered model.

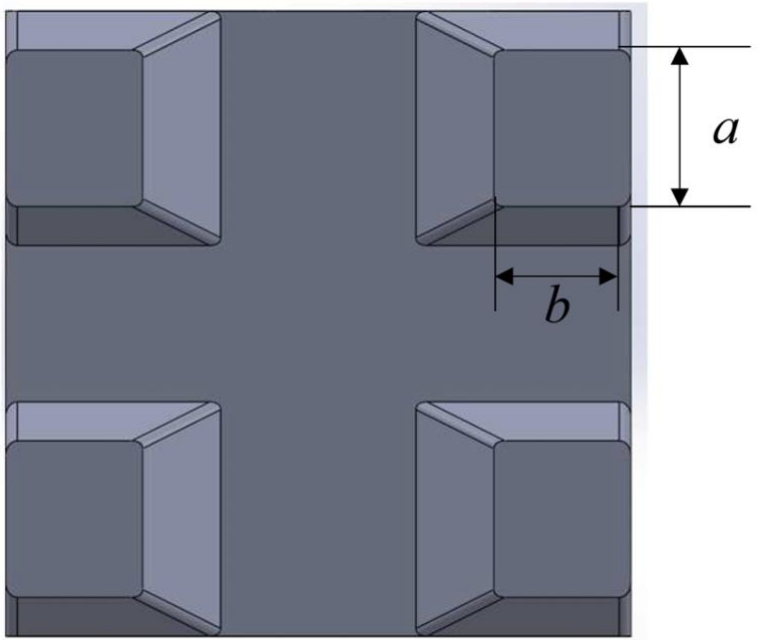


Figure 2.4. A view from bottom demonstrates four legs, each with a layer of Ag coating. The footprint of each leg is versatile, allowing for adjustments to accommodate varying sizes of die pad areas.

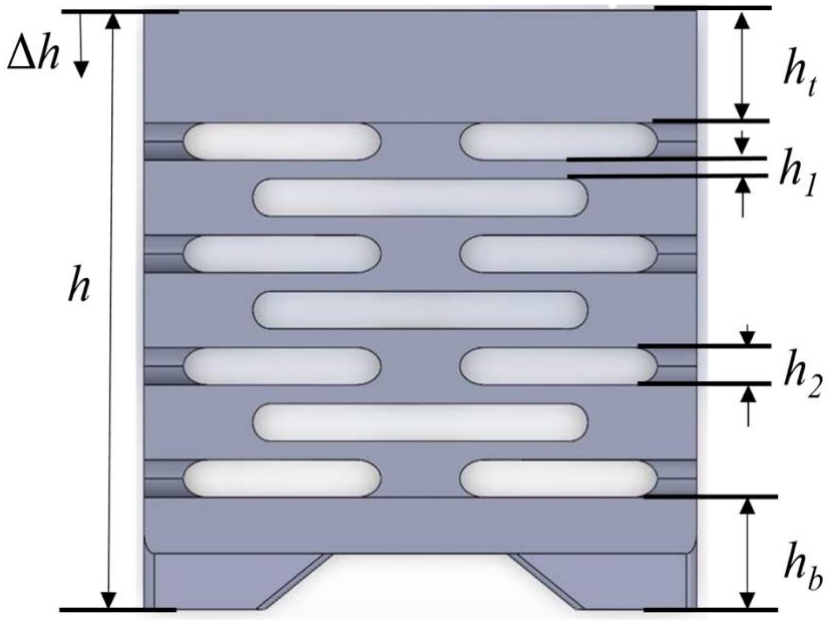


Figure 2.5. Side view of the MS, visualizing the design parameters: total height (h) with deflection of Δh, slit height (h_1), distance between slit layers (h_2), top layer height (h_t), and bottom layer height (h_b).

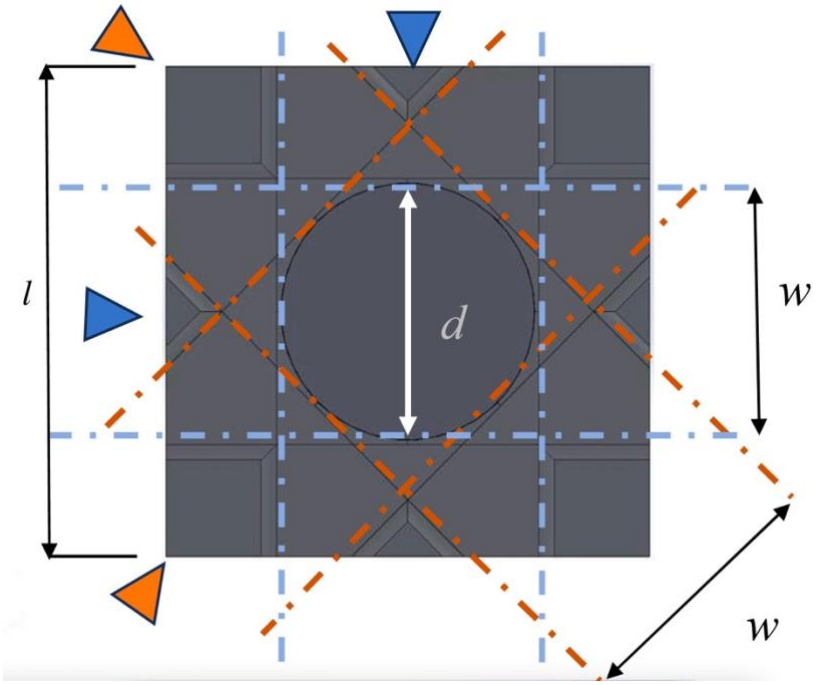


Figure 2.6. The top view of the MS demonstrating MS width l, slit width w, through-hole diameter d (not through the base layer) and tapped hole for mounting. The blue and orange slit layers are interleaved, while laser-cutting directions are denoted by blue and orange arrows.

The design variables and views from different perspectives for the cubical MS are demonstrated through Figures 2.3—2.6. 1) The width of the MS body appears square-shaped and is specified as *l*. This dimension is determined by the size of the FET die and the spacing between them. 2) The width of the slits within the MS is denoted as *w*, with both ends designed to be rounded. This shaping strategy not only minimizes the stress concentration within the material, but also reduces the computational load required for FEA simulations. 3) There are three essential design parameters further define the structure of the slits: h_1, which is the height of the slits; h_2, which is the vertical distance separating one slit from another within successive layers; and *n*, which is the total count of slit layers. 4) The MS is constructed by additional layer heights: h_t, which is the height of the top layer and is characterized by a tapped hole that enables mounting to the Cu lid as seen in Figures 2.2 and 2.5; and h_b, which is the height of the bottom layer equipped with four legs that serve as the interface between the MS and the transistor dies, yet it does not include holes. 5) The clamping force applied on the MS is quantified as *F*, ensuring the required stress levels are reached across the transistor dies while being evenly distributed. 6) All inner layers of the MS are pierced by a uniform cylindrical hole, whose diameter is indicated by *d*. Addition of a cylindrical hole contributes to an increase in the amount deflection of under a constant clamping force. This increased deflection is a desired attribute, as it reduces the spring constant and enhances the controllability of the HFPP FET module while keeping the total height (*h*) constant. 7) Finally, the footprint of the MS legs is defined as *a* and *b*, representing the length and width required to match the transistor die areas. However, in the optimization process, the complexity and computational costs increase significantly as the number of optimization parameters, which is selected from the design parameters,

increases. To manage this complexity efficiently, certain design parameters are preselected, and set based on the specific requirements of the application, as given in the footnotes of Table 2.1.

Table 2.1. Relationships between design objectives and variables.

Design Objectives	Design variables
Deflection, Δh (mm)	$w \uparrow$, $h_1 \uparrow$, $h_2 \downarrow$, $d \uparrow$, $n \uparrow$
Total height, h (mm)	$h_1 \uparrow$, $h_2 \uparrow$, $n \uparrow$
Total mass, m (g)	$w \downarrow$, $h_1 \uparrow$, $h_2 \uparrow$, $d \uparrow$, $n \uparrow$
Max. body stress, $\sigma_{body,max}$ (MPa)	$w \uparrow$, $h_1 \uparrow$, $h_2 \downarrow$
Average leg stress, $\sigma_{leg,avg}$ (MPa)	$w \uparrow$, $h_1 \uparrow$, $h_2 \uparrow$, $d \uparrow$, $n \uparrow$
DC resistance, R_{DC} (mΩ)	$w \downarrow$, $h_1 \uparrow$, $h_2 \uparrow$, d, $n \uparrow$
AC resistance at 20 kHz, R_{AC} (mΩ)	$w \downarrow$, $h_1 \uparrow$, $h_2 \uparrow$, $d \uparrow$, $n \uparrow$
Stray Inductance (AC), L_s (nH)	$w \uparrow$, $h_1 \uparrow$, $h_2 \uparrow$, $n \uparrow$

Upward arrows represent positive correlations, whereas downward arrows represent negative correlations. To improve the optimization process efficiency, following design parameters are predetermined: l =16 mm, $h_t = h_b$ = 3 mm, F = 650 N, n = 7, a = 3.92 mm, and b = 3.34 mm.

Various number of the total slit layers (n) have been compared via FEA simulation. Based on the design objectives, n has been chosen 7. A seven-layer design introduces several benefits. 1) It facilitates a more uniform distribution of stress across the transistor dies, which is essential for robust electrical performance and long-term reliability of the device. 2) It causes the total height (h) and the total mass (m) to decrease, thereby contributing to a more lightweight and compact PP assembly design.

The fundamental design objectives related to the mechanical and electrical performance of the device are presented in Table 2.1, alongside the relation with the design variables. It is important to highlight the existence of an internal through-hole at the center

of the design, which serves multiple purposes. First, this through-hole is strategically positioned to avoid any overlap with the transistor legs, so that no additional stress is accumulated at the center of the device. Second, the presence of the through-hole has been proved to reduce stress within the body of the device and to increase its deflection range (Δh) with a consistent set of design parameters. Third, the introduction of the through-hole reduces the overall mass (m). This reduction is achieved without causing a significant increase in stray inductance and electrical resistance, thereby keeping the superiority of the MS in terms of electrical property while improving its mechanical performance.

Deformation of solid materials under stress is generally classified into two main categories: elastic and plastic deformation, as represented in Figure 2.7 [15]. Plastic deformation occurs in various solid materials because of sustained external force. On the

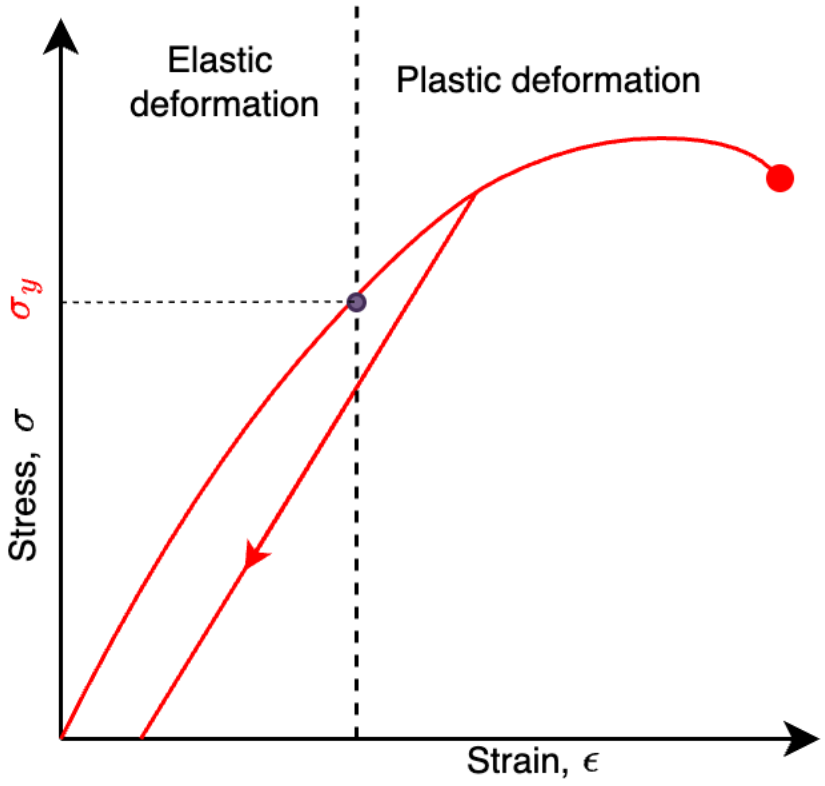


Figure 2.7. Strain vs. stress curves, including elastic deformation and plastic deformation regions.

other hand, elastic deformation is a temporary change where a material stretches or compresses but it can return its original position once the external force is removed. When the external force is no longer exists, any deformation in elastic region disappears. However, it is not possible to recover its initial shape once entered to the plastic deformation region. Stress leads to shifts in the positions of atoms within a material. If further increased, it can break the bonds between atoms, forming small cracks that may grow and eventually cause the material to break apart [15]. The key difference between elastic and plastic deformation is their permanence: elastic deformation is a temporary state that can be reversed, whereas plastic deformation leads to permanent and lasting changes in the material. It is also noted in [16] that a material should not exit elastic deformation region to keep pressure distribution uniform across the transistor dies.

To ensure Δh is within the limits of elastic region, maximum body stress ($\sigma_{body,max}$) should not exceed the material's yield strength (σ_y) with margin. Various materials are investigated and BeCu alloy is selected for the material of MS. This alloy can handle stress of up to 1206 MPa [17], whereas the yield strength of stainless steel is up to 207 MPa [18]. Furthermore, because BeCu is composed of more than 97% copper, it performs better almost like pure copper in terms of electricity and heat conduction. Additional to the constraint for the maximum body stress, the MS should deflect more than 0.7 mm under the preselected configuration (Δh > 0.7 mm). If Δh < 0.7 mm, the imperfections in manufacturing process will cause clamping force to be different than the preselected value.

2.2 Simulation and optimization process of proposed MS using FEA

Finite element analysis, commonly known as FEA, utilizes the finite element method (FEM), which is a computational approach that breaks down an object's structure into a multiple of small elements. These elements are then systematically reassembled at points called nodes. The results of FEA, which will be detailed in forthcoming sections, are exported from the COMSOL Multiphysics 6.1 software suit. Furthermore, LiveLink for MATLAB module has been employed to control the FEA simulations and to construct the optimization algorithm. This methodical approach allows for a detailed investigation of the structural and electrical behavior of the MS under various conditions and increases the efficiency in the design and optimization process.

2.2.1 Construction of the optimization algorithm

The optimization process plays a crucial role in the design methodology of the MS. Although the theoretical design space for the MS might appear limitless, practical manufacturing constraints introduce differences between the initial 3D model and the final manufactured MS. These variations are typically due to the limitations in manufacturing precision, which can affect the exact dimensions and performance of the MS. As such, the design process must consider these potential deviations and must ensure that the MS remains functional and effective within the specified tolerances of the intended application.

To improve the optimization process's effectiveness and to reduce the computational costs, the number of design variables and objectives (Table 2.2) has been reduced intentionally. The variables d and n have been set ahead of time after carefully comparing different combination of these variables (d = 8.4 mm, n = 7). Due to the limits of the manufacturing, scanning the preselected design space is a suitable strategy for the

optimization process, and it also yields the best suitable design points based on design objectives.

The parameters defining the design space have been set as follows: the height h_1 varies from 1 to 2 mm in increments of 0.05 mm; the distance h_2 ranges from 0.5 to 1 mm, also with a step size of 0.05 mm; and the slit width (w) spans from 5.3 to 9.1 mm, with each step being 0.05 mm. The preselected range of w is selected considering the design limitations. Similarly, higher values of h_1 limits the maximum possible width for w. This constraint is essential as it ensures the MS maintains its spring functionality. By adjusting the ranges for various combinations, the optimization process aims to improve the structural integrity and electro-mechanical performance of the MS.

The design objectives have been simplified to reduce computational costs. The first design objective is to limit the maximum body stress $\sigma_{body,max}$ to 1000 MPa. The design configurations that allow for larger deflection when subjected to a maximum external force of 650 N (F) have been focused during the scanning. The evaluation of these design configurations is based on the total height of the MS ($7h_1 + 6h_2 + 6\ mm$). This method of evaluating the design configurations helps to reduce both AC/DC resistance (R_{AC}, R_{DC}) and stray inductance, as detailed in Table 2.1. This optimization approach ensures that the MS not only meets its stress and force requirements but also optimizes its electrical characteristics for better performance. The results of the optimization process have been thoroughly discussed in the following subchapter.

2.2.2 Electrical and mechanical FEA results of the optimization process

The preselected intervals of the design parameters are analyzed using FEA, and the results of this scanning has been displayed in Figure 2.8 through Figure 2.10. These graphs

illustrate the simulation results of scanning various design points, with x and y axis representing the design variables, z axis of the graph indicating the maximum body stress ($\sigma_{body,max}$), and the color gradient showing the deflection value (Δh).

Due to the limitations introduced by the material's tensile strength, the optimal MS configuration is selected from the plotted optimization results. This optimal configuration ensures that $\sigma_{body,max}$ remains below the threshold of 1000 MPa. This process highlights the optimization of mechanical properties and structural dimensions to achieve a design that meets all specified operation criteria.

The optimization scanning of the design variable space confirms the relationships between design parameters and variables, detailed in Table 2.1. The analysis shows that increasing the values of h_1 results in higher $\sigma_{body,max}$ and greater Δh, as seen in Figures 2.9 and 2.10. Like h_1, higher values of w will increase $\sigma_{body,max}$ and Δh as demonstrated in

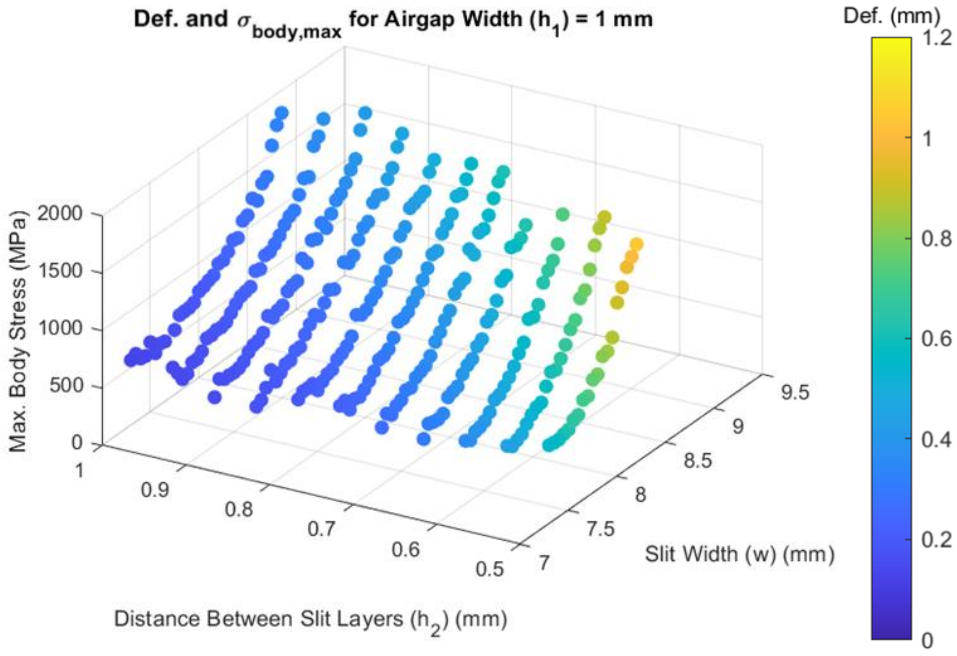


Figure 2.8. Maximum body stress ($\sigma_{body,max}$) and deflection (Δh) simulation results from scanning design variables, while h_1 is 1 mm.

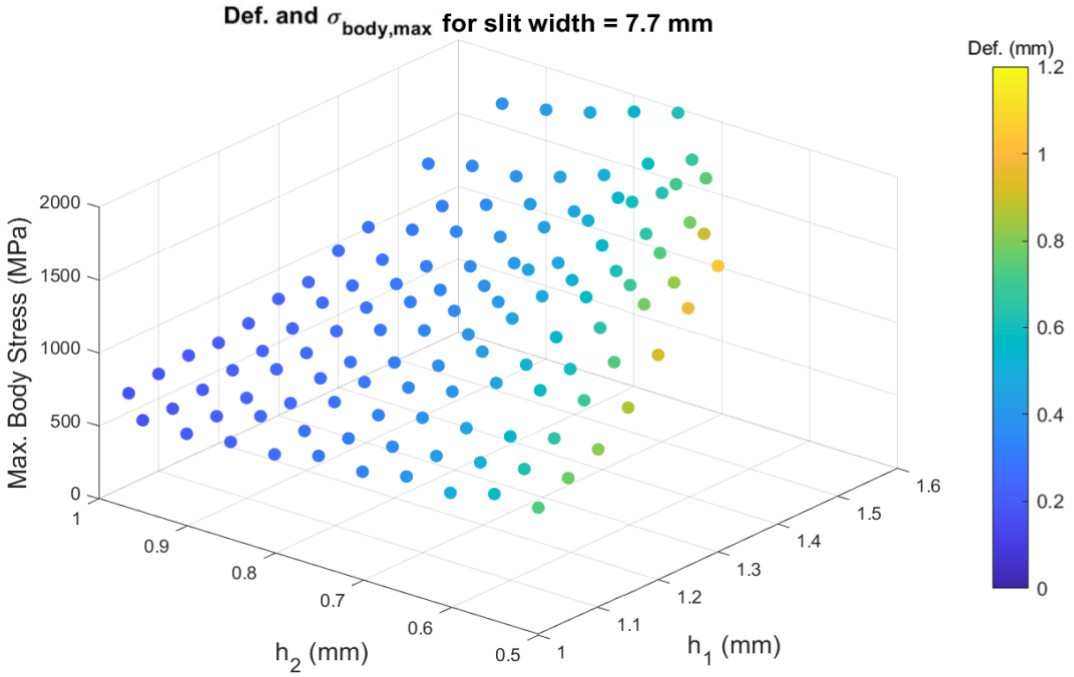


Figure 2.9. Maximum body stress ($\sigma_{body,max}$) and deflection (Δh) simulation results from scanning design variables, while w is 7.7 mm.

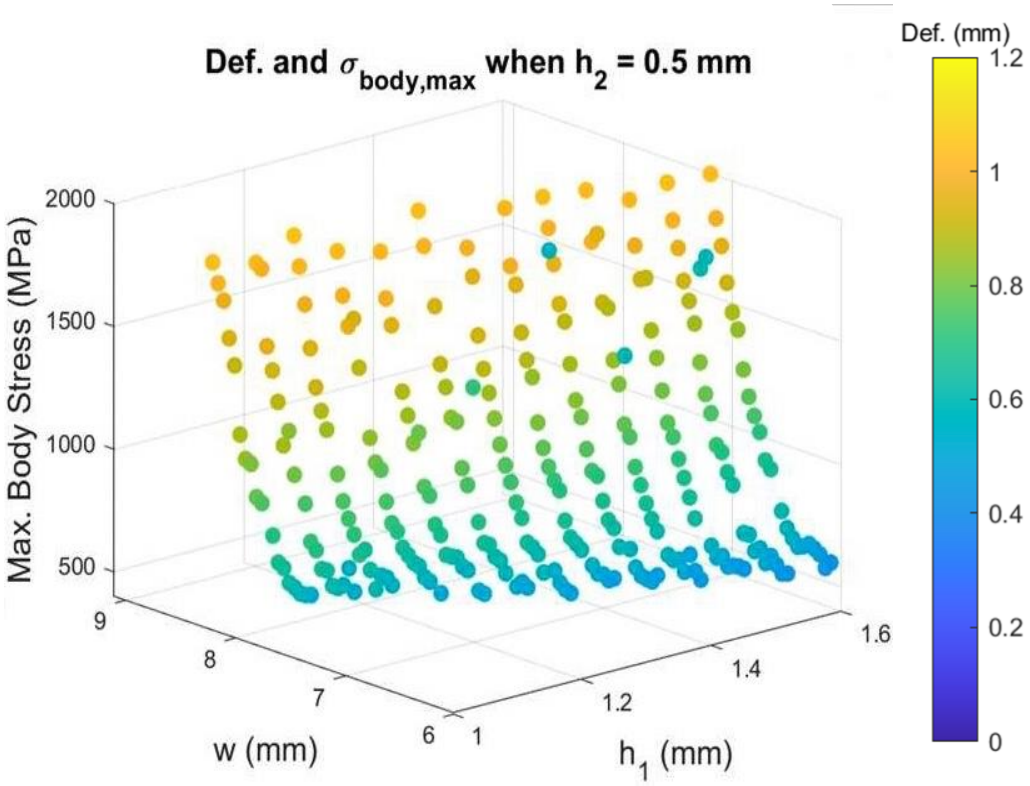


Figure 2.10. Maximum body stress ($\sigma_{body,max}$) and deflection (Δh) simulation results from scanning design variables, while h_2 is 0.5 mm.

Figures 2.8 and 2.10. On the other hand, an increase in h_2 leads to a decrease in $\sigma_{body,max}$

and Δh, as illustrated in in Figures 2.8 and 2.9. This scanning also provides a clear understanding of how the design variables impacts the overall mechanical performance of the MS.

Table 2.2. Design variables and objectives of the optimized variables.

Design Variables	**Design Objectives**
$w = 8.7\ mm$	Deflection, Δh = 0.733 mm
$h_1 = 1\ mm$	Total height, h = 16 mm
$h_2 = 0.5\ mm$	Max. body stress, $\sigma_{body,max}$ = 874.7 MPa
$n = 7$	DC resistance, R_{DC} = 148 μΩ
--	AC resistance at 20 kHz, R_{AC} = 224.5 μΩ
--	Stray Inductance (AC), L_s = 2.8 nH
--	Average leg stress, $\sigma_{leg,avg}$ = 7.7 MPa

The optimized MS design has been selected from the scanned design space and the optimized design variables have been demonstrated in Table 2.2. A design configuration with 7 layers of slit has been adapted to reduce both DC and AC resistance effectively. However, this configurations tends to allow only limited deflection, while strictly maintaining the maximum body stress ($\sigma_{body,max}$) below 1000 MPa. The stress limit has been set to compensate potential inconsistencies that may exist due to manufacturing. Meanwhile, the optimized deflection (Δh = 0.733 mm) has been identified as sufficient and appropriate to move forward for the current application.

The optimized MS has been further simulated using COMSOL software to evaluate the stress distribution across both the body of the MS and the legs attached to the transistor

dies. It has been noted that stress tends to accumulate at the ends of the slits, which explains the strong relationship between the slit width (w) and the maximum body stress ($\sigma_{body,max}$), as depicted in Figure 2.11. Moreover, the pressure distribution across the transistor dies averages at 7.7 MPa. The stress on the transistor die surface shown in Figure 2.12, is notably uniform, which makes it suitable to implement in the current application. The uniform distribution is crucial as it ensures consistent electrical performance across the entire assembly, thereby enhancing the reliability of the PP module.

2.3 Comparison of MS and DS module in terms of design parameters

The DS module is an elaborate structure assembled from several layers of DSs along with other components, which are strategically assembled to separate DSs from the pathway of electrical current. Therefore, any unintended electrical connections that could lead to short circuits within the module is avoided. While the DS architectural approach is effective, it leads to existence of various dry contact surfaces within the current flow path

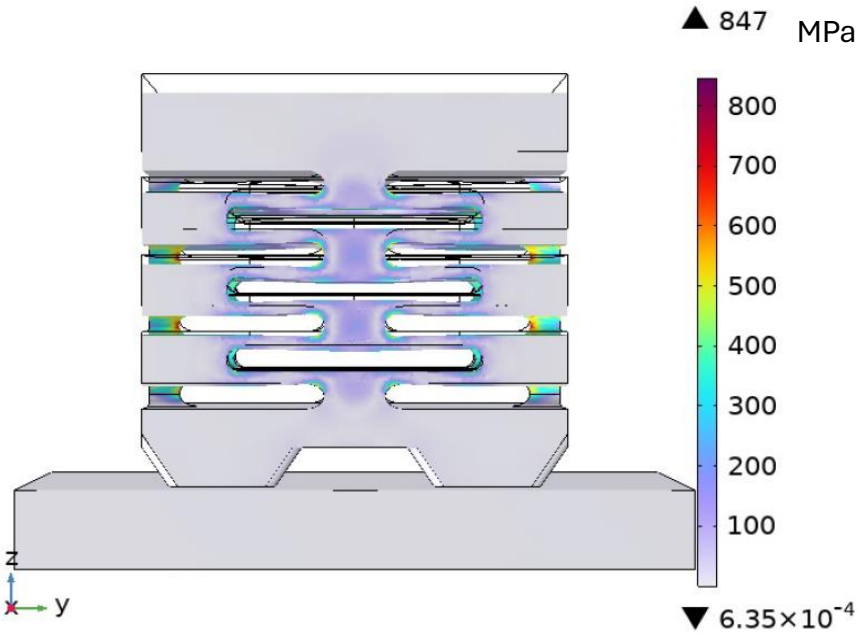


Figure 2.11. The optimized COMSOL Multiphysics simulation results of the body stress (MPa) (with *F*) with initial dataset edges (without *F*).

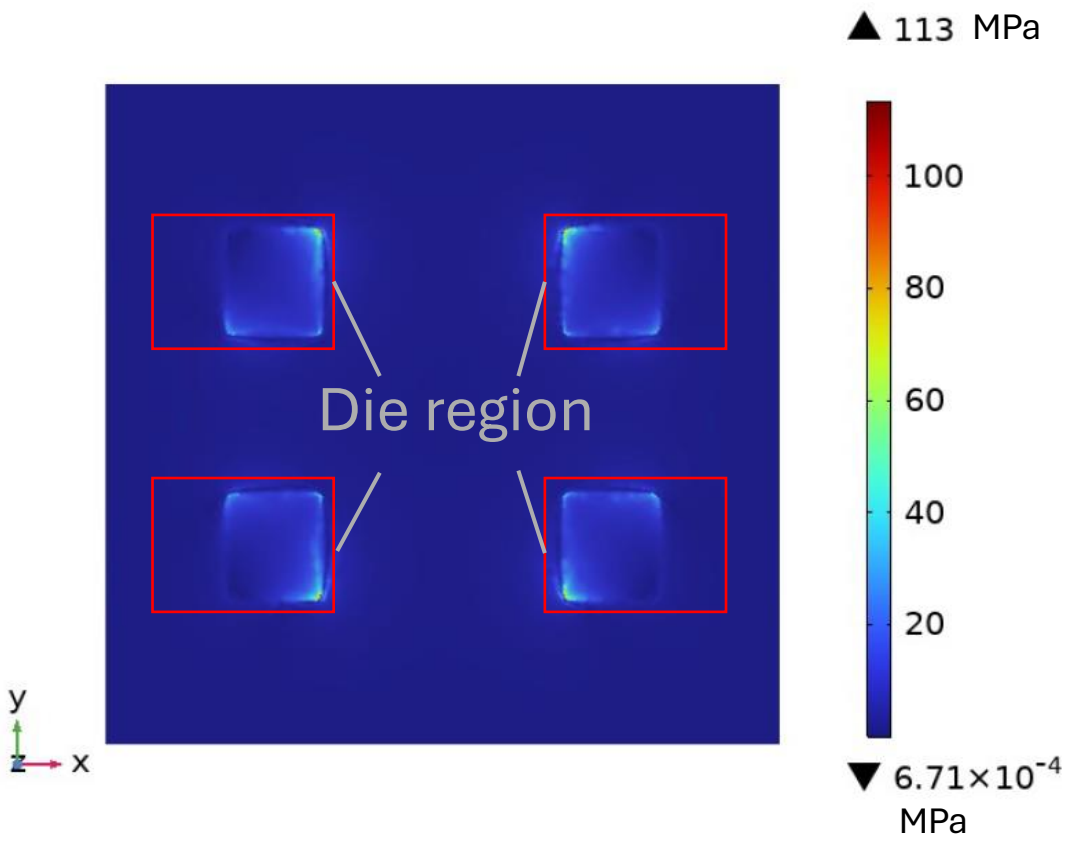


Figure 2.12. The proposed MS COMSOL Multiphysics pressure distribution results (MPa) across the transistor dies (with *F*).

between the surfaces of the current path and the module. The dry contact surfaces can further increase the electrical and magnetic field losses in the DS module, which not only impacts the efficiency of the DS module but also its reliability and robustness. The DS module, introduced in the previous chapter, has been built using Computer-Aided-Design (CAD) tools and it is depicted in Figure 2.12. This model is engineered to align with the optimized MS in terms of the design objectives, and it is aimed to meet the specific application demands. The model employs CDM 168204 DSs, and a copper current path is integrated in the module's structure to ensure a continuous flow of electrical current. The fundamental goal of this detailed DS module design analysis and comparative study is to pinpoint the superiority and limitations of each design strategy.

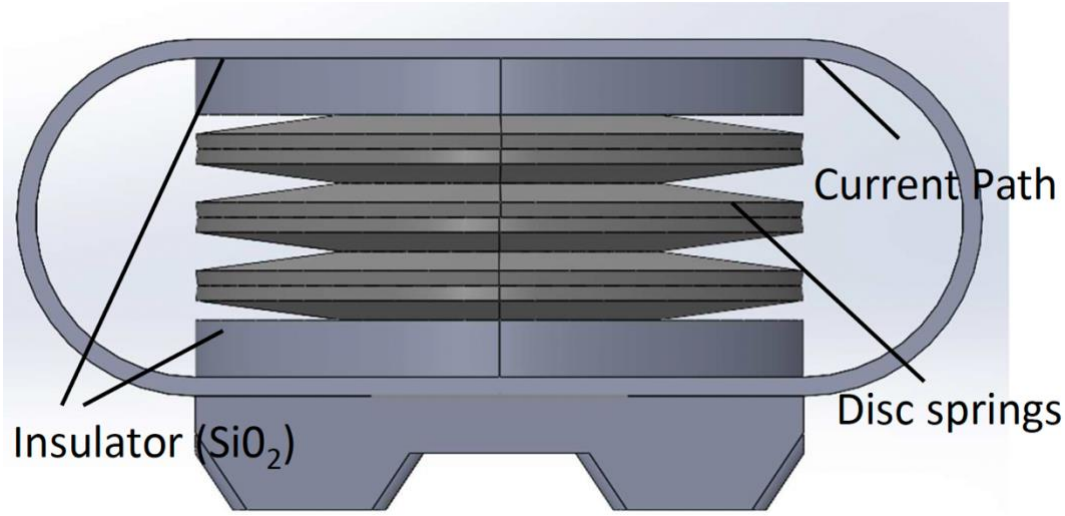


Figure 2.13. The DS module modeled in CAD tools.

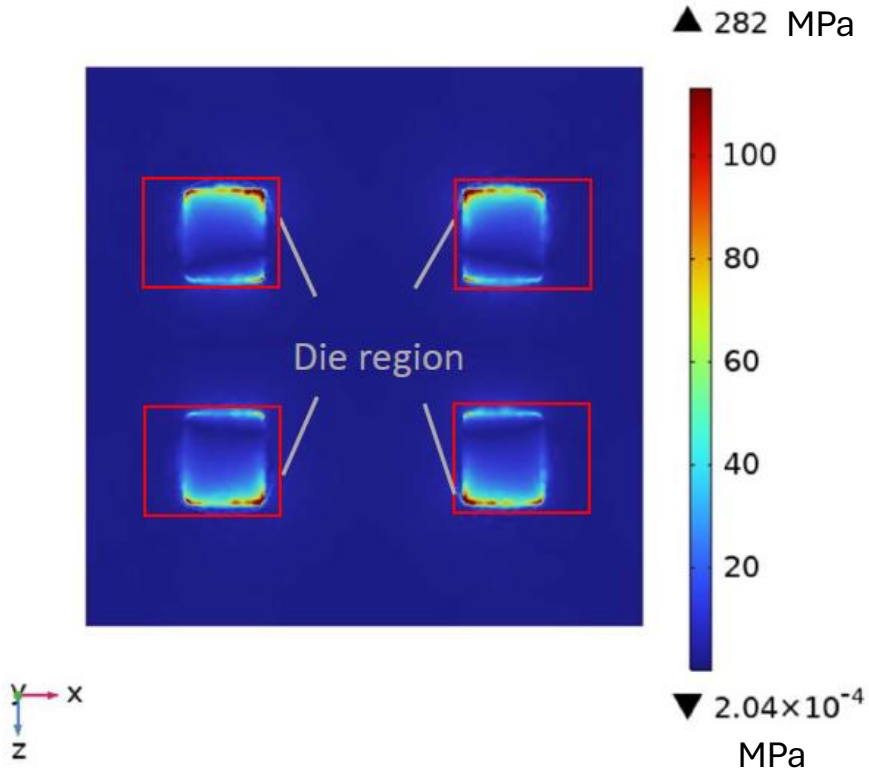


Figure 2.14. The modeled DS module COMSOL Multiphysics pressure distribution results (MPa) across the transistor dies (with *F*).

Insulating block within the DS module aims to interrupt the flow of current through the DS stack and direct the current through the current path, effectively reducing the

resistive losses. Nonetheless, the parasitic inductance of the DS module is comparatively higher than in the MS module due to the insulation. Furthermore, the pressure distribution across the transistor dies when using the DS module is illustrated in Figure 2.13, and it is compared with the distribution shown in Figure 2.11 for the MS module. It has been observed that the maximum pressure applied on the transistor dies is greater in the DS module than in the MS module when the same external force is applied. Hence, the MS design achieves a more uniform pressure distribution compared to the DS module, which not only enhances the robustness of the MS design but also makes it a more reliable choice in practical applications.

During the design phase of spring modules, it is critical to take into account the thermal resistance factor. Modules with higher thermal resistance may require cost-intensive cooling systems to dissipate the heat generated during operation. The proposed MS design aims to significantly reduce thermal resistance and to increase heat dissipation through a unified single-module structure. On the other hand, the DSs within the traditional DS design allow heat to transfer mainly around the edges of the discs, which results in increased thermal resistance. The heat management of both the DS and MS modules have been thoroughly analyzed via thermal FEA simulations. A constant heat source has been added to each transistor die region to simulate steady-state temperature distribution. Both the upper and lower surfaces of the modules have been conditioned to remain constant at 70 °C to replicate the effect of a cooling mechanism. Additionally, the modules are simulated as they have been sintered into a singular piece, which is consistent with the MS module. However, the DS module consists of multiple dry-contact regions, complicating their representation in FEA simulations due to surface roughness.

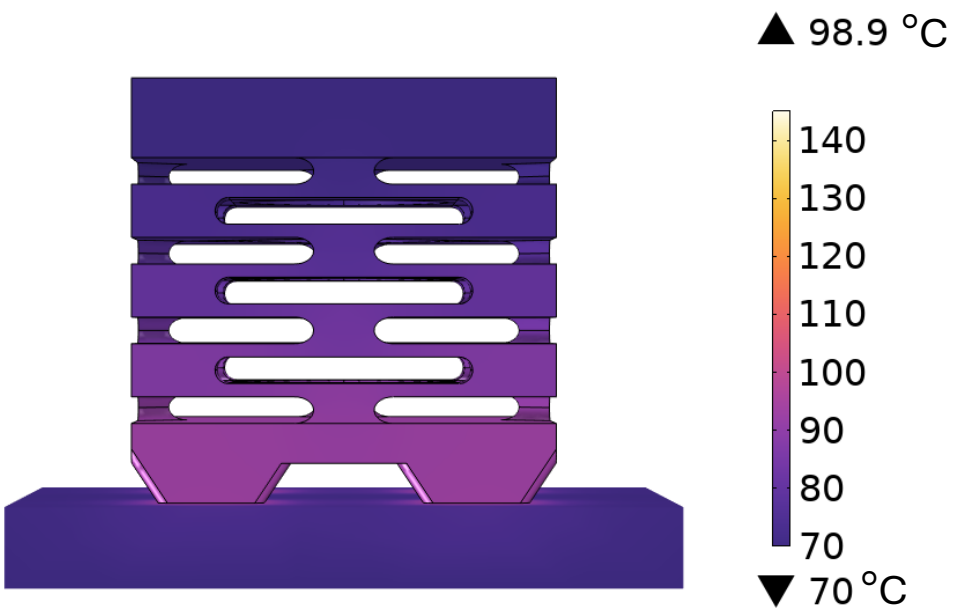


Figure 2.15. Temperature Distribution of the optimized MS body.

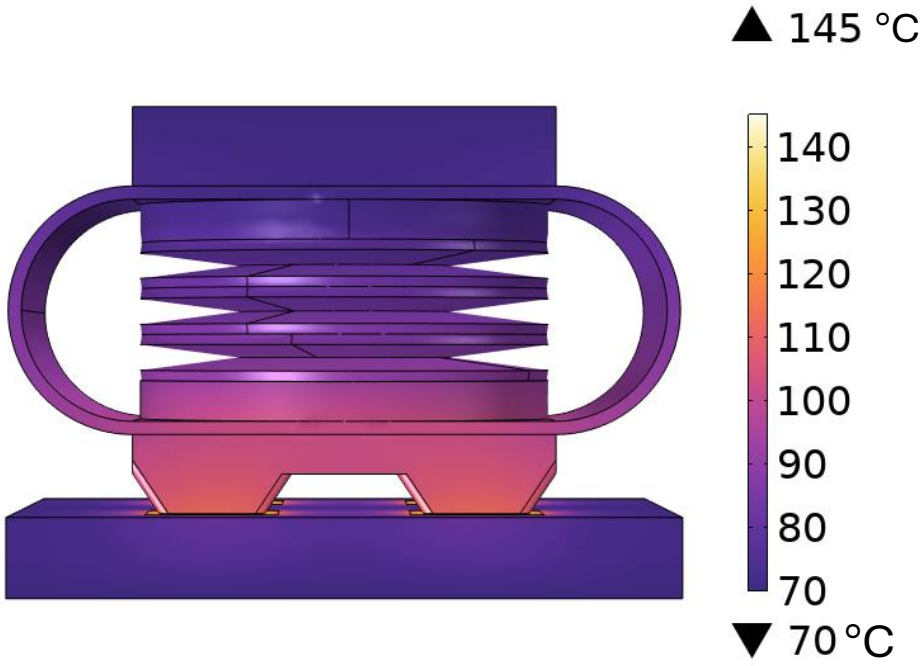


Figure 2.16. Temperature distribution of the modeled DS body.

The temperature distribution within the MS module (Figure 2.13), within the DS module (Figure 2.14), across the transistor dies within the MS module (Figure 2.15) and

the DS module (Figure 2.16) have been illustrated to compare both modules' thermal performance. A uniform temperature scale is used throughout the thermal FEA simulations. The MS module proposes a lower temperature increase due to the slits that increase the cooling surface area. Moreover, the MS reduces the peak die temperature by 46.1 °C. This reduction represents the significantly lower thermal resistance for the MS module, which improves the reliability of the PP module and decreases failure rate.

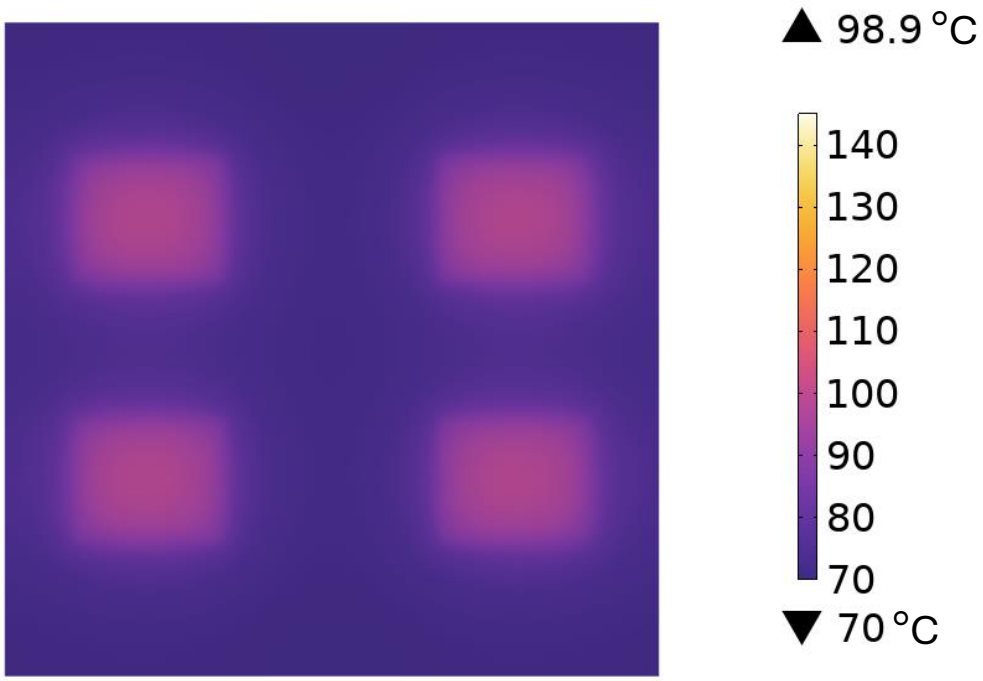


Figure 2.17. Temperature Distribution across the transistor dies utilizing the proposed MS.

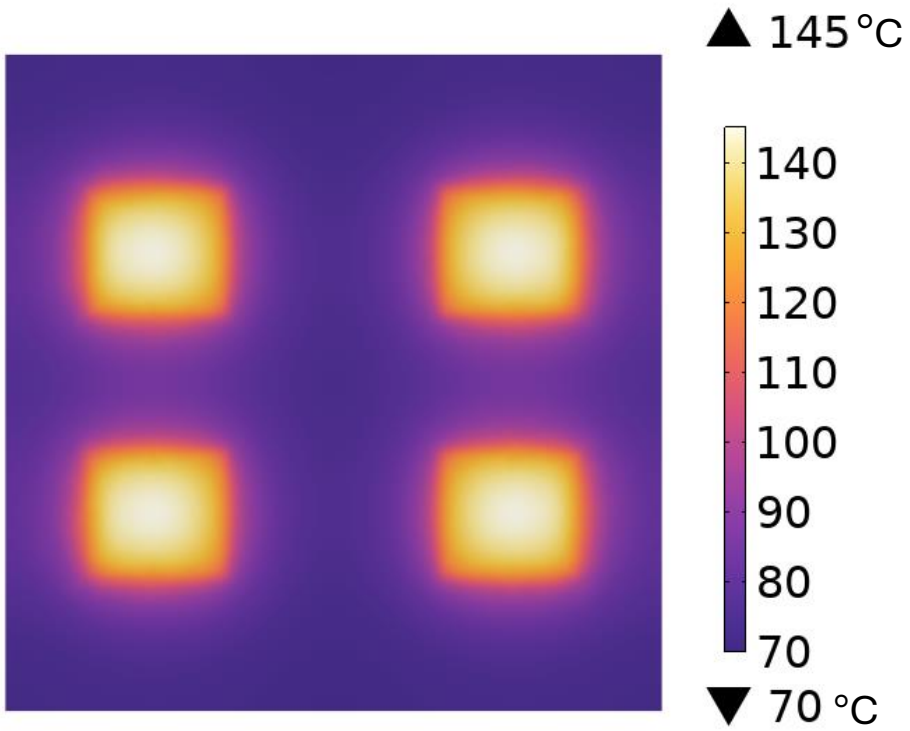


Figure 2.18. Temperature Distribution across the transistor dies utilizing the modelled DS.

CHAPTER 3. EXPERIMENTAL RESULTS OF MANUFACTURED MS DESIGN

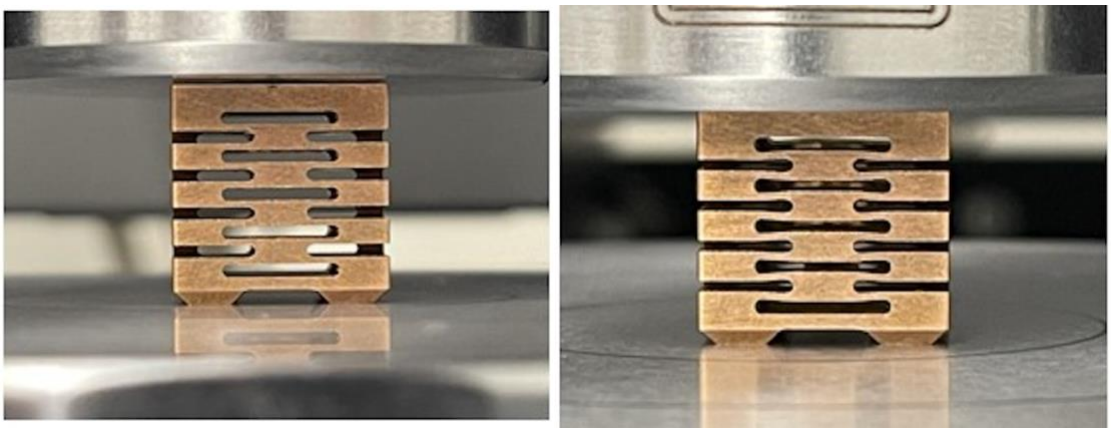
The proposed MS design is still in the pre-production phase. However, a specific design within the set range of design variables has been selected. An order for five prototypes has been placed for the purpose of conducting the experimental tests. The main goal of this chapter is to check the precision of the simulation predictions by comparing them with real-world experimental data. Two distinct experimental tests have been carried out to achieve this goal. Initially, a mechanical test has been performed to measure the deflection data when varying the applied force. This test is crucial to understand the operational limits of the manufactured MS while being still functional. It also allows for the behavior of the MS under real-world mechanic loads to be compared with what has been expected from COMSOL simulations, specifically investigating how it reacts to mechanical stress. Secondly, an electrical test has been carried out to determine the resistive and inductive characteristics of the MS design. Assessing the electrical performance is essential for gauging the effect of the MS design on the electrical performance of the PP module. This approach offers to check if the computer simulations have been precise in forecasting the design's electrical behavior. Throughout these experimental testing, insight into how the MS might affect overall PP module efficiency and accuracy have been obtained, while validating the simulation outcomes.

Using both simulation and hands-on experimental testing strengths the robustness and real-world applicability of the proposed MS design. It has been ensured by confirming that the predictions made by the COMSOL simulations are correct and by uncovering any useful information that could lead to improvements in the MS design. As a result, the latest

MS design has been developed, and its benefits compared to the DS design have been detailed in the previous subchapters.

3.1 Mechanical testing of the manufactured MS

The mechanical performance of the manufactured MS has been evaluated using Instron 5966, a universal testing machine. Instron 5966 is known for its precision and reliability in the materials testing industry. As highlighted in [19], Instron 5966 is part of a line known for its robust construction and ability to handle a wide range of testing applications. This model is equipped to perform tensile, compression, and bending tests on



(a) (b)

Figure 3.1. The manufactured BeCu MS spring deflection and stress experiments, (a) without and (b) with clamping force.

various materials, making it ideal for assessing the manufactured MS design's mechanical properties. The manufactured MS underwent a series of tests to determine the force required for four distinct deflection thresholds: 0.35 mm, 0.8 mm, 0.9 mm, 1.0 mm. The initial position and the position when the maximum clamping force is applied have been demonstrated in Figures 3.1(a) and 3.1(b), respectively.

The experimental results of deflection for varying applied force have been illustrated in Figure 3.2. Manufacturing imperfections introduced a nonlinear relationship

between the applied force and the deflection for smaller deflection and force values. However, this nonlinearity eventually transitioned into a more predictable, linear behavior as the clamping force is increased. Most importantly, the MS has been confirmed to operate within safe stress limits, with a maximum body stress less than 1035 MPa which is the tensile strength of BeCu. This ensures that the MS can return to its original shape.

Another important result from the mechanical testing is that the force required to achieve a specific amount of deflection in the MS is greater than what has been initially predicted from the simulation results, which means a greater spring constant for the MS in practical applications. For instance, in the COMSOL Multiphysics model, an applied force of 650 N has been predicted to result in a deflection of 1.46 mm. However, the actual deflection of the manufactured MS model was only 0.81 mm. This discrepancy highlights a difference in performance between the simulated predictions and the real-world behavior of the MS under the same loading conditions. Nevertheless, it is possible and encouraged to have increased clamping force that 650 N for the maximum deflection level due to the application requirements. Due to the characteristics of HFPP SiC transistor dies, higher clamping force will reduce the resistive losses across the die until reaching a threshold level.

3.2 Electrical testing of the manufactured MS

The manufactured MS has been equipped at the both ends with aluminum plates to facilitate the measurements of DC resistance ($R_{DC,measured}$) and stray inductance ($L_{S,measured}$) using an RLC meter. The outcomes of these electrical tests confirmed the predictions made by the COMSOL simulations, recording a DC resistance of 191.92 μΩ, and a stray inductance of 6.296 nH. However, it should be kept in mind that possible measurement

errors may exist. These results underscore the MS module's enhanced efficiency when compared to the DS module and highlight its effectiveness in minimizing electrical energy losses. This comparison not only illustrates the MS's superior performance but also verifies the reliability of the simulation methods used in its development process.

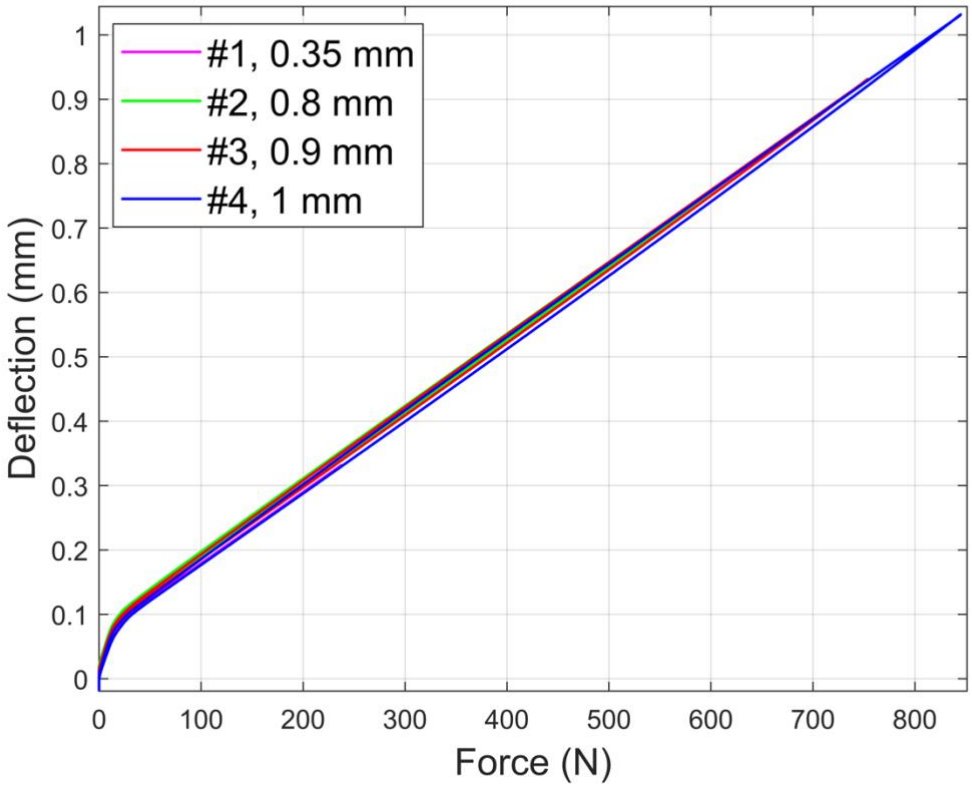


Figure 3.2. Mechanical experiment results of the manufactured MS using four deflection limitation.

CHAPTER 4. CONCLUSION AND FUTURE WORK

The primary objective of this research is to advance the design of HFPP modules that can handle high currents, minimize conduction losses, and operate at high switching frequencies. These types of modules are particularly intended for use in modern MV distribution-grid-scale power converters aimed at improving both the efficiency of power distribution and the resilience of the grid. The implementation of SCFM in series configurations at increased converter voltages is an essential requirement for ensuring reliability. Traditional Si press-pack devices like SCRs, IGCTs, and IGBTSs suffer from inherent limitations in terms of conduction losses and switching frequencies. As a solution to these challenges, the implementation of high-frequency press-pack SiC FET modules have been proposed. The comparison between the traditional PP IGBT modules and the proposed HFPP SiC FET module has been conducted throughout the research process. Refinement and optimization of the proposed design has been achieved by conduction both simulations and experimental testing. The optimization process has focused on increasing maximum switching frequency allowed and on decreasing unwanted electrical losses and noise, thereby potentially enhancing the performance standards of power modules in the industry.

To confirm the accuracy of the simulation results, practical experiments have been carried out on a manufactured MS design point. The experiments include a mechanical test to assess the deflection response under various applied forces, as well as an electrical test to evaluate resistance and inductance values. The research presented in this paper introduces an innovative MS made of beryllium-copper designed to overcome challenges often found in HFPP modules that utilizes DS configurations. High electric resistance and

parasitic inductance, inadequate cooling capabilities are the challenges that have been resolved by the proposed MS design. The structure of the proposed MS includes features such as laser-cut slits, silver-coated transistor legs, and a smoothly polished top surface, all of which contribute to the aim of reducing electrical losses and improving thermal management. Moreover, the MS is designed for a directly sintered to the SiC FET dies via the transistor legs, which enhances both the efficiency and the heat distribution of the PP module. Key contributions of the research encompass the development of the novel MS structure and a design optimization approach aimed to meet precise requirements related to applications in terms of deflection, spring constant, and stress uniformity. This approach ensures that the PP module operates more efficiently by minimizing resistive and inductive losses. The newly proposed HFPP switch cell design, which utilizes the proposed MS design, offers significant improvements over traditional HFPP designs that rely on DS modules. In table 4.1, the enhancements in electrical resistance for both DC and AC alongside a thermal performance parameter, have been detailed. The proposed MS module shows an 82.7% reduction in DC resistance (R_{DC}) when compared to the DS module. Moreover, the proposed MS module features a 77.2% reduction in AC resistance (R_{AC}), which is expected to improve the reliability at high switching frequencies. To evaluate the thermal performance of both the MS and the DS modules, maximum temperature on die region ($T_{max,die}$) has been selected. Maximum temperature across dies is 145 °C for the DS module, whereas it is 98.9 °C for the MS module. This reduction equates to a 31.8 % decrease in the maximum die temperature, thus reducing the thermal resistance of the module.

Table 4.1. Simulation results comparison between DS and MS modules.

DS module	MS module	Change Rate
R_{DC} = 856.1 μΩ	R_{DC} = 148 μΩ	- 82.7 %
R_{AC} = 987.1 μΩ	R_{AC} = 224.5 μΩ	- 77.2 %
$T_{max,die}$ = 145 °C	$T_{max,die}$ = 98.9 °C	- 31.8 %

The implementation of the proposed MS design significantly improves the performance of the proposed HFPP switch cell, making it more effective than traditional DS-based models. Continued investigation and refinement of the Monolithic Spring design are essential to expand our knowledge and to explore potential enhancements that could yield a more efficient and reliable power module for medium-voltage applications. Future research directions may include:

1. The optimized MS may be manufactured and subjected to rigorous testing to compare the results predicted by the COMSOL Multiphysics simulations.
2. It is important to note that the contact boundaries within the DS simulations were not included, leaving room for further detailed Multiphysics simulations in future research. When two flexible surfaces are modeled, the computational demands increase, and the solver often struggles to find a solution [20]. Users need to dedicate significant effort to fine-tune the contact parameters. Such simulations will enable a more accurate representation of DS performance, contributing to the overall enhancement of HFPP module technology.
3. There may be a continuation of the HFPP semiconductor packaging research, which focuses on assessing the quality of sintering, the accuracy of spring constant simulations, the design of gate drivers, and insulation integrity to manage

phenomena like partial discharges, as well as determining the durability of the PP module during repetitive power cycles.

4. Throughout the optimization process, there was a challenge in reducing the spring height without compromising the maximum amount of deflection allowed. Certain applications might demand higher deflection levels. Future iterations of the design may aim to accommodate greater deflection for a more compact design while maintaining the material's elastic property.

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