University of Nebraska - Lincoln
DigitalCommons@University of Nebraska - Lincoln

Library Philosophy and Practice (e-journal) | Libraries at University of Nebraska-Lincoln

Winter 1-31-2021

Phase locked loop using VLSI Technology: A Bibliometric Survey and Future Research Directions

UJWALA KSHIRSAGAR
ujwala.kshirsagar@sitpune.edu.in

Ayushi Kamboj Ms.
Symbiosis International University, ayushi.kamboj.mtech2020@sitpune.edu.in

Follow this and additional works at: https://digitalcommons.unl.edu/libphilprac

 Part of the Electrical and Computer Engineering Commons, and the Library and Information Science Commons

KSHIRSAGAR, UJWALA and Kamboj, Ayushi Ms., "Phase locked loop using VLSI Technology: A Bibliometric Survey and Future Research Directions" (2021). *Library Philosophy and Practice (e-journal)*. 5056.
https://digitalcommons.unl.edu/libphilprac/5056

Phase locked loop using VLSI Technology: A Bibliometric Survey and Future Research Directions

Dr. Ujwala Kshirsagar

Associate professor, Symbiosis Institute of Technology (SIT) affiliated to Symbiosis International (Deemed University), Pune, India, ujwala.kshirsagar@sitpune.edu.in

Ayushi

M-tech ENTC Student, Symbiosis Institute of Technology (SIT) affiliated to Symbiosis International (Deemed University), Pune, India, ayushi.kamboj.mtech2020@sitpune.edu.in

Corresponding author: Ujwala Kshirsagar (kshirsagarujwala9@gmail.com)

Phase locked loop using VLSI Technology: A Bibliometric Survey and Future Research Directions

Ujwala A. Kshirsagar[1], Ayushi[2]

[1]*Associate Professor, Symbiosis Institute of Technology (SIT) affiliated to Symbiosis International (Deemed University), Pune, India,*

ujwala.kshirsagar@sitpune.edu.in

[2]*M-tech ENTC Student, Symbiosis Institute of Technology (SIT) affiliated to Symbiosis International (Deemed University), Pune, India,*

ayushi.kamboj.mtech2020@sitpune.edu.in

Abstract: For the design of high frequency networks power has been one of the most significant specifications. Power usage is therefore one of the most significant challenges to microprocessor design. If we lower the supply voltage, this immediately leads to a decrease in static and dynamic power usage in order to reduce the circuit's power dissipation. Decreasing the voltage of the supply, however, often decreases the circuit's output, which is not reasonable.

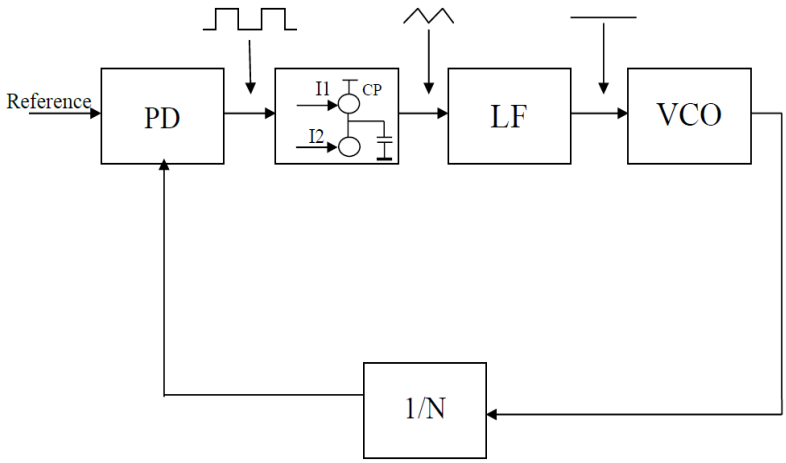
The low power proposed phase locked loop (PLL) is therefore built using microwind 3.1, 45nm CMOS/VLSI technology, which, in practice, at low power, delivers high intensity output. The well-organized (area) architecture for Phase Locked Loop (PLL) with multiple outputs is also planned using microwind 3.1, 45nm CMOS/VLSI technology. At the level of physical detail, Microwind 3.1 facilitates the design and simulation of an integrated circuit. For 45 nm technology, the operating gate length required is 25nm.

Keywords: Phase locked loop, VLSI Technology, Low power, CMOS Technology, Digital Phase locked Loop

1. Introduction

In this review paper we tried to do a survey about what work is done till now from the last one decade in PLL by using CMOS/VLSI Technology. Here we refer the papers from the year 2010 to till date. Basically, it is possible to use a phase locked loop to maintain

a well-defined phase, and thus a frequency relationship between two independent sources of signal.



PD – Phase detector

CP – Charge pump

LF – Loop filter

VCO – Voltage controlled oscillator

Figure1. Block schematic of Phase Locked Loop (PLL) block

The phase detector, low pass filter (loop filter) and a voltage-controlled oscillator are the main components of the Phase Locked Loop (PLL). A low power phased-locked loop with multiple output(s) design and analysis is essentially applied by adjusting the closed loop frequency of the PLL-blocks control system. The output voltage of the Phase Detector equals the phase difference between the output signal from the VCO and the reference signal (Input of Phase detector). Because the input clock and the input signal have a phase change of 90° or (π/2), the output of the phase detector produces normal square oscillations. The performance for other angles is not normal. The phase detector output is the phase error voltage, which, after filtering through the filter of the system, regulates the frequency of the VCO. The ability to perform all PLL functions on a single integrated circuit (IC) has provided a cost-effective, mass manufacturing approach to satisfy market needs.

Sr. No.	Acronyms	Full Form of Acronyms
1.	PLL	Phase Locked Loop
2.	TDC	Time to Digital Converter
3.	PD	Phase Detector
4.	LC	Inductor-Capacitor
5.	LPF	Low Pass Filter
6.	VCO	Voltage Controlled Oscillator
7.	IC	Integrated Chip
8.	Fin	Input Frequency
9.	Fout	Output Frequency
10.	CLKIn	Input Clock
11.	CLKOut	Output Clock
12.	VDD	Supply Voltage
13.	VC	Capacitor Voltage
14.	ASIC/SOC	Application Specific Integrated Chip/ System on Chip
15.	RF	Radio Frequency
16.	SOS	Silicon on Sapphire
17.	DLL	Delayed Phase Locked Loop
18.	FM	Frequency Modulation
19.	RMS	Root mean square
20.	LCO	Local Controlled Oscillator

Figure2. Shows the list of Acronyms

2. Reviews

2.1. Configuration of Low Power PLL Using 45nm Very Large Scale Integrated Technology

- In this article authors Ms. Ujwala A. Belorkar (Kshirsagar) and Dr. S. A. Ladhake describe about a low power PLL using VLSI technology. The Phase Locked Loop is implemented with Microwind 3.1 software using the 45nm VLSI technology process. Hence, at low power, it offers high speed performance. The electronics sector has attained an outstanding growth mostly in previous couple of decades; it's primarily related to development in implementation. To generate a clock

signal, the PLL is then used from a serial string of bits sent without a synchronization clock pulse as a circuit for clock recovery. Basically, a high-frequency oscillator and a filter whose speed differs is employed by PLL. The VCO is related via a phase stabilization mechanism. The most significant building block in PLL is the VCO. The VCO output frequency determines the efficacy of the PLL. It absorbs much of the system's power when we run the VCO at high frequencies. Therefore, in order to minimize power usage, we need to concentrate further on this block. The analysis and design of the low power consumption PLL using 45nm VLSI technology is the subject of this article. In communication applications such as frequency synthesis, PLLs are widely used for missile detection, although noise stability is a significant aspect that can be studied with filter components.

- **Experimental Results:** In the findings, we got a higher efficiency of proposed PLL circuit, and stable frequency vs time simulation as well. The greatest drawback to this PLL type is that the supply and temperature are having a significant effect on the reliability of the oscillation. If we vary the current of the unit, the oscillation frequency is adjusted accordingly. And such oscillations are hardly used for frequency generators with high stability.

2.2. 2.45 GHz gilbert mixer using 45 nm CMOS technology

In this paper authors *Ms. Ujwala A. Belorkar, and **Dr. S.A. Ladhake, *Member, IEEE, and* * * * Dr. Sujata N. Kale describe about a transistorized circuit used as an analog multiplier and frequency mixer is the Gilbert mixer. The output current is an accurate multiplication of the (differential) base currents of both inputs, one of the most significant benefits of this type of circuit. Its balanced operation as a mixer is to cancel out several unnecessary mixing materials, leading to a polished output. Most of the attempts are made using Very Large-Scale Integrated Technology (VLSI) technologies to design Gilbert cells. The Gilbert Mixer is developed by the author with microwind3.1 software using 45nm technology. Microwind 3.1 software helps an integrated circuit to be engineered and replicated at the level of physical definition. In integrated circuit applications, the doubly balanced bipolar Gilbert cell mixer is preferred. Now a day's power becomes the one of the most significant parameters when designing every circuit for multiple frequencies. To implement mixer for

modern communication engineering applications in low power dissipation, high strength and low jitter rate, the Proposed Gilbert mixer was also useful in frequency conversion in communication.

2.3. Effective Region 3.3GHz PLL with four multiple output using 45nm VLSI Technology

The area effective and low power architecture for phase locked loop with four outputs was proposed in this article by authors Ms. Ujwala A. Belorkar (Kshirsagar) and Dr. S. Ladhake. Using CMOS/VLSI technologies, efforts were undertaken to develop multiple outputs, low power Phased Locked Loop. VLSI technology consists of the processing of chips, parameters of real time circuits, circuit switching and building blocks of configuration. The area-efficient phased locked loop is equipped with microwind 3.1 software using 45nm CMOS/VLSI technology. According to lambda-based law, the effective gate length of 45nm technology is half of the 25nm technology. In this article, the author suggested a low power (0.211milliwatt) PLL with four multiple outputs at different frequencies. Because multiple PLL outputs provide multiple clock generation, it is therefore important to build the low-power consumption, high-stability and low-jitter PLL that is needed for modern communication applications.

In this article, the author presents a design aspect using Very Large Scale Integrated Technology (VLSI) technology for the design of low power PLL with low power performance. The region effective low power phased locked loop design process starts with a defined set of specifications, if these are not met, then design needs to be strengthened. This paper uses 45nm CMOS/VLSI technologies in microwind 3.1 software to develop the proposed PLL.

Basically, the PLL consists of three components: phase detector, low pass filter, and VCO. The simple PLL output is 1x for multiple PLL outputs, the 90 ° phase shift output is produced by using the delay circuits or logic gates that provide low power high speed efficiency. In this article, the author suggested four multiple outputs, which can be found in multiphase clocking circuits, such as 1x, 2x, 4x and 8x. This type of PLL can be used for multi-channelling communication systems therefore, which provides a very fast multitasking communication. Therefore, with four multiple outputs, the author is able to design efficient, low power and optimum PLL.

2.4. A 2 GHz fractional-n digital PLL

A low-power, noise-shaping time to digital converter (TDC) is defined in this article by authors Dong-Woo Jee et al., implementation represents a fractional N-digital PLL. In

this paper author also said that the $\Delta\sum$ architecture of TDC basically handles a large number of input range hence, enhancing the linearity and resolution transfer efficiency. The Digital PLL is fabricated by using 0.13μm Very Large-Scale Integrated Technology. Without distortion of signal information, the maximum range of TDC input is transformed to a modulated stream of single bit by using the basic switch-based delta modulated structure which is connected in cascade with a charge pump modulator. By minimizing the delay amount in TDC, signal transfer function (STF) bandwidth and noise transfer function (NTF) pass band gain can be effectively equipped to reshape the diagnostic and statistical manual of mental disorder (DSM) noises and make them minimal, so that even with a wide bandwidth, By using a loop filter, they can be easily winnow out.

2.5. Jitter injection-locked PLL

In this paper authors Zhang, H., Narayanan, A.T., Herdian, H., Liu, B., Wang, Y., Shirane, A., Okada, K addresses an injection-locked PLL that actually uses the RC pulse generator calibration and injected timing to enhance the jitter and correlation stimulation performance. An ultra low power oscillator is therefore intended to achieve low power consumption of PLL. The researcher of this article states that the integrated chip is developed using 65nm CMOS technology covering an area of 0.025mm^2. The injection-locked PLL attain 70fsrms integrated jitter and -66dBc reference spurs and consumes the 0.2mW power, which is equivalent to -270dB figure of merit (FoM) at output frequency of 2.4GHz. The outcome we get in this paper is that it fits for the injection ratio spectrum from 3 to 24 for the 2.2GHz to 2.6GHz frequency range.

2.6. A low power, low jitter, lc phase locked loop

In this article authors have introduced a low-power, low jitter inductor capacitor (LC) PLL. It is planned and produced using the 0.25mm Silicon-on-Sapphire CMOS commercial process. The estimated tuning range varies from 4.6GHz to 5.0GHz. Therefore, the squandering of power at the centre frequency is 111mW. In the laboratory research, an inductor capacitor (LC) PLL manufactured with industrial 0.25 mm silicon on sapphire CMOS technology. The problem related to the limited tuning range was evaluated and identified. After narrow tuning range problem was fixed, this inductor-capacitor (LC) the Phase Locked Loop (PLL) will be included in our upcoming 10 Gbps serialized clock unit.

2.7. Low power &high speed PLL frequency synthesizer

In this paper author explained about the importance of power consumption in communication systems. Basically, PLL is an adaptable tool which is often used in the synthesis of frequency. The Dynamic CMOS logic is the fastest logic among all the CMOS logic family. The DSCH CAD method for the development of logical circuits is used here and 120nm technology is used to simulate parametric analysis. The power consumption was lowered to 0.13 mW in the complex CMOS/VLSI logic PLL, resulting in an improvement in speed to 0.50 GHz. Therefore, because of the decrease in power dissipation, the existing CMOS dynamic PLL functioned at a very high speed. The number of transistors is decreased in the design because of the reduction in chip area. It can be used in various communication devices, such as the frequency modulation (FM) transmitter and the circuit for frequency synthesis.

2.8. Invention of delayed-locked loops with low power using two 130nm technology

In this paper, authors M. Firlej et al., describe the performances of various low power Delay Locked Loop prototypes for their use in particle physics were evaluated. Basically, in two different 130nm CMOS technologies, the DLL was developed as system A and system B, providing the opportunity to differentiate these two CMOS processes. The DLL's jitter duration depends on the chosen output process and varies from 2.5ps to 12.1 ps (RMS). It is proved experimentally that power consumption, commonly at 40MHz input, is very low at about 0.7mW. 680μm-210μm and 430μm-190μm are occupied by the DLL prototype, designed in system A and system B. The author has stated that the proposed DLL is relative to other designs have smallest area and the ratio of power to frequency in the suggested DLL is the least.

2.9. Diverse range of phase-locked loop ultra-low-power with automatic frequency setting using 130 nm CMOS data serialization technology

The layout and analysis result of a section discusses the optimal range of frequency and ultra low power Phase Locked Loop. Basically, the PLL was developed using 130nm CMOS technology. In the feedback loop of PLL, several factors were included in this division in order to facilitate the introduction of numerous data serialization schemes. The PLL was basically configured with automated VCO mode switching and stimulated due to some limitations of the SLVS interface for a frequency range of 30MHz-3GHz. The analysis was carried at 1.3 GHz and the accurate reporting was investigated intensively and concluded that power consumption is very low at 1 GHz, around 0.7 mW. The proposed PLL has indeed been successfully applied in the 6-bit and 10-bit multichannel

reading process analog to digital converter (ADC) application specifics integrated chip (ASICs). Basically, it is planned to use the proposed PLL for much higher data rates.

2.10. Wider tunning range frequency synthesis of a 1.25-20GHz

The propose circuit is implemented using CMOS 55nm technology. The frequency doubler improves its power and region performance using 10 GHz phase locked loop to 20GHz frequency. The 10GHz basic signal and its second harmonic at 20GHz generated using an integer-N PLL and a mixed frequency doubler, respectively. By using VLSI/CMOS 55nm technology, the frequency synthesizer was designed and deployed. The doublers consume 40.08mW power when power supply is 1.2V and it is among the recorded literature's lowest power usage.

2.11. DSP channel engine to activate theta phase-locked for brain simulation using 216nWatt

The neural theta oscillation phase for phase-locked loop triggering simulation analysis is predicted for the first time by a chip and an algorithm by authors Alzuhair, A., Marković, D. Dependent on data recorded from the human hippocampus, the performance judge or estimation achieve elevated correctness and efficacy in the target. Although architecture intersperses channel-depth configuration, relative to single-channel design, 41 percent energy and 58 percent space are obtained and saved. The author effectively specifies that the power dissipation of the 32-channel integrated chip is 216nW per channel and inhabits a central region of 0.011mm2 per channel. This is aimed to use the low-power 40nm CMOS technology suitable for implantable devices.

2.12. design and analysis of the jitter and power dissipation differential multiphase DLL

The author specifies the optimization of power in delay locked loop (DLL). The key aim of the analysis was to design low-power consumption, less locked time and less circuit jitter. The time period of the signal becomes very small as we increase the clock frequency thus, the amount of jitter in the system can now be permitted. The model was developed and stimulated by the operating frequency spectrum from 100MHz to 1GHz using 90nm CMOS/VLSI technology.

2.13. Scalable bang bang phase locked loop based integrated sensor interfaces

A description of the time-based sensor interface in this paper is given by the Bang Bang Phase Locked Loop-based sensor to digital converter. Low voltage prototypes, durable and extremely scalable, and low power consumption are the result of the digital frequency-based sensor deployment. With three different test chips, this has been

confirmed. The first chip is designed using the 130nm CMOS technology and the suggested design enables one to scale down the power supply to 0.3V. Using 130nm CMOS technology, the second chip implementation shows the robustness of the supply voltage and temperature variations. A fully digital configuration of the sensor with a capacitive sensor in carbon-based nanotechnology is implemented in the third or final test chip.

2.14. Deployment of low power phase-locked-locked loop and PLLl-based serial transceiver

The proposed circuit designed and fabricated by authors Feng, Y., Chen, J., You, Y., Tang, Y., Fan, Q., Zuo, Z., Pendyala, P., Gong, D., Liu, T., Ye, J. by using 0.35µm CMOS/VLSI technology. The proposed PLL generates the clock signal in the band of frequency from 380MHz to 1.1GHz. The power consumption of the proposed PLL is 4.5mW at 1GHz. The proposed PLL transceiver has been verified in the 600-950MHz frequency range. Data transfer between the transmitter and the receiver was tested at a rate of 600 Mbps. A simple and basic protocol is presented for such a future system of transmission.

2.15. Low phase noise lc oscillator analysis and design for sub-mw pll-free biomedical receivers

This article introduces the idea of a low power phase noise inductor capacitor (LC) oscillator for a phase locked loop free receiver. Using the 180nm CMOS/VLSI technology, the proposed local control oscillator (LCO) has been developed. Therefore, the results shows that when the supply voltage was 1.8V, the power consumption in local control oscillator (LCO) was 140µW, which basically corresponds to the results of the previous layout simulation. Outcomes often signify that in PLL remarkable power reduction while the bit error rate (BER) achieves less than 10^-4 at a data rate of 200kb/s, which is good for several of the communication with the bio signal.

Bibliometric Analysis of Phase Locked Loop

This section explains briefly various bibliometric analyses done on Phase Locked Loop (PLL) for different applications. The required database is taken from Scopus. The main aim of this study is to understand the amount of work done on Phased Locked Loop, the scope of work, and to find the best resources for PLL design.

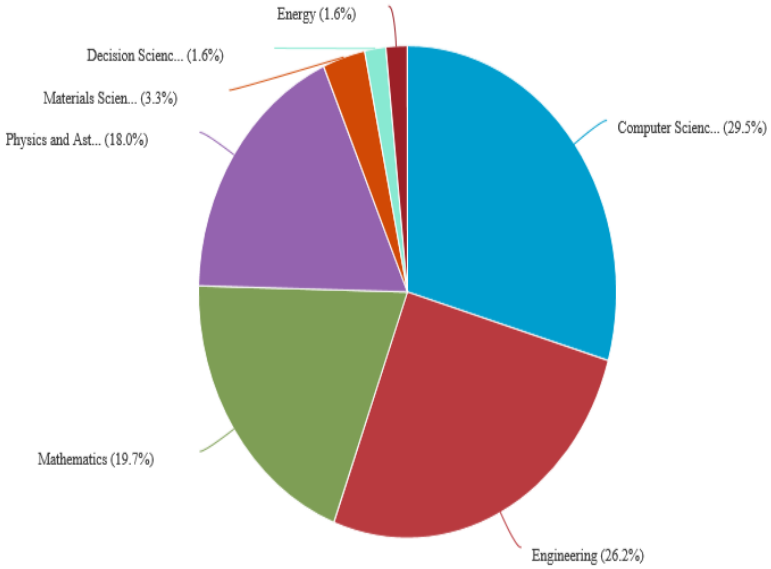


Figure3. Shows the documents by subject area

In Figure 3 Pie Chart shows the documents published by particular subject area. In the pie chart it shows that in area of engineering 26.2 % of total documents published. In the area of computer science 29.5 total documents published in the last one decade, while in the area of mathematics 19.7% of total documents published and for physics & art 18% of documents published, for material science 3.3% of total documents published. The data is taken from Scopus. Here we have done this bibliometric analysis in the period of 2010 to 2020.

In figure 4 the graph shows the number of documents published on PLL per year. In the starting or in 2010 the graph is at 1 then start decreasing reach to zero in the year of 2011. It shows that no document was published in the year 2011. Then again graph start increasing and reach to 5 in the year 2012, therefore it shows that in the year of 2012 total 5 papers are published. Then the graph decreases again in the year 2013, so the number of documents published in 2013 is 2. As the curve is in the form of zigzag, it shows that it did not remain constant. In 2014 curve is increment by one and reaches to 3, after that in the year of 2015 the curve is decrement by 1 and reach to 2 which shows that number of documents published in the year of 2015 is 2. In 2016 the curve reaches to 5 therefore, it shows that the number of documents published in this year is 5. In the year of 2017 again it shows decreasing slope and number of documents published in this year is 2. In the year of 2018 number of documents published is 4 and after that slope is decreasing therefore, it shows that number of documents published in 2019 is 4. The curve

is still decreasing in 2020 and shows that the number of published documents in 2020 is 2. The graph is different from year to year, as we can see. The maximum number of published documents per year is 5, published in 2012, 2106, 2108, and the minimum number of published documents per year is zero (0), published in 2011.

In figure 5 the pie chart shows the document by type published for PLL. Here in the pie chart, it shows that 58.1% conference paper are published for Phased locked loop up to 2020 and 38.7% of article published in this domain and 3.2% conference review paper. Here we have done the bibliometric survey for 10 years from 2010 to 2020. And the complete information is taken from the Scopus.

In the figure6 we compare the documents count up to 10 countries. The whole data is taken from the Scopus and here we have done the bibliometric survey for last 1 decade from 2010 to 2020. This figure proves that the highest numbers of documents are published by India which is 12 followed by Poland and United States.

The graph in Figure 7 explains the number of documents that the author has published. A bibliometric survey of the number of documents published by the author was conducted here. Whole data is taken from the Scopus and we did a complete bibliometric survey of last one decade. The contribution of the top ten authors in the area of Phase Locked Loop is summarized in figure7 and table1. Firlej.M. and Idzik.M has published a maximum number of documents which are 4 documents followed by Firotuski, T. and Liu, T. with a count of 3 documents.

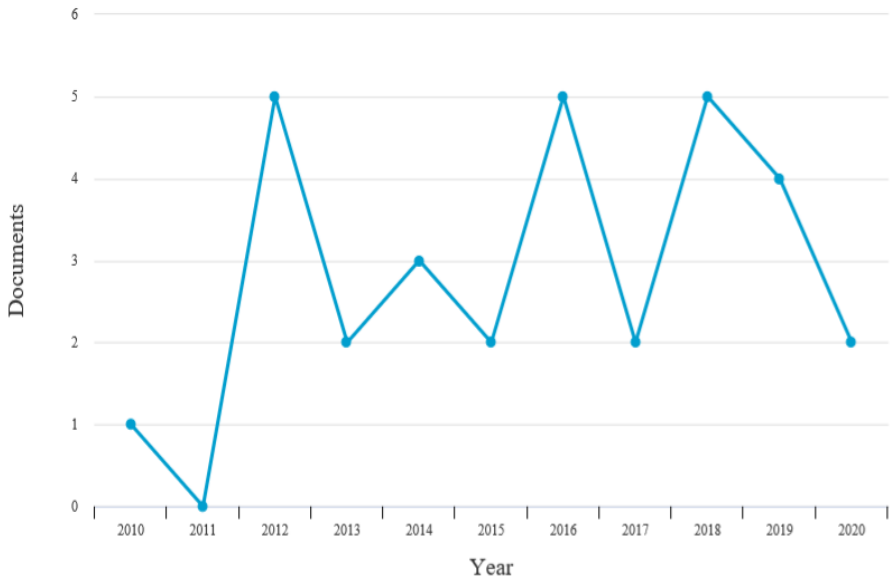


Figure 4. Shows the Documents by year

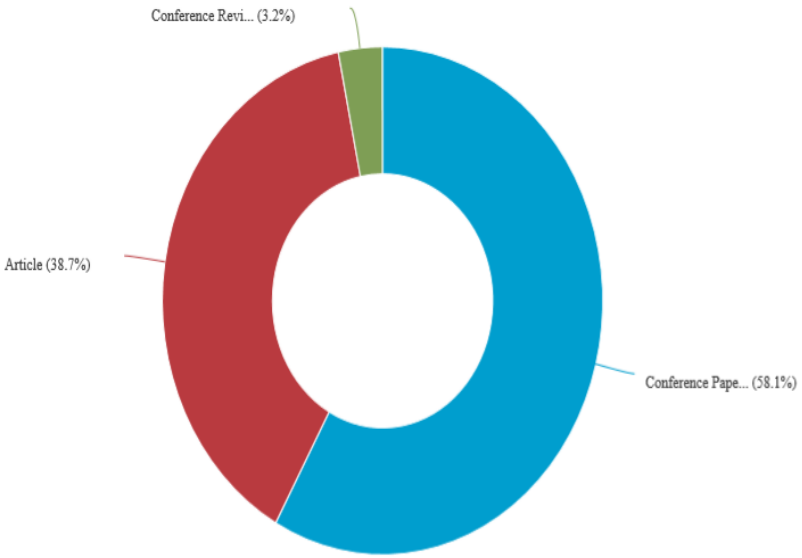


Figure5. Shows the Document by Type

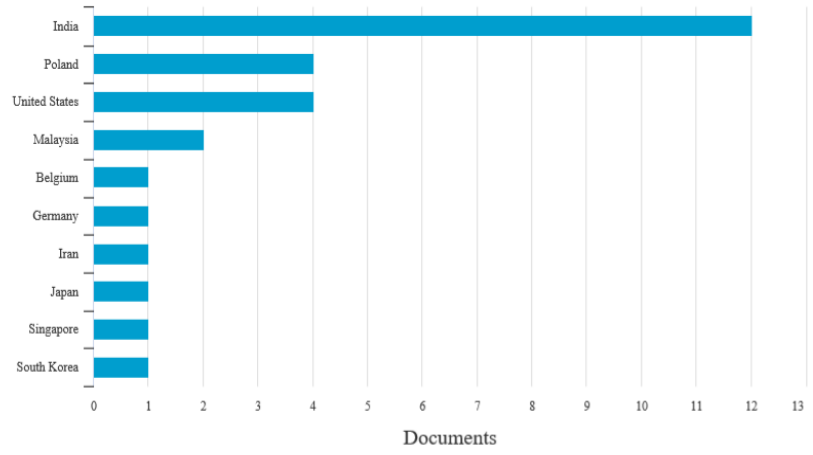


Figure6. Shows the Documents published by country or territory

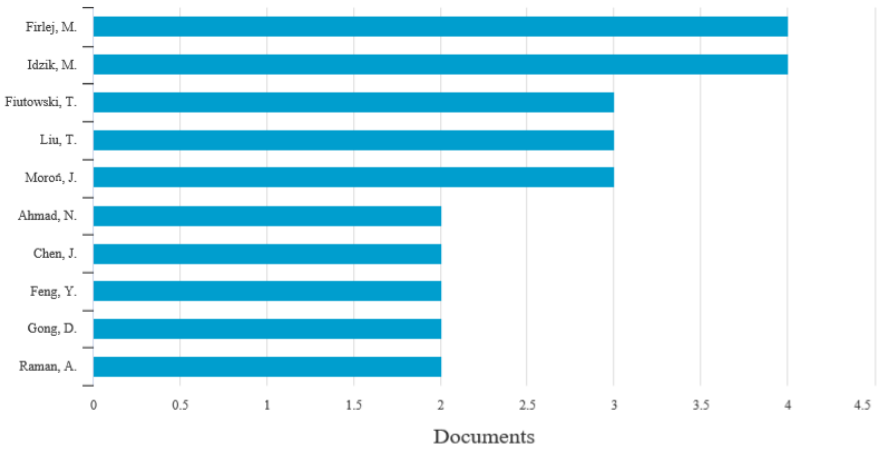


Figure7. The bar chart of research contribution by top ten authors

Figure 8 is the bar chart of documents published by top universities in the field of Phase Locked Loop and the corresponding table is shown in table 2. It shows that University AGH University of Science & Technology is the leading university in Phase Locked Loop design. As per the database of Scopus of last 10 year, 31 universities from all over the world have given their valuable contribution to the research area of the Phase Locked Loop.

Table1. Details of number of documents published by top ten authors

Sr. No.	Author Name	No. Of documents published
1	Firlej.M. a	4
2	Idzik.M	4
3	Firotuski, T	3
4	Liu, T	3
5	Moroa, J.	3
6	Ahmad, N.	2
7	Chen, J.	2
8	Feng, Y.	2
9	Gong, D	2
10	Raman, A	2

Table3 provides the information of the top five documents that are highly cited in the field of Phase Locked Loop (PLL). All documents are taken from the Scopus. The document of Jee, D.-W., Seo, Y.-H., Park, H.-J., Sim, J.-Y. the highest cited document which is cited by count of 31 and followed by the document of Hoppner, S., Eisenreich, H., Henker, S., (...), Ellguth, G., Schuffny, R. Which is cited by 19. The document of Zhang, H., Narayanan, A.T., Herdian, H., (...), Shirane, A., Okada, K. Is at third place which is cited by 5 and followed by the document of Liu, T. which is cited by 5. And the document of the Sreehari, P., Devulapalli, P., Kewale, D. Is at position 5 which is cited by 4.

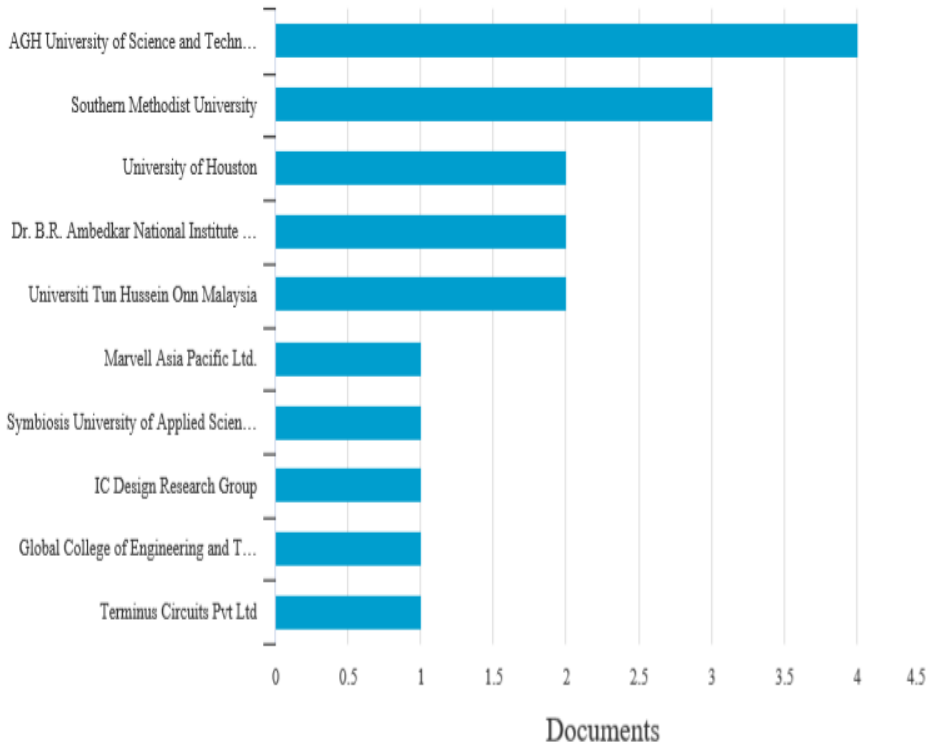


Figure8. Bar chart of the number of papers issued by the top ten universities

Table2 Number of documents from the top ten universities published

Sr. No.	University Name	No. of paper published
1	AGH University of science and technology	4
2	Sothern Methodist University	3
3	University of Houston	2
4	Dr. B. R. Ambedkar National Institute	2
5	University Onn Hussein Onn Malaysia	2
6	Marvell Asia pacific Ltd.	1
7	Symbiosis University of applied science	1
8	IC design research group	1
9	Global college of Engineering and Technology	1
10	Terminus circuits Pvt. Ltd.	1

Table3. Details of top five highly cited documents

Sr. No.	Document Title	Authors	Year	Source	Citation Count
1.	A 2 GHz fractional-N digital PLL with 1b noise moulding TDC	Jee, D.-W., Seo, Y.-H., Park, H.-J., Sim, J.-Y.	2012	IEEE Journal of Solid-State Circuits 47(4),6157640, pp. 875-883	31
2.	A compact clock generator for heterogeneous GALS MPSoCs	Hoppner, S., Eisenreich, H., Henker, S., (...), Ellguth, G., Schuffny, R.	2013	IEEE Transactions on Very Large-Scale Integration (VLSI) Systems 21(3),6166353, pp. 566-570	19
3.	Using De-Sensitized SSPD-Based Injection-Time Self-Alignment Injection-Locked PLL Achieving -270dB FoM and -66dBc Reference Spur	Zhang, H., Narayanan, A.T., Herdian, H., (...), Shirane, A., Okada, K.	2019	IEEE Symposium on VLSI Circuits, Digest of Technical Papers 2019-June,8778059, pp. C38-C39	5
4.	A low power, low jitter, LC phase locked loop of 4.9-GHz	Liu, T.	2010	Journal of Instrumentation 5(12),C12045	5
5.	Power optimized PLL implementation in 180nm CMOS technology	Sreehari, P., Devulapalli, P., Kewale, D., Asbe, O., Prasad, K.S.R.K.	2014	18th International Symposium on VLSI Design and Test, VDAT 2014 6881065	4

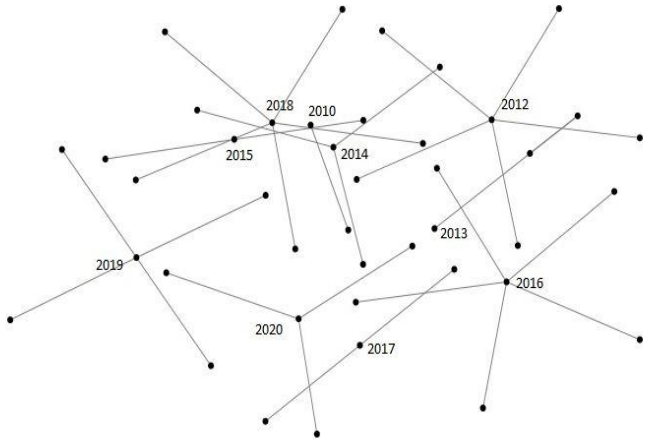


Figure9. Cluster of the publishing year and title of the paper

As you can see figure9 represent the cluster of the publishing year and the title of the paper published. The above graph is designed by using the software NodeXL. So from the above the figure, you can see that maximum publication was done in 2012 followed by 2016 and 2018 whereas minimum publication was done in 2013 and 2017.

3. Future Research Direction

In accordance with the characteristics of CMOS mixers suitable for RF (radio frequency) receivers, the problem is to reinvent a structure that would be both convenient in relative to the number of transistors in the signal path and, at almost the same time, to maintain a consistent port to port isolation. So, the future scope in this field is to focus on the circuit architecture, to resolve this issue. The first edition of ultra low power phase locked loop has already been developed, created and successfully manufactured. Use only a fraction of the frequency band of the PLL for these ASICs, but much higher configuration and transmission rates are planned for the future. A low power 4.9-GHz, low jitter, LC phase locked loop, the determined C-V curve suggests that Even though the measured results vary greatly from the simulated data, the MOSFET-based Varactor continues to act as required. In the future, studies will be carrying out. The outcomes of the estimation rule out the suspicion of inaccuracy. The Varactor model produces a small tuning range.

4. Conclusion

This bibliometric survey is carried out to notify the amount of work done in the field of Phase Locked Loop and its corresponding future scope. Basically, the bibliometric survey provides the details of publication counts in various journals, countries, subject areas, and documents per year. In this paper we did a bibliometric

survey of last 10 years. Evidently, the analysis done on the number of publications per year indicates that there is a still lot of scope in the field of Phase Locked Loop. With this review paper we studied how Phase Locked Loop is changing the world by eliminating the limitations of conventional techniques which are used in designing and fabrication process. The authors also elaborated on Keywords to explain the linkage between different keywords. However, this review paper also provides guideline to new researchers to refer to the research work of various authors done till now according to their number of publications or citation count. Moreover, it proved from the bibliometric analysis that India is leading in the field of Phase Locked Loop followed by Poland. Basically, the bibliometric survey is very useful for new upcoming researchers to find the research gap in the area of Phase Locked Loop.

References:

Abhishek Srivastava* and Maryam Shojaei Baghini "Analysis and Design of Low Phase Noise LC Oscillator for Sub-mW PLL-Free Biomedical Receivers" *2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID)*

Abiri, E., Darabi, "A. CNTFET-based divide-by-N/[N+1] DMFPs using m-GDI method for future generation communication networks" *(2018) Nano Communication Networks, 18*

Alzuhair, A., Marković, D." A 216 nW/channel DSP engine for triggering theta phase-locked brain stimulation" (*2018) 2017 IEEE Biomedical Circuits and Systems Conference, BioCAS 2017 - Proceedings, 2018-January*

Binti Noor Al Amin, F., Ahmad, N., Hairol Jabbar, M. "A Low Power CMOS Phase Frequency Detector in High Frequency PLL System" *(2018) Journal of Physics: Conference Series, 1049*

Dong-Woo Jee, Young-Hun Seo, Hong-June Park, *Member, IEEE*, and Jae-Yoon Sim, *Member, IEEE "*A 2 GHz Fractional-N Digital PLL with 1b Noise Shaping ΔΣ" *IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 47, NO. 4, APRIL 2012*

Fadhilah Binti Noor Al Amin2, *, Nabihah Ahmad1, 2 and M. Hairol Jabbar1,2 "A Low Power CMOS Phase Frequency Detector in High Frequency PLL System" IOP Conf. Series: Journal of Physics: Conf. Series 1049 (2018) 012059 doi :10.1088/1742-6596/1049/1/012059

Feng, Y., Chen, J., You, Y., Tang, Y., Fan, Q., Zuo, Z., Pendyala, P., Gong, D., Liu, T., Ye, J. “A low-power 12.5 Gbps serial link transmitter ASIC for particle detectors in 65nm CMOS” *(2017) Journal of Instrumentation*

Javed S. Gaggatur(B) and Abhishek Chaturvedi *High Speed Circuits Design Group, Terminus Circuits Pvt Ltd, Bangalore 560094, Karnataka, India “*1.25–20GHz Wide Tuning Range Frequency Synthesis for 40-Gb/s SerDes Application”

J. Moron, 1 M. Firlej.M and M. Idzik *Faculty of Physics and Applied Computer Science, AGH University of Science and Technology, A. Mickiewicz 30 Ave., 30-059 Krakow, Poland* “Development of low power Phase-Locked Loop (PLL) and PLL-based serial transceiver” *PUBLISHED: January 26, 2012*

Jelle Van Rethy n , Hans Danneels, Georges Gielen KU Leuven, *Department of EE, Kasteelpark Arenberg 10, 3001 Leuven, BelgiumScalable* “Bang–Bang Phase-Locked-Loop-based integrated sensor interfaces” *published on 25 June 2014*

M. Firlej, 1 T. Fiutowski, M. Idzik, J. Moron and K. Swientek “A 4.9-GHz low power, low jitter, LC phase locked loop” *PUBLISHED BY IOP PUBLISHING FOR SISSA PUBLISHED: December 20, 2010*

M. Firlej,1 T. Fiutowski, M. Idzik, J. Moron and K. Swientek *Faculty of Physics and Applied Computer Science, AGH University of Science and Technology, Al. Mickiewicz 30, Krakow, Poland* “Development of a low power Delay-Locked Loop in two 130nm CMOS technologies”

Ms. Ujwala A. Belorkar and Dr. S.A. Ladhake “AREA EFFICIENT 3.3GHZ PHASE LOCKED LOOP WITH FOUR MULTIPLE OUTPUT USING 45NM VLSI TECHNOLOGY” *International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.1, March 2011*

Ms. Ujwala A. Belorkar and Dr. S.A. Ladhake "DESIGN OF LOW POWER PHASE LOCKED LOOP (PLL) USING 45NM VLSI TECHNOLOGY" *International journal of VLSI design & Communication Systems (VLSICS), Vol.1, No.2, June 2010*

Ms. Ujwala A. Belorkar, and **Dr. S.A. Ladhake, *Member, IEEE, and* * * * Dr. Sujata N. Kale "2.45 GHz Gilbert Mixer Using 45 nm CMOS Technology" *2012 IEEE Business, Engineering & Industrial Applications Colloquium (BEIAC)*

Patri Sreehari Pavankumarsharma Devulapalli Dhananjay Kewale Omkar Asbe KSR Krishna Prasad " POWER *OPTIMIZED PLL IMPLEMENTATION IN 180nm CMOS TECHNOLOGY" Published in 2014 by IEEE*

Ranjan, R., Anurag " Design and analysis of differential multiphase DLL for jitter and power optimization" *(2016) 2015 2nd International Conference on Recent Advances in Engineering and Computational Sciences, RAECS 2015*

1T.Nirm alraj, 25.Radhakrishnan l,2Department of Electronics and Communication Engineering, Srinivasa Ramunujan Centre, SASTRA University, Kumbakonam, Thanjavur, Tamil Nadu , India, 3 Rakesh Kumar Kern, 45.K Pandiyan 3.4Department of Electronics and Communication Engineering, SASTRA University, Thanjavur, Tamil Nadu, India Design of Low Power, "High Speed PLL Frequency synthesizer using Dynamic CMOS VLSI Technology" I*EEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI-20 I7)*

T. Liu1;2 Southern Methodist University, Dallas, Texas 75275, U.S.A." A 4.9-GHz low power, low jitter, LC phase locked loop" *PUBLISHED BY IOP PUBLISHING FOR SISSA December 20, 2010*

You, Y., Chen, J., Feng, Y., Tang, Y., Huang, D., Rui, W., Gong, D., Liu, T., Ye, J. "A 12 GHz low-jitter LC-VCO PLL in 130 nm CMOS" *(2015) Journal of Instrumen*tation

Zhang, H., Narayanan, A.T., Herdian, H., Liu, B., Wang, Y., Shirane, A., Okada, K." 0.2mW 70Fsrms-Jitter Injection-Locked PLL Using De-Sensitized SSPD-Based Injecting-Time Self-Alignment Achieving -270dB FOM and -66dBc Reference Spur" *(2019) IEEE Symposium on VLSI Circuits, Digest of Technical Papers, 2019-Jun*e