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Design of a 1.8V 8-bit 500MSPS Folding-Interpolation CMOS A/D Converter with a Folder Averaging Technique

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Abstract - In this paper, a CMOS analog-to-digital converter (ADC) with an 8-bit 500MSPS at 1.8V is designed. The architecture of the proposed ADC is based on a Folding ADC with a cascaded-folding and a cascaded-interpolation structure. A self-linearized pre-amplifier with source degeneration technique and a folder averaging technique for the high-performance are introduced. Further, a novel auto-switching encoder is also proposed. The chip has been fabricated with 0.18 μm 1-poly 5-metal CMOS technology. The active chip area is 0.79mm² and it consumes about 200mW at 1.8V power supply. The DNL and INL are within $\pm 0.6/\pm 0.6\text{LSB}$, respectively. The measured result of SNDR is 47.05dB.

I. INTRODUCTION

The demands for analog-digital interface are now being increased, due to the development of SOC (System-On-a-Chip) technique. Specially, a high speed and low power A/D Converters (ADC) are key elements in next-generation communication systems. In the field of high speed ADC, full flash type architecture is known to be the most popular one. However, it consumes large chip area and power dissipation, because of many comparators. In order to overcome the drawbacks of the flash type ADC, folding and interpolation

techniques are proposed [1]-[5]. The folding-interpolation type ADC has the advantage of small number of comparators and chip area, while the operating speed is same as that of flash type [2]. For that reason, we propose a low power ADC using folding and interpolation technique for UWB system in this paper.

II. ARCHITECTURE

The block diagram of the proposed ADC is shown in Fig. 1. It consists of the pre-processing block, the coarse ADC (3-bit), the fine ADC (5-bit), and the digital signal processing block including a digital error correction. With the principle of folding-interpolation architecture, the MSB 3-bit and the LSB 5-bit are divided into a coarse ADC and a fine ADC, respectively. Further, the fine ADC is composed of the proposed cascaded-folding cascaded-interpolation for a high-speed operation. The pre-processing block is needed to amplify the analog input signal. A proposed self-linearized pre-amplifier with source degeneration technique is adopted for the high-linearity performance in the pre-processing block. Moreover, in the folding block a folding amplifier with averaging folder are described. Also, we introduced a novel auto-switching encoder for the efficient digital processing.

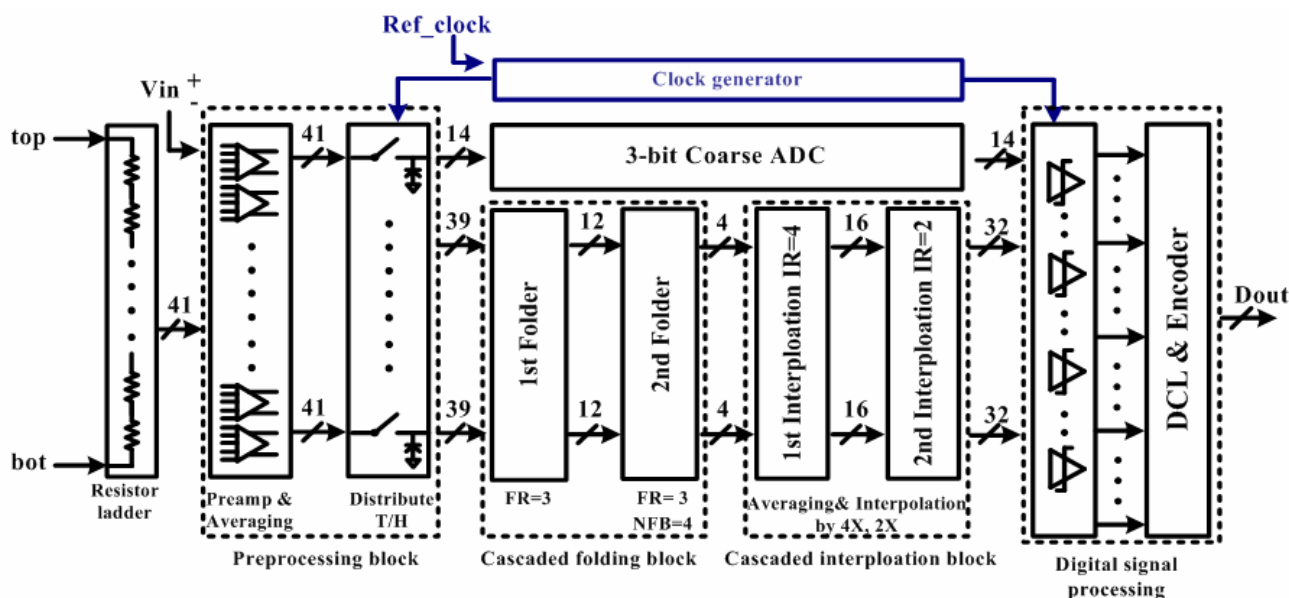


Fig. 1 Block Diagram of the proposed ADC

III. CIRCUIT DESIGN

A. Self-Linearized Pre-Amplifier

The linearity of the pre-amplifier [4] is more important than the voltage gain in the pre-processing block. Therefore, a self-linearized pre-amplifier with the source degeneration technique is proposed for the high-linearity performance. As shown in Fig 2 (a), a degeneration resistor is inserted into the source terminal of input MOSFET. Thus, the linearity of input signal is increased by the degeneration function. Due to the principle of degeneration, the voltage of R_s is drop by I_D , when the V_{in} is increasing. Since the gate-source overdrive input voltage is protected at the degeneration resistor R_s , a smoother variation of I_D appears at the output node. Fig. 2 (b) shows the input range of the proposed pre-amplifier with $R_s=0$ and $R_s \neq 0$.

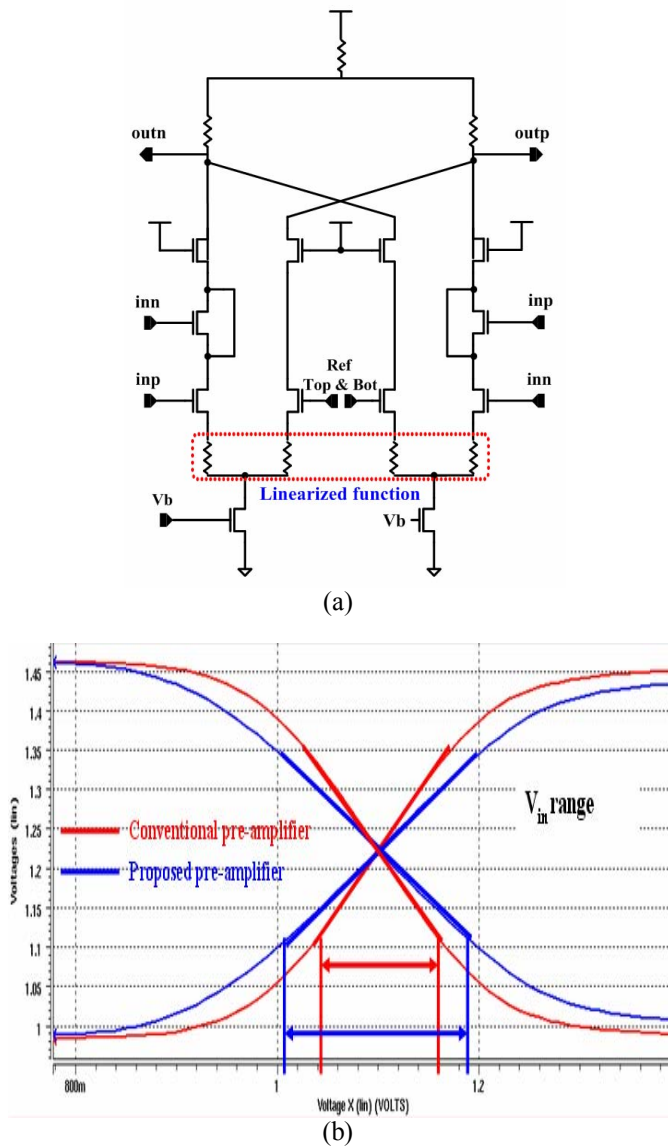


Fig. 2 Self-Linearized Pre-Amplifier
(a) Circuit Diagram (b) Input Range with $R_s=0$ and $R_s \neq 0$

B. Folder Averaging Technique

The distribution of the current at the folding blocks is asymmetrical because of the mismatching problems at the folding input transistors. The asymmetric errors cause the non-linearity errors of the folding signals and decrease the performance of ADC. In conventional ones, a dummy folder is inserted to reduce the mismatching problems for the odd number of the folding amplifiers, as shown in Fig. 3 (a). In this paper, to reduce the non-linearity errors, a folding amplifier with a folder averaging is proposed in Fig. 3 (b). The averaging folder is composed of both the last folder and an inserted folder. Further, two folders are connected by common unit current source. Therefore, the size of the proposed averaging folder is half of the other differential pairs. Since the input of the averaging folder is driven by the over range of the pre-processing block, the current of the folding output is averaged with symmetry. Consequently, the zero-crossing error is reduced and the linearity of the folding signal is improved, compared to the conventional ones. As shown in Fig. 4, the asymmetric errors of the proposed folding signals are significantly decreased by the averaging folders.

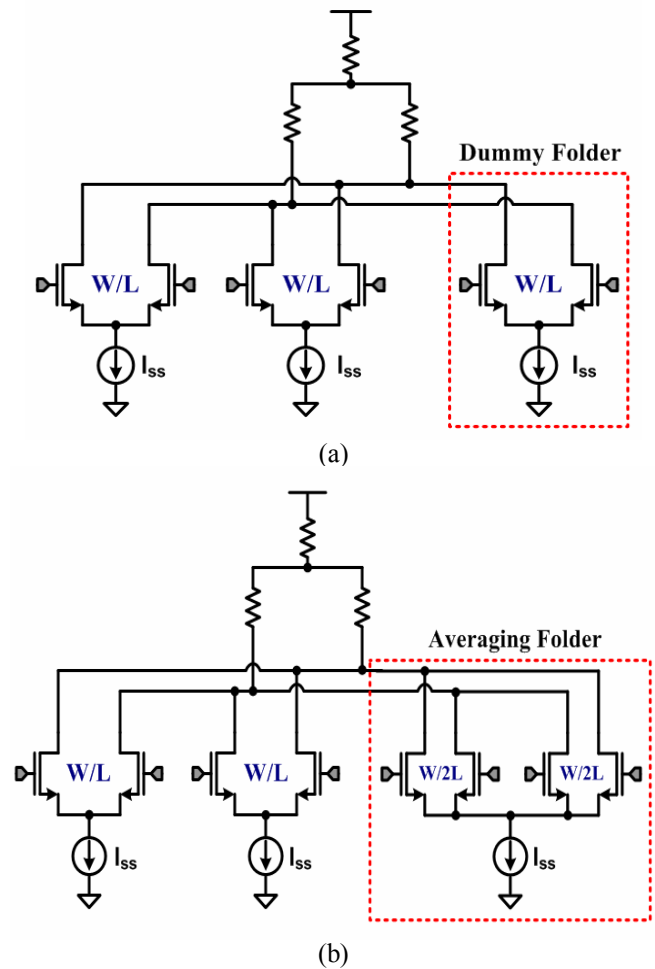


Fig. 3 Folder Averaging Circuit
(a) Conventional Dummy Folder in $FR=2$
(b) Proposed Folder Averaging in $FR=2$

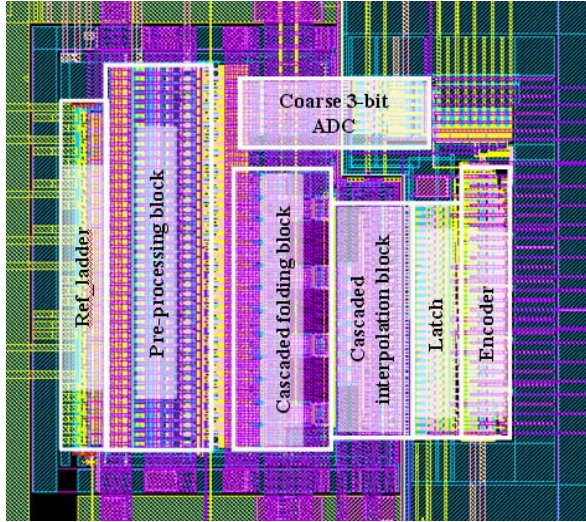
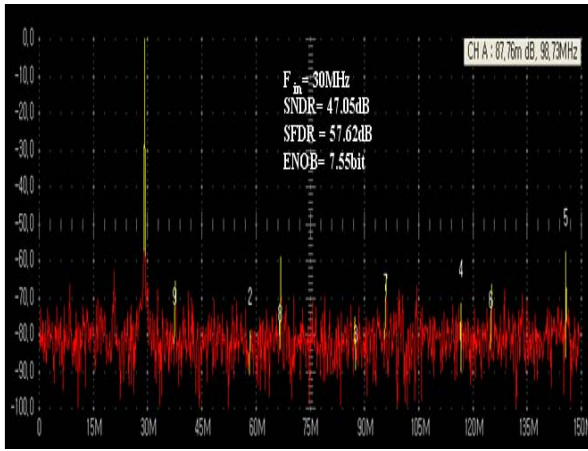
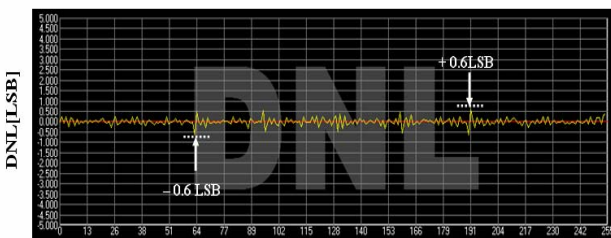
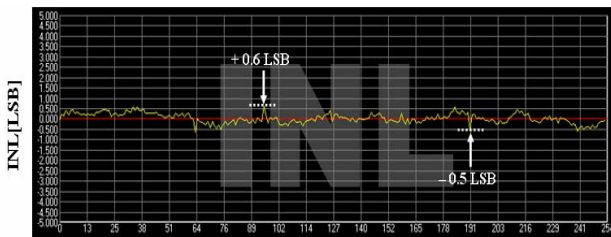


Fig. 7 Chip Layout Drawing of the proposed ADC



(a)



(b)

Fig 8. Measured Results
(a) Measured FFT (b) Measured INL&DNL

V. CONCLUSION

A 1.8V 8-bit 500MSPS CMOS ADC has been described. The architecture of the proposed ADC was based on a folding ADC using a cascaded-folding cascaded-interpolation structure. The self-linearized pre-amplifier with source degeneration technique, the folder averaging technique, and an auto-switching encoder were discussed for the desired performance of the ADC. The effective chip area was 0.79mm^2 , the ADC consumed 200mW at 1.8V supply. The measured ENOB of the proposed ADC was 7.55bits when the input frequency was 30MHz at 500MSPS . The measured results of the ADC are summarized in Table 1.

Table 1. Measured Results of the proposed ADC

Resolution	8-bit
Sampling Freq.	500MSPS
Power Supply	1.8V (Analog + Digital)
Analog Input Range	Diff. 1Vpp
DNL / INL (Measured Data)	$\pm 0.6\text{LSB} / \pm 0.6\text{LSB}$
ENOB (Measured Data)	7.55bits (Fs=300MHz)
Power	200mW
Core Area	$920\mu\text{m} \times 860\mu\text{m}$
Process	Samsung 0.18um CMOS

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