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Nonvolatile memory element based on a ferroelectric polymer Langmuir–Blodgett film

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We report the operation of a potential nonvolatile bistable capacitor memory element consisting of a metal gate, a 170 nm thick ferroelectric Langmuir–Blodgett film of vinylidene fluoride (70%) with trifluoroethylene (30%) copolymer, and a 100 nm thick silicon-oxide insulating layer, all deposited on an *n*-type silicon semiconductor substrate. The device exhibited clear capacitance hysteresis as the gate voltage was cycled between ± 25 V, with a capacitance dynamic range of 8:1 and threshold voltage shift of 2.8 V. The results are in good agreement with the model of Miller and McWhorter [J. Appl. Phys. **72**, 5999 (1992)].
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A ferroelectric crystal can be electrically switched between two stable polarization states, and therefore is particularly attractive for use in nonvolatile random-access memories. Work on ferroelectric memories began in the 1950s[1,2] and has recently blossomed into the commercial development of inexpensive memory cards, integrating perovskite ferroelectric films like lead zirconate titanate into the gate insulator of field-effect transistors (FETs).[3] The current state of the art has overcome considerable engineering obstacles, mostly those related to device cycle lifetime.[4] Even with these achievements, the trend toward thinner and more densely packed devices presents a major challenge for perovskites, which will suffer from increased conductance and electrochemical instability.

Polyvinylidene fluoride (PVDF) and its copolymers with trifluoroethylene (TrFE) are particularly attractive ferroelectrics for nonvolatile memory applications due to their chemical stability, ease of fabrication in thin film form, large polarization, and excellent switching characteristics.[5] In 1986, Yamauchi reported the operation of two promising devices that incorporated 73% VDF copolymer P(VDF-TrFE 73:27) films, which were formed by solvent spinning on a silicon substrate.[6] However, both devices required operating voltages of at least 30 V. In order to reduce the operating voltage below 5 V, similar devices would require polymer films less than 25 nm thick, too thin for reliable fabrication by solvent spinning, so further progress seemed unlikely at the time. A major breakthrough was the fabrication of ferroelectric films of VDF copolymers by Langmuir–Blodgett (LB) deposition,[7] resulting in ferroelectric films as thin as 1 nm that can be switched with as little as 1 V.[8–10] Here we report the fabrication and operation of a metal–ferroelectric–insulator–semiconductor (MFIS) memory element that incorporated a ferroelectric polymer LB film. The small-signal capacitance was measured over a wide range of operating conditions, and it exhibited strong hysteresis due to the bistable polarization state of the ferroelectric film. The results are in good agreement with the predictions of the model of Miller and McWhorter.[11]

For the present study, we prepared a MFIS capacitor like that shown in the inset of Fig. 1. The substrate was a highly polished *n*-type silicon wafer from Polishing Corporation of America and had a 100 nm thick silicon oxide grown on top. Ohmic contact was made to the back side of the silicon with a vacuum-evaporated aluminum film annealed at 450 °C for 10 min. A 100 monolayer (ML) ferroelectric film of the P(VDF-TrFE 70:30) copolymer was fabricated on top of the oxide layer by horizontal LB deposition from a water subphase at a temperature of 25 °C and a surface pressure of 5 mN/m, topped with a 90 nm thick Al gate electrode, and subsequently annealed at 130 °C for 1 h. Further details of the LB film preparation are given elsewhere.[10,12]

The bistable operation of the MFIS device is evident in capacitance–voltage $C(V)$ hysteresis loops like in the example shown in Fig. 1, which was recorded at 30 ± 0.1 °C with a freshly annealed (initially unpolarized) sample. The capacitance was measured with a Hewlett Packard model 4194A capacitance meter operating at 1 kHz and 0.1 V amplitude as the gate voltage V was ramped slowly at a rate of

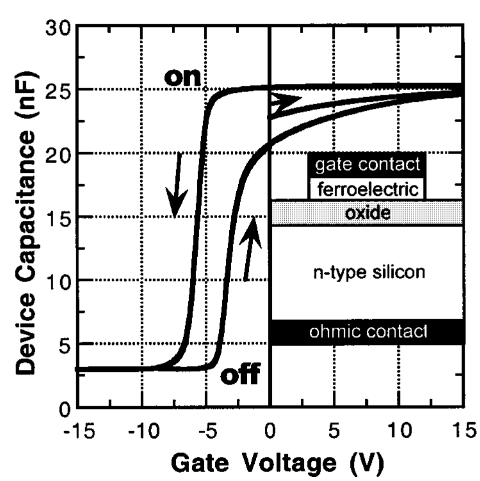

FIG. 1. Capacitance data for the MFIS capacitor measured with 0.1 V excitation amplitude at 1 kHz at 30 °C. Inset: Schematic of the ferroelectric–polymer MFIS capacitor.

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0.05 V/s between ±25 V. After the ferroelectric film polarization was saturated during the first cycle, the loop repeated itself in subsequent cycles without returning to the unpolarized state. The capacitance shows clear hysteresis, due to the bistable polarization states of the ferroelectric film. We designate as "on" the state obtained after saturation with large positive gate voltage, and as "off" the state obtained with large negative voltage. The on/off capacitance ratio was 8:1 at −5 V bias and 1.2:1 at zero bias making it easy to determine the device state without disturbing it. The device capacitance in both the on and off states remained steady for at least 36 h under a holding bias of −5.5 V. At 0 V holding bias, the capacitance in the on state remains stable for at least 36 h, but the off-state capacitance first rises above and then relaxes to the on-state value over several hours. Further study is necessary to determine the cause of this.

The $C(V)$ hysteresis loops of the MFIS device can be qualitatively explained by accounting for the nonlinear characteristics expected of a semiconductor field-effect device, plus the reversible surface charge from the bistable polarization of the ferroelectric film. For large positive gate bias, the semiconductor is in accumulation mode with relatively large capacitance, so the device capacitance of about 25 nF is dominated by the combined ferroelectric and oxide layers. Large positive bias well above the coercive voltage V_C of the ferroelectric film should saturate the polarization state of the ferroelectric film and produce a positive charge density equal to the saturation polarization, $\sigma_F \approx +P_S$, at the ferroelectric–insulator interface. This polarization state is maintained even as the gate bias is decreased (the on–state line in Fig. 1) to zero and slightly negative bias. The sharp decrease in capacitance beginning at approximately −5 V for decreasing bias indicates the growth of a depletion layer as the semiconductor switches from accumulation to inversion. The low capacitance plateau for larger negative gate voltages is dominated by the saturated deep depletion layer and has a value of about 3 nF in this case. The large negative bias well below $-V_C$ saturates the opposite polarization state of the ferroelectric film, producing negative charge density $\sigma_F \approx -P_S$ at the ferroelectric–insulator interface. On increasing the bias, the capacitance rises again as the silicon goes into accumulation mode but at a different bias due to the negative polarization charge. In an equivalent MIS capacitor, the expected threshold gate voltage at 30 °C would be −5.3 V. The reversible polarization of the ferroelectric film shifts the threshold voltage to either side of this value.

A convenient way by which to determine the threshold voltage shift is to use the intersecting points in the slope dC/dV of the $C(V)$ curve shown in Fig. 2. There are two thresholds evident in the hysteresis loop, V_{th1} for the on state and V_{th2} for the off state. The shift $\Delta V_{th} = V_{th2} - V_{th1}$ between the on and off states therefore depends on the saturation polarization and coercive voltage of the ferroelectric film and, the magnitude of the gate voltage sweep. For the data in Fig. 1, the threshold voltage shift ΔV_{th} was saturated at its maximum value of 2.8 V if the voltage sweep was at least ±25 V.

As a further test that the device state is controlled by the bistable ferroelectric polarization and not due to charge injected into the polymer or oxide layers, we recorded the $C(V)$ hysteresis loops as a function of the temperature. As

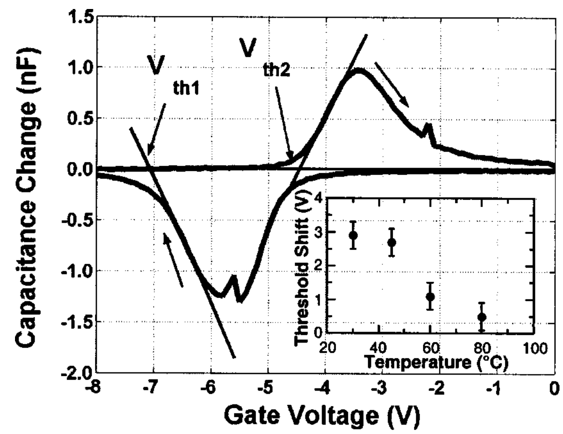

FIG. 2. Derivative of the small-signal capacitance data from Fig. 1 showing the graphical method for determining threshold voltage. Inset: Temperature dependence of threshold voltage shift $\Delta V_{th} = \Delta V_{th2} - \Delta V_{th1}$.

shown in the inset of Fig. 2, the shift in voltage ΔV_{th} decreases to zero as the ferroelectric layer approaches the phase transition temperature of 100 °C, above which there is no spontaneous polarization.[8] Further, no hysteresis was observed with a similarly constructed MIS device.

The MFIS capacitor is accurately described by the model of Miller and McWhorter,[11] which we adapt for comparison with the data. The MFIS capacitor is essentially a MIS capacitor with ferroelectric film on top of the oxide insulating layer. The capacitance C of the MIS device depends strongly on the gate voltage V_G because the surface charge Q at the semiconductor–insulator interface is strongly dependent on the silicon surface potential energy φ_S. The device response is calculated by solving the static Kirkhoff equations for charge and potential.[11,13,14] The gate or device voltage is then

$$V_G = \frac{\varphi_S}{q} - \frac{Q(\varphi_S)}{C_{ox}} + E_f d_f + \frac{\varphi_{MS}}{q}, \tag{1}$$

where q is the elementary charge, C_{ox} is the capacitance of the oxide film, E_f and d_f are the electric field and thickness of the ferroelectric film, and φ_{MS} is the difference in the metal–semiconductor work function. The surface charge on the silicon is opposite that on the bottom surface of the ferroelectric film,

$$Q/A = -\varepsilon_f \varepsilon_0 E_f - P^{\pm}(E_f), \tag{2}$$

where ε_0 is the permittivity of free space, A is the device area, and ε_f is the low-field dielectric constant of the ferroelectric film. We assume here that there is no space charge in the insulating layers, and that the capacitance of the oxide and ferroelectric layers is independent of field, although in practice the dielectric constant of the ferroelectric increases by about 10% at E_C due to the nonlinear contribution from the polarization.[15] The polarization P_f of the ferroelectric film is well approximated by the form[11]

$$P_f^{\pm}(E_f) = P_s \tanh\left(\frac{E_f \mp E_C}{\Delta E_C}\right), \tag{3}$$

where P_S is the saturation polarization, E_C is the coercive field, and ΔE_C is a hysteresis loop shape parameter. The small-signal capacitance C_{ss} of the MFIS device depends on

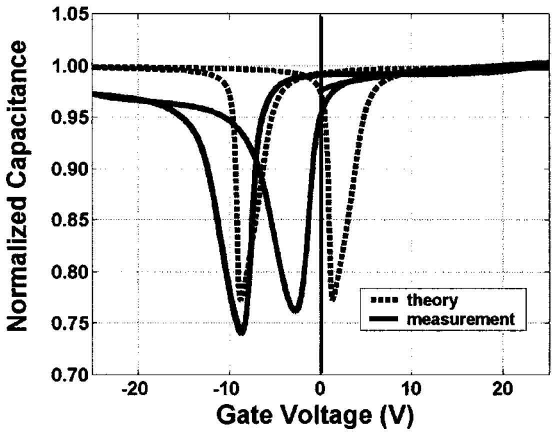

FIG. 3. Small-signal capacitance calculated from the model (dotted lines) and the capacitance measured with 0.1 V excitation amplitude at 250 Hz while the sample was illuminated at 30 °C (solid lines).

the differential capacitance $dQ/d\varphi_S$ of the depletion/accumulation layer, which in turn depends on the surface potential energy $\varphi_S(V)$ as follows:[11,13,14]

$$\frac{1}{C_{ss}}=\frac{1}{C_f}+\frac{1}{C_{ox}}+\frac{1}{dQ/d\varphi_S}. \tag{4}$$

The $C(V)$ curves for the MFIS device were calculated with the iterative procedure of Miller and McWhorter[11] to obtain the relation $\varphi_S(V)$ for a voltage sweep of ± 35 V and then applying Eq. (4) to obtain the small-signal capacitance. The input parameters were obtained as follows. Independent measurements of the hysteresis loop of a similar 100 ML LB copolymer film deposited on glass, with Al electrodes, yielded a coercive field $E_C=82\pm 4$ MV/m and shape parameter $\Delta E_C=28\pm 4$ MV/m. The film thickness $d_f=170\pm 20$ nm was determined from independent ellipsometric measurements of identically prepared LB films over a wide range of thickness,[16] and the saturation polarization $P_S\approx 0.10$ C/m^2 was estimated from values in the literature.[5] The properties of the *n*-doped silicon and oxide obtained from the literature were $\varepsilon_{ox}=3.9$, $\varepsilon_S=11.8$, and $\phi_{MS}=-0.3$ V, while the effective doping level $N_D\approx 3\times 10^{16}$ cm^{-3} was estimated from the MIS device measurements; the oxide thickness $d_{ox}=100$ nm was provided by the manufacturer, and the device area $A=1.7\pm 0.02$ cm^2 was equal to that of the Al gate electrode.

In order to obtain experimental $C(V)$ curves corresponding to the model, we illuminated the sample with fluorescent lighting (intensity 100 μW/cm^2) and measured the capacitance at 250 Hz. Illumination increases the number of free carriers at the silicon surface, thereby increasing the semiconductor capacitance in inversion mode so that the device capacitance returns to the ~25 nF value from the oxide and ferroelectric layers only. If the sample is not illuminated, as was the case for the data shown in Fig. 1, the device capacitance at negative bias stays low, approximately equal to the limiting silicon capacitance, except at frequencies well below the inverse minority carrier response time,[13] which was well below the 5 Hz limit of the capacitance meter. The agreement between the measured and calculated $C(V)$ curves shown in Fig. 3 is very good, considering that none of the parameters were adjusted. The shift in voltage ΔV_{th}, in this case the shift in the position of the capacitance minimum, was 10.0 V from the calculations and 5.9 V from the data. But the calculations revealed that even for a ± 35 V sweep, a 100 ML ferroelectric film with $E_C=82$ MV/m would not be fully switched, implying that the true film coercive field was much smaller.

Detailed characterization of the LB polymer MFIS device demonstrated hysteresis with a threshold shift of 2.8 V and bistable operation with an 8:1 ratio between the on and off states. The Miller–McWhorter model reproduced the data well, but indicated that the coercive field and/or the switchable polarization of the ferroelectric film incorporated into the device were smaller than expected. Although the 100 ML device is an excellent learning tool, and demonstrated some of the capabilities of ferroelectric copolymer Langmuir–Blodgett films, with an operating voltage of ± 25 V it is not likely to be a commercially viable device. Since the ferroelectric LB films show excellent switching characteristics down to 1 nm thickness, we anticipate no fundamental impediments to making devices that operate at 1 V or less. While perovskites require processing temperatures as high as 800 °C, the polymers require annealing at about 130 °C for 1 h, which should have no significant effect on other device components. Since the copolymer melts irreversibly at temperature of about 150 °C, it will probably be necessary to apply this layer after the high-temperature hydrogen annealing. This is feasible with both the MFIS and field-effect device structures. Future studies will probe data retention, switching speed, fatigue, and other lifetime-limiting effects, all crucial to the development of a competitive ferroelectric memory. Other potential uses of the switchable polarization include inducing and controlling carrier densities in ferroelectric and ferromagnetic films, two-dimensional electron gases, and quantum wells.

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