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H.Q. Li
National Institute of Standards and Technology, Boulder, Colorado

R.H. Ono
National Institute of Standards and Technology, Boulder, Colorado

L.R. Vale
National Institute of Standards and Technology, Boulder, Colorado

D.A. Rudman
National Institute of Standards and Technology, Boulder, Colorado

Sy_Hwang Liou
University of Nebraska-Lincoln, sliou@unl.edu

A novel multilayer circuit process using $YBa_2Cu_3O_x/SrTiO_3$ thin films patterned by wet etching and ion milling

H. Q. Li,[a),b)] R. H. Ono,[c)] L. R. Vale, D. A. Rudman, and S. H. Liou[a)]
National Institute of Standards and Technology, Boulder, Colorado 80303

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A process combining hydrofluoric acid (HF) and Ar^+ ion milling has been used to make $YBa_2Cu_3O_x/SrTiO_3/YBa_2Cu_3O_x$(YBCO/STO/YBCO) multilayer test circuits. Low-angle steps can be readily etched in STO and YBCO films with this process. YBCO lines crossing 5° steps have about the same critical temperature T_c (89–90 K) and critical current density J_c ($>1\times10^6$ A/cm^2 at 86 K) as lines on planar surfaces. Via connections have the same T_c as other circuit components and adequate critical currents for most circuit designs. © *1996 American Institute of Physics.* [S0003-6951(96)04744-4]

We have developed a reproducible fabrication process which allows us to pattern multilevel high-temperature superconducting (HTS) structures with the best critical current densities (J_c) and transition temperatures (T_c) of the fabrication processes reported to date.[1–10] In conjunction with HTS Josephson junctions, structures of this type are used in many superconducting applications such as dc SQUID flux transformers and Josephson digital circuits. Our process is suitable for these HTS multilayers circuits, since both upper and lower HTS layers have high crystalline quality even at crossovers and via connections and are well isolated by the intermediate epitaxial insulator. We have fabricated our test samples using $YBa_2Cu_3O_x$ (YBCO) on $SrTiO_3$ (STO) on YBCO, a material system which has been used by several groups. In addition, the process appears to be compatible with other, low dielectric constant, epitaxial insulators.

A great challenge for multilayer circuits made from HTS films is the requirement that all of the layers maintain epitaxy when grown over the topology of patterned underlying layers. The fabrication process must include careful cleaning and surface preparation after each layer is patterned; the cleaning is often made problematic by the presence of photoresist residues. The epitaxial quality of crossovers and interconnects could be maintained either by planarization (a technique not yet perfected in HTS processing), or by forming shallow slopes. There are two motivations for forming shallow slopes in the edges of the patterned bottom YBCO layer and the insulating STO layer. First, the desired *c*-axis orientation of upper YBCO thin films is changed when crossing a high-angle step, forming grain boundaries[1] which reduce J_c and introduce unwanted Josephson junctions at the crossing. Second, the flux noise in the YBCO increases rapidly as the film crystalline quality degrades.[2] This letter will focus on transport J_c as the figure of merit in evaluating our process. Ion milling at an inclined incident angle combined with photoresist overbaking was used by several groups[3–5] to etch the bottom YBCO and the insulating STO layer for beveled steps. Another way to form low-angle crossovers is the use of shadow masks[6–8]; however, this technique is not applicable for making via connections. Hydrofluoric acid (HF) solutions are highly selective for etching STO films over YBCO, and have been used in fabricating high T_c superconducting multilayer circuits.[9] Our process combines HF wet etching and ion milling in making YBCO/STO/YBCO multilayer circuits with slope angles as low as 5°.

All YBCO and STO layers used in this study were grown *in situ* on (100) $LaAlO_3$ substrates by KrF laser ablation. The YBCO was grown in 106 Pa (800 mTorr) of O_2 at 775 °C and the STO in 53 Pa (400 mTorr) of O_2 at 745 °C. The bottom YBCO layer, 100–200 nm thick, and a STO layer, 150–250 nm, were grown in one deposition step, ensuring a clean and high quality interface. We will call this level ''Y1.'' Using a conventional positive photoresist mask, the bilayer was patterned and isotropically wet etched with 3% (wt) HF in H_2O at 25 °C to etch the STO layer. The etch rate of STO is 100 nm/min under these conditions while the rate for etching YBCO is only 4.5 nm/min. The photoresist was removed after the HF and the pattern profiles were examined by atomic force microscopy (AFM). We can reproducibly make 3–30° steps in the STO layer depending on the baking cycles (soft, post-exposure, and hard) and the HF concentration. In general, angles are steeper for higher bake temperatures because the step angle depends critically on the adhesion of the photoresist to the STO.

The wet-etched STO was then used as a conformal ion-milling mask for etching the bottom YBCO layer at 0° incident angle by 300 eV Ar with a 0.5 mA/cm^2 beam current density. In our ion-mill system YBCO and STO etch rates are similar (10 nm/min for STO and 12 nm/min for YBCO) so the shallow angle step in the STO layer was copied into the bottom YBCO layer. After ion milling, the film is ready for the next deposition without the need for further cleaning, since no photoresist was present during the ion milling. The thicknesses of the YBCO and STO were selected in such a way that a thin layer of STO remained after milling, leaving a seed layer for the subsequent STO isolation layer.[3,10] A drawing of the vertical structure is shown in the inset to Fig. 1. An insulating STO layer of 150–200 nm was then deposited on the etched film. The film was heated up in 800 Pa (6 Torr) of O_2 before the deposition of the insulating STO layer to prevent oxygen loss from the bottom YBCO layer. Figure 1 shows the profiles of a step in a test chip measured by AFM after [1(a)] the HF etching of the protective STO, [1(b)] ion milling of the bottom YBCO, and [1(c)] the depo-

[a)]Permanent address: Department of Physics, University of Nebraska, Lincoln, NE 68588-0111.
[b)]Electronic mail: hli@unlinfo.unl.edu
[c)]Electronic mail: ono@boulder.nist.gov

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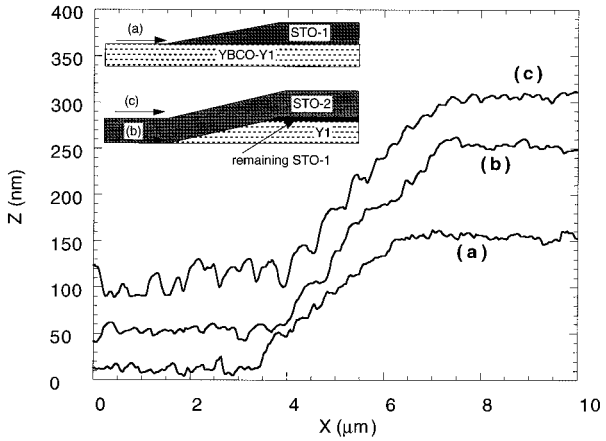

FIG. 1. Three AFM scans: (a) after the HF etching of the protective STO, (b) after ion milling of the bottom YBCO, and (c) after the deposition of the insulating STO. The slope angles are approximately 5° and the curves have been offset for clarity. The inset shows the vertical structure that is probed: STO-1 is the milling mask (note that a thin layer remains after ion milling), STO-2 is the insulating layer, and the arrows indicate the surfaces that are scanned in (a), (b), and (c).

sition of the insulating STO. The slope angles are approximately 5°. This shows that the profile formed by first HF wet etching in the protective STO layer was maintained throughout the processing, with small variations due to slight differences in milling rates.

Via connections were opened in the STO layer using the shallow-angle HF wet-etching process. The film was then ion milled for 1 min to clean the bottom YBCO in the windows which had been exposed to HF solution. Again since no photoresist was present in this ion-mill process problems with photoresist residue were avoided. AFM scans were taken after each process step. The wet etch provided via holes with low-angle edges. Finally, the sample was heated up to 775 °C, again in 800 Pa of (6 Torr) O_2, and the top YBCO layer of 200 nm was deposited after the O_2 pressure was lowered to 106 Pa (800 mTorr). After cooling, approximately 50 nm of Au was sputtered on the YBCO for low contact resistance pads. Then the film was patterned and ion milled to form the desired pattern in the top Au/YBCO bilayer; this layer will be called ''Y2.''

For electrical characterization, we used a multilayer test circuit which included: (1) a 10-μm-wide, 220-μm-long line in Y2 with 1 crossover; (2) a zigzag path in Y2 with 80 crossovers; (3) a 10 turn coil in Y2 with 31 crossovers and an 8×16 μm^2 via connection to Y1; (4) two via connections between Y2 and Y1 of 10×10 μm^2 and 10×20 μm^2 in area, respectively; (5) a 6-μm-wide line in Y1; (6) a 10-μm-wide line in the Y2; and (7) a 100×200 μm^2 trilayer pad to test the STO isolation. A micrograph of the center region of a finished sample is shown in Fig. 2.

We investigated the influence of step angle on the superconducting properties of crossovers for different samples etched to give different step angles. We measured the 10-μm-wide Y2 lines with a single crossover on several different samples. Figure 3 shows $J_c(T)$ of 5°, 15°, and 25° crossovers with T_c values of 89.8, 89.1, and 90.6 K. The transition temperatures show no consistent variation with the step angle; however, only the 5° crossover has the same J_c as that

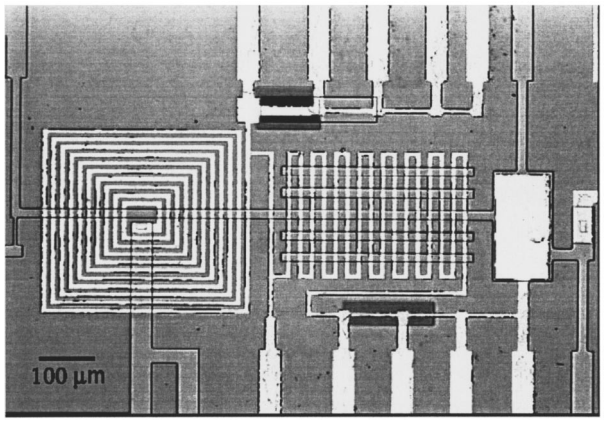

FIG. 2. A micrograph of the multilayer process test structure.

of a planar film. The following results on crossovers and interconnects were obtained from a sample with 5° slopes. The test chip had a 100 nm Y1 layer, a 200 nm STO layer, and a 200 nm Y2 layer. The top and bottom YBCO test strips had T_c values of 90 and 89.3 K, respectively. The resistivity of the insulating STO layer is typically 8×10^7 Ω cm or higher with a breakdown field of 10^4 V/cm. We measured the J_c vs temperature of various test structures. These data are shown in Fig. 4. The $J_c(T)$ curve of the crossover line is close to those of the top and bottom YBCO films, indicating that there are no weak links at the 5° STO steps. The lower $J_c(T)$ of the zigzag path arises primarily from a slightly lower T_c somewhere in the 3-mm-long line. Normalizing the $J_c(T)$ to a slightly lower T_c moves the curve directly onto the other three curves in Fig. 4(a); it is therefore likely that there are no weak links at the crossovers.

The two vias from Y2 to Y1 are 10×10 μm^2 and 10×20 μm^2. Their critical currents at 80 K are 16.5 and 26 mA, respectively, high enough for most practical circuits. It is not clear where the limiting current is first reached: in the crossing down to the Y2 surface, the Y1 to Y2 c-axis contact, or the perimeter of the Y1 film. The current densities shown in Fig. 4(c) were calculated by dividing the critical current by area of the contact. The J_c of the coil, in Fig. 4(b), was calculated using the cross-sectional area of the 10-μm-wide

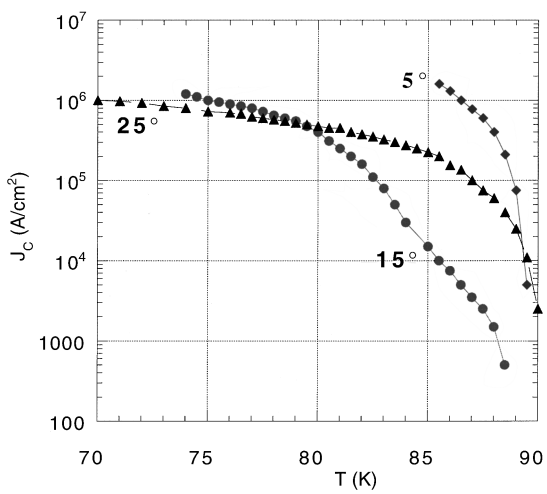

FIG. 3. J_c vs T of crossings over three different step angles, 5° (diamonds), 15° (circles), and 25° (triangles).

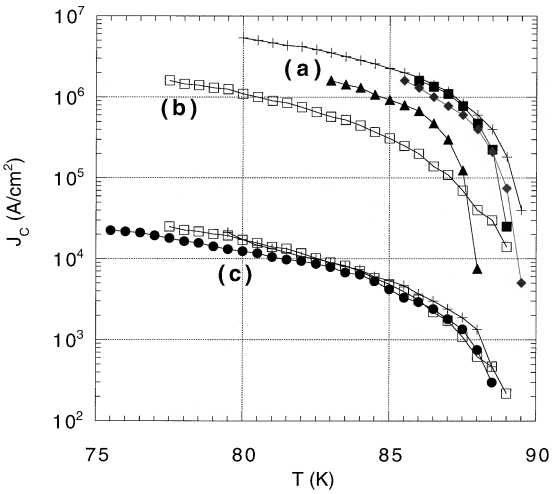

FIG. 4. (a) The J_c vs T of various test strips: bottom YBCO (+), top YBCO (■), single crossover (♦), 80 crossings (▲). (b) $J_c(T)$ for the coil calculated from the wire cross section (□). (c) The $J_c(T)$ of the large via (●), small via (+) and coil (□) using the via areas.

line. The curve shown reaches 1.1×10^6 A/cm^2 at 80 K, but is much lower than that of the zigzag path even though it has fewer crossovers. The J_c of the coil is probably limited by its via connection, 8×16 μm^2 in area. We converted the $J_c(T)$ curve according to the contact area as shown in Fig. 4(c). This is very close to the $J_c(T)$ curves of the two vias calculated in the same way. The values of J_c are consistent with the current densities reported for transport in the c-axis direction.[12]

In conclusion, we have described a new process for making YBCO/STO/YBCO multilayer circuits by combining HF wet etching and ion milling; this process does not expose photoresist to the ion milling, simplifying cleaning before subsequent STO and YBCO depositions. We have made very high quality bottom and top YBCO films, and low-angle crossovers which have the same J_c as the planar film. Via connections with adequate critical current were also obtained in this way. The limiting J_c of this type of multilayer circuit appears to be the via connection, suggesting the need for more complex via structures, perhaps with increased a-b plane interfacial areas. We are extending this work to investigate the patterning of other epitaxial insulators such as Sr_2AlTaO_6 and Sr_2AlNbO_6 in collaboration with other groups and we are investigating this technique for forming the base electrode layers for edge geometry Josephson junctions.

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