2006

Self-Oscillating CMOS Class D Amplifier Optimized for Low Output Power

Daniel J. White
University of Nebraska-Lincoln

SELF-OSCILLATING CMOS CLASS D AMPLIFIER OPTIMIZED FOR LOW OUTPUT POWER

by

Daniel J. White

A THESIS

Presented to the Faculty of
The Graduate College at the University of Nebraska
In Partial Fulfillment of Requirements
For the Degree of Master of Science

Major: Electrical Engineering

Under the Supervision of Professor Michael Hoffman

Lincoln, Nebraska

December, 2006

SELF-OSCILLATING CMOS CLASS D AMPLIFIER OPTIMIZED FOR LOW OUTPUT POWER

Daniel J. White, M.S.

University of Nebraska, 2006

Advisor: Michael Hoffman

The continual push for smaller size and decreased power consumption has prompted the adoption of class D amplification for speaker and headphone drivers in portable media devices. With proper design, the power efficiency of this amplifier type can exceed any other topology over the whole output range, even at low output levels.

Simple amplifier topologies are not the norm for these integrated circuit (IC) class D amplifiers. This thesis shows that such complexity is not necessary for good performance. A recently presented simple self-oscillating topology is mapped into a standard CMOS technology and fabricated in a 0.5 micron process. The output stage is optimized for a range of modulation indices, simultaneously increasing average efficiency and reducing chip area.

Modifications are presented that reduce the large transient currents inherent in CMOS inverter chains without increasing implementation complexity. Also, changes to the optimization procedure are presented that make the results more relevant to low-power, self-oscillating topologies. Test results are compared to predicted and simulated values. This thesis shows that design complexity is not requisite for good performance and high efficiency.

Contents

List of Figures

List of Tables

Acknowledgments

I would like to acknowledge the following people for their contribution to this thesis work:

- Dr. Hoffman for providing a perspective on the project that wasn't buried in implementation details. The questions he asked required me to justify project aspects in terms of real improvements and relevance. His flexibility in advising a thesis on amplifier design allowed his different set of expertise to make this a more rounded project.

- Dr. Balkır for providing a path to chip fabrication. It was the prospect of available die area that kickstarted this design, allowing for a full proof-of-concept design chain. His trust allowed me to take an unconstrained design approach without requiring a justification of every non-standard feature.

- My wife Kathryn for the support and encouragement she gave me during the whole process. Looking back, I can now empathize with her thesis process and can see the multitude of ways her help allowed me to do my best. I am indebted to her and am constantly amazed with this wife I don't deserve.

Chapter 1

Introduction

The adoption of class D topologies for low power (< 1W) amplifiers is due to their superior efficiency over the whole modulation range. Even though the class D operating principle is relatively straight forward, implementations typically have layers of control loops and complexity to reduce nonlinearities due to imperfect devices. Such complexity comes at the expense of increased power consumption and implementation size, both claimed advantages of the class.

1.1 Background

The canonical implementation of an analog input class D amplifier utilizes what's called Natural Pulse-Width Modulation (NPWM) where the input signal is compared with a triangular carrier to generate a 2-level signal. Figure 1.1 shows the relevant signals within such an amplifier. Varying both the leading and trailing pulse edge positions yields a baseband output spectrum that is free of switching components. This pulse-train is then typically demodulated with a second-order LC filter to recover the baseband signal. Problems with the NPWM approach include the generation of very high quality triangular carrier reference and a power supply rejection

ratio (PSRR) of 0dB. Nonideal switches and comparators both reduce efficiency and increase distortion.

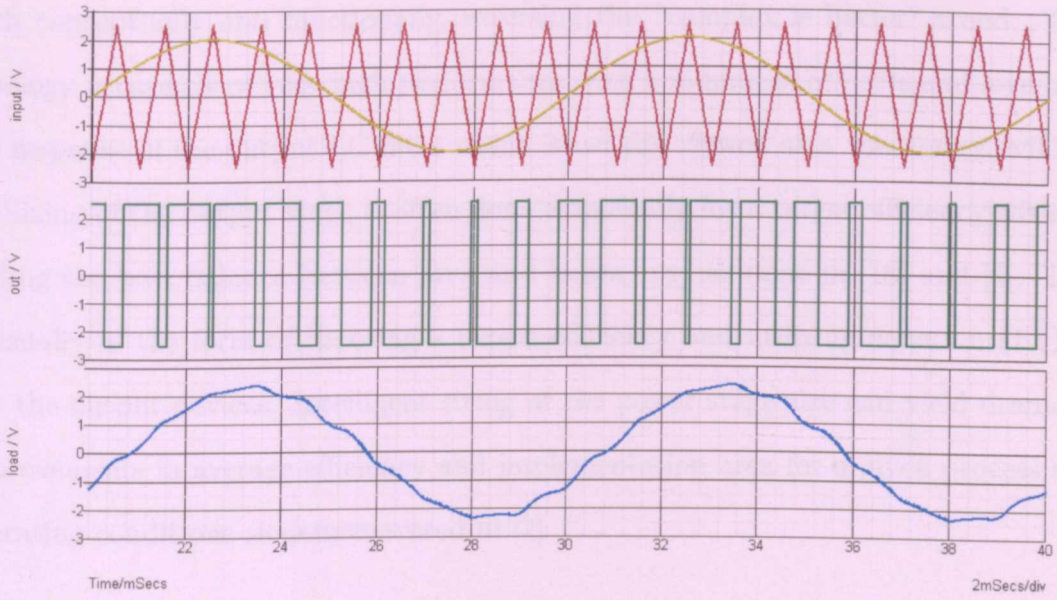

Figure 1.1: NPWM amplifier signals from the top: Input and triangular reference, comparator output, demodulation filter output.

Within a digital system, it would be desirable to directly generate NPWM from digital signals. Directly implementing NPWM with digital signals requires a counter running at $2^N \times f_s$ to generate the triangular carrier signal to provide the same pulse-width resolution as the input signal. Such a directly implemented system is only practical for very low bit depth signals. For example, a 16-bit 44.1kHz signal for CD would require a counter running at $2^{16} \times 44,100 = 2.89$GHz while an 8-bit 8kHz signal for telephone only requires 2.05MHz. Noise-shaping modulators reduce the bit depth and clock frequencies at the expense of greater out of band noise. This modulator also has a PSRR of 0dB.

Many feedback techniques have been used for both the analog and digital input modulators which compensate for nonideal behavior by increasing the effective loop gain or pre-distorting the PWM signal. Though many of these topologies are capable

of very low distortion performance and flat frequency response, they exhibit complexity in both analysis and implementation. A recently introduced topology [1] is simple both conceptually and functionally, reversing the "complex is better" trend. This topology is capable of very high performance with a minimum of parts and leverages the response of the output LC filter which is usually viewed as a "necessary evil."

Sizing of the output stage is often done empirically for a target efficiency without finding the best balance between area and losses, e.g. as done in [18] and [4]. This is usually in the form of choosing a target efficiency and utilizing equation (1.1) to size the output devices. Intelligent sizing of the power stage size can yield dramatic improvements in average efficiency and implementation area for a given process and operating conditions as demonstrated in [2].

$$\eta_{max} = \frac{R_{load}}{R_{load} + R_{on}} \tag{1.1}$$

1.2 Motivation

My personal interest in class D amplification started with learning about the A and B amplifier classes and some of their design issues. It was set aflame during the senior year capstone design project for my B.S.E.E. which was a $100W$ class D amplifier using NPWM and output stage feedback. By this time I was involved in audio mixing ("sound guy"), vintage audio gear repair, and recording console upgrades and maintenance and jumped at the chance to apply coursework to an audio design problem. Interest and coursework in CMOS VLSI and a general passion for analog electronics made for a natural extension of class D design into this M.S. thesis topic.

Class D amplification is fast becoming the choice for high-power audio amplification because of its efficiency. Portable low power devices also benefit from this

increased efficiency, resulting in smaller batteries and longer run times. Consequently, it seems that every IC company is introducing commercial class D-on-a-chip solutions

Integrated circuit class D solutions pave the way for including an audio amplifier on the same die as a processor, memory, and signal processing, reducing cost and size at the same time. A one-chip cell phone and the next iPod "pico" are example applications. Just as switch-mode power supplies have pushed out traditional regulators, signal (power) amplification is being taken over by switching designs.

Chapter 2

Self-Oscillating Topologies

There are several techniques for creating a self-oscillating condition in a switching amplifier. Many variations on these base techniques have been presented (e.g. [12], [13], [9], [10], [11], [7]) while retaining the core operating principle. These categories include: hysteresis, phase-shift, and LC phase-shift.

One advantage of self-oscillation is the elimination of the need for a low jitter clock source, required for both high performance analog and digital input fixed-frequency amplifiers. Switching frequency is then set by an oscillation condition and varies nonlinearly as a function of the input signal. A notable exception to large switching frequency variation is the one-cycle control topology in [7].

Disadvantages of the self-oscillating feature include intermodulation products generated when using multiple amplifiers in a system; analysis and testing of class D oscillator coupling and synchronization is given in [6]. Also, large-signal analysis becomes feasible only with simulation, as the small-signal approximations typically given only hold for modulation indices of $D \ll 1$.

2.1 Hysteresis

The hysteresis oscillator, shown conceptually in Figure 2.1, is both simple to implement and capable of good performance. The switching frequency of this amplifier is dependent on power supply voltage, input level, and hysteresis range. Also, the minimum pulse width is also only one half of the idle pulse width [1]. These factors combine to make its overload characteristics particularly poor. When approaching clipping, a "tizz" can be heard as the switching rate descends into the audio range while still retaining considerable energy at f_{sw} [1].

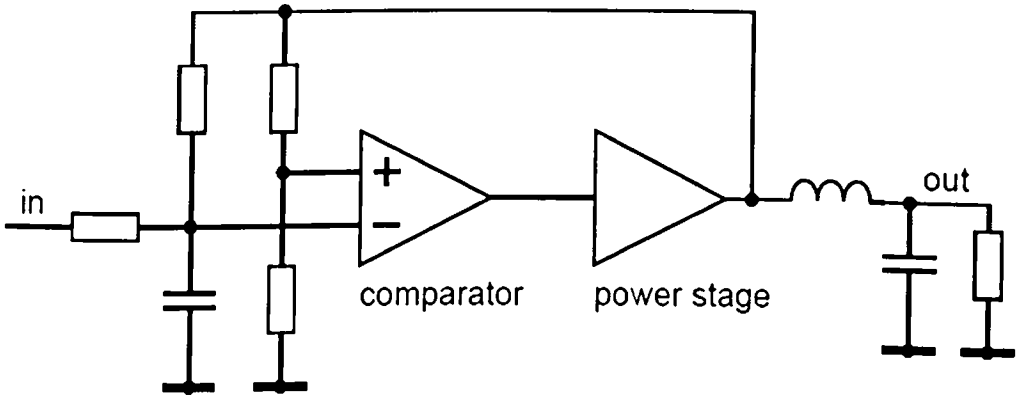

Figure 2.1: Conceptual diagram of a hysteresis-based class D amplifier, from [1]

This amplifier frequency response is sensitive to load variations, given the damped resonant RLC output network. Non-linearities introduced in the output filter are not corrected at all. Typical modifications move the feedback to the filter output ([14], [13], [9]). Specifically, dropping the input capacitor in [9] and using the inductor to provide the integral of the output allows some control over load variations. Unfortunately, the amplifier still suffers from poor near-overload behavior, made evident from the oscilloscope plots shown in the reference.

2.2 Phase-Shift

This amplifier type, shown in Figure 2.2, uses a general phase-shift network at the input to generate 180° of phase shift. Inversion in the comparator generates the remaining 180°, creating the 360° phase shift necessary for sustained oscillation.

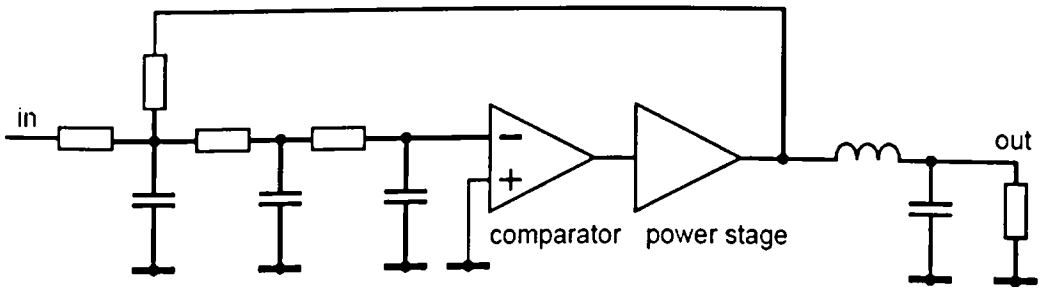

Figure 2.2: Conceptual diagram of a phase-shift-based class D amplifier, from [1]

The overload behavior of this amplifier is better behaved since the pulse width can go to zero. Energy in the switching harmonics also decreases, serving to eliminate the "tizz" heard in the hysteresis amplifier. Informal listening tests confirm this in [1].

As in the hysteresis amplifier, there is no output filter control, leaving high frequency response a sole function of filter loading. Proposed modifications add extra feedback loops to reduce the effects of loading and non-linear behavior [12] at the expense of increased f_{sw} dependence on the input. Overload behavior then tends to behave like the hysteresis amplifier.

2.3 LC Phase-Shift

Introduced by [1] and shown in Figure 2.3, this amplifier type also uses phase shift to generate an oscillation condition. However, it leverages the phase response of the external L-C filter and the inherent delay through the amplifier to generate the

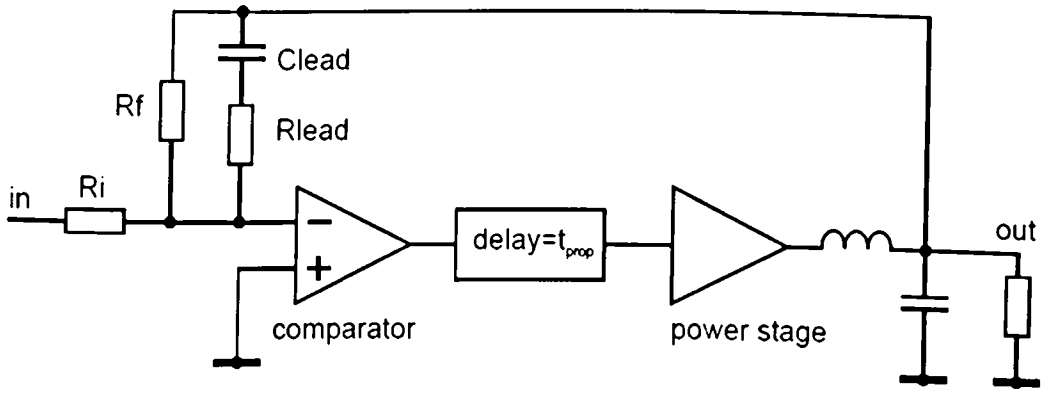

Figure 2.3: Conceptual diagram of a L-C phase-shift-based class D amplifier, from [1]

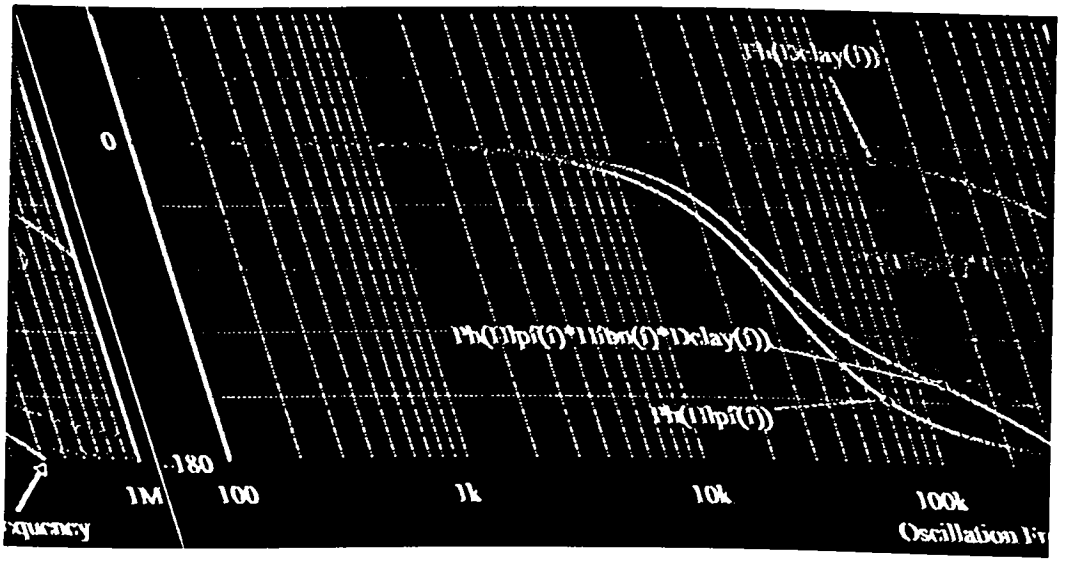

Figure 2.4: Phase response of feedback network including the output filter, from [1]

necessary 180° phase shift. The comparator provides the inversion as before.

The $R_{lead} - C_{lead}$ network provides a phase lead to cause the composite phase response to cross 360° at a greater slope. Figure 2.4 shows the phase response of the output filter alone, time delay, composite lead network and output filter, and the total response (in green). It shows that the addition of the lead network both increases the phase slope at oscillation and increases the switching frequency.

Additional passive or active poles at the input considerably increase the loop gain of this amplifier. Per the analysis in [1], loop gain generated in this amplifier is

approximately 6 dB less than the inverse of the feedback network attenuation (which is mainly the output filter) at the switching frequency, see equation (2.1). Loop gain therefore tracks the response of the output filter; consequently, the frequency response of the unloaded amplifier is almost indistinguishable from when a load is attached. This is in stark contrast to the unloaded responses obtained in both the (open loop) hysteresis and phase-shift topologies.

$$A_{DC} = \frac{1/2}{H_{LPF}(f_{sw})} \tag{2.1}$$

2.4 Mapping LC Phase-Shift Amplifier into CMOS

Originally presented as a discrete component $100W$ amplifier, this topology can be readily mapped into a standard CMOS technology. Its simple loop gain enhancement technique and relaxed active control requirements allow an IC implementation to be barely larger than the power stage itself.

Besides the power stage, the LC phase-shift amplifier needs a comparator, a small lead network, closed-loop gain-setting resistors, and an output LC filter. Except for the filter, all other elements can easily be included on-chip for better integration. Requirements placed on the comparator are relatively weak as described in section 4.1.1 and mostly affect the maximum switching frequency and system DC offset.

Chapter 3

Power Stage

A pulse-width modulated (PWM) signal, or some variation two-level modulation such as $\Sigma\Delta$ or pulse-density modulation, is sent to the power stage which switches supply voltage to the output filter in the same manner as a buck converter. Three-level modulation is not considered here because of its reliance on a full-bridge output stage which is incompatible with standard three-wire headphone connections.

The power stage analyzed and implemented in this thesis is not specific to any particular amplifier topology. Therefore, discussion of power dissipation, gate drivers, and optimization is independent of the choice of class D topology. However, the focus here is on low output power amplifiers, e.g. portable battery-powered applications, and self-oscillating topologies.

3.1 Power Dissipation Mechanisms

Within a switching amplifier, there are three power dissipation mechanisms usually considered: resistive, capacitive or switching, and short-circuit. Simplistic reductions only use the resistive mechanism to find maximum efficiency at full modulation and ignore the effect of device size at low modulation levels.

In [2], Chang, et al. use these three mechanisms for finding an optimum power stage size, accounting for all three mechanisms. Their procedure will be discussed in section 3.3. The formulas presented below for these three mechanisms are from [2], modified for the half-bridge output stage and new gate drivers. Symbols used in the following discussion are described in Appendix A.

In addition to the three "main" mechanisms, there are a few other areas where dissipation occurs which are magnified by characteristics of a self-oscillating topology, typical input signals, and the relatively low total power output found in portable applications. It has been shown that these extra mechanisms have a significant impact on practically obtained efficiency levels [4].

Calculation of efficiency is done through equation (3.1):

$$\eta = \frac{P_{load}}{P_{load} + P_{res} + P_{cap} + P_{sc} + P_{react}} \tag{3.1}$$

3.1.1 Resistive

Resistive dissipation is a function of load current and "on" resistance of the output transistors. Load current varies linearly with modulation depth, assuming both a purely resistive load and neglecting load current reduction due to non-zero R_{on}. Note that both R_{on} and I_o given here are halved from [2] due to the change to half-bridge output. Also note that the PMOS/NMOS ratio α is chosen to yield approximately equal on resistances.

$$P_{res} = \frac{1}{2}\left(D \times I_o\right)^2 R_{on} \tag{3.2a}$$

$$I_o = \frac{V_{dd}/2}{R_{load}} \tag{3.2b}$$

$$R_{on} = \frac{L/(\mu_p C_{ox})}{(V_{dd} - V_{th})W_p} + \frac{k_{1p} + \alpha k_{1n}}{2W_p} + R_L \tag{3.2c}$$

$$k_{1p,n} = (l_1 + 2l_3)R_{p,n} + 2(l_1 + l_2)R_{ctp,n} \tag{3.2d}$$

This mechanism is inversely proportional to the output stage size and is a dominant term in systems with power output over a few watts, showing the validity of equation (1.1). Also, as discussed in section 3.3, it is dominant at high modulation depths. Reducing these losses implies increasing the power stage size.

3.1.2 Capacitive

Capacitive dissipation arises from nodes charging and discharging during switching events. Output nodes and the gates of the large devices present a significant capacitance to be charged. Since there is no "digital logic" per-se within the amplifier, every node has a switching activity factor of 1.0 [16]. These equations only include one bonding pad and halve k_2 and k_3 compared to [2] due to the change to half-bridge.

$$P_{cap} = \frac{1}{2}V_{dd}^2 f_{sw}\left[C_{pad} + (k_2 + k_3)\, W_p T_{sum}\right] \tag{3.3a}$$

$$k_2 = \left(1 + \tfrac{1}{\alpha}\right)\left(C_{ox}L + C_{gso} + C_{gdo}\right) \tag{3.3b}$$

$$k_3 = \left(C_{jp} + \tfrac{C_{jn}}{\alpha}\right) L_{DS} + \left(1 + \tfrac{1}{\alpha}\right)\left(C_{gdo} + 2C_{jsw}\right) \tag{3.3c}$$

Reducing node capacitance and f_{sw} reduces this power dissipation linearly, but

decreases quadratically with supply voltage. Capacitive dissipation is a linear function of power stage size which is in contrast to resistive dissipation ($1/W_p$). Also note that this mechanism is independent of modulation depth, apart from variation of switching frequency versus amplitude in the self-oscillating amplifier.

3.1.3 Short-circuit

Analysis of the dynamic operation of the standard PMOS-NMOS inverter yields a small amount of time during a transition in which both devices are on [16]. Figure 3.1 plots the dynamic behavior of a simple inverter. The supply current shown is only related to the short-circuit current because capacitive switching current is flowing from the output node to ground during a $1 \rightarrow 0$ transition.

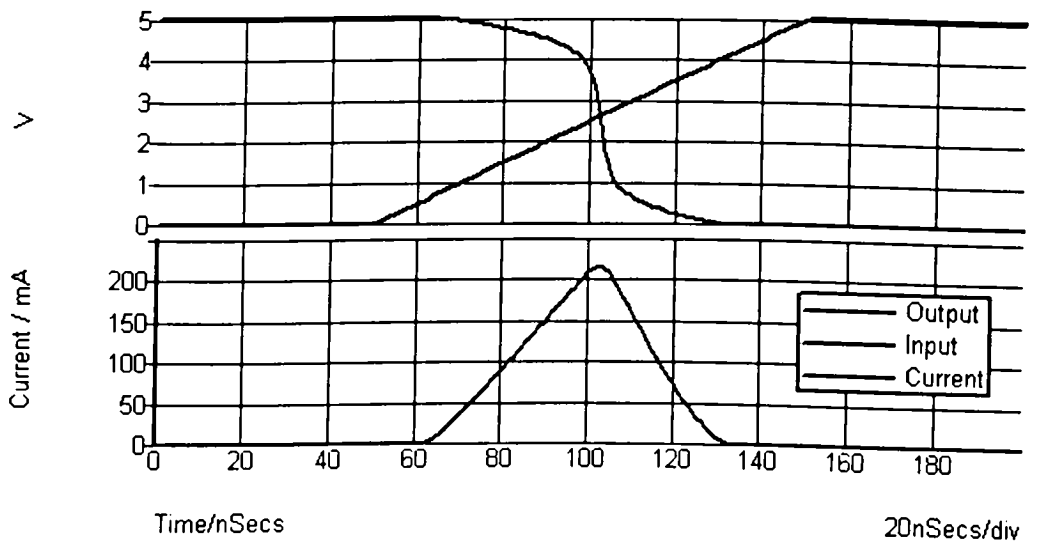

Figure 3.1: CMOS inverter dynamic current plot showing short-circuit current transient during transition

$$P_{sc} = k_5 \left(V_{dd} - 2V_{th}\right)^3 \left(T_{sum} - 1\right) f_{sw} t_r W_p \tag{3.4a}$$

$$k_5 = \frac{C_{ox}\mu_p}{6L} \tag{3.4b}$$

A triangular approximation was made to represent the current pulse during the rise-time of the input. This yields a reasonable approximation that dissipation varies linearly with respect to rise-time t_r, switching frequency f_{sw}, and power stage size W_p.

Along with capacitive dissipation, this mechanism is the cause of the "digital switching noise" that is carefully avoided in high-performance analog systems. Reductions to these mechanisms not only improve efficiency but can reduce high-frequency noise coupling into sensitive analog nodes.

3.1.4 Other Mechanisms

The following power dissipation mechanisms are not typically mentioned in the context of a class D efficiency analysis, [15] and [4] being exceptions. However, they become significant at the milliwatt power levels and low load impedances ($4 - 32\Omega$) typically found in portable devices.

Filter reactance

Given a half-bridge output configuration, reactive inductor ripple current generated by the switching action flows between the power supply and output filter. This current is related to the well known "bus pumping" phenomenon in half-bridge output stages. Unfortunately, even under the unrealistic assumption of a zero-impedance power supply, reactive currents flow through the output devices and inductor ESR

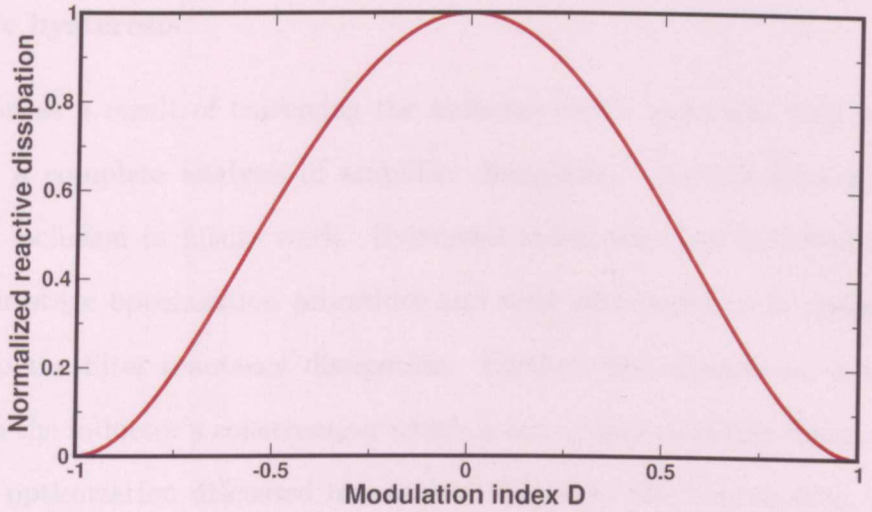

Figure 3.2: Normalized reactive power dissipation versus modulation index.

causing another power dissipation mechanism.

$$P_{react} = (i_{ripple})^2 (R_{on} + R_L) \tag{3.5a}$$

$$i_{ripple} = \frac{D(1-D)V_{dd}}{f_{sw} L \sqrt{3}} \tag{3.5b}$$

In contrast to both capacitive and short-circuit dissipation, this mechanism depends on modulation depth. Dissipation is maximum at idle ($D = 0.5$) and falls to zero at full modulation as shown in Figure 3.2, e.g. dissipation is weighted by the input signal's statistics.

A recent conference paper [4] also discusses ripple current and is the only other mention of this mechanism the author is aware of within a low-power class D context. Nielsen, in [15], discusses inductor-related losses within high power amplifiers where it was included for accuracy, but not as a mechanism with significant contribution.

Magnetic hysteresis

Dissipation as a result of traversing the inductor core's hysteresis loop must be included in a complete analysis of amplifier dissipation. Section 5.2.1 discusses its necessary inclusion in future work. Hysteresis losses were not included in the current power stage optimization procedure and were considered to be insignificant in relation to the filter reactance dissipation. Further, this dissipation is specifically coupled to the inductor's construction which is not a subject of this thesis; the power stage size optimization discussed in section 3.3 ignores this contribution because of its independence from W_p.

Quiescent and other mechanisms

Finally, omnipresent in any amplifier is the power dissipated when idle. Quiescent dissipation in the amplifier presented here occurs only in the comparator and its associated bias-generation network. This term should be well under $100\mu W$ for a well-designed comparator and is included in efficiency calculations as a constant.

Sub-threshold conduction and leakage are not considered in this analysis. Also, losses incurred through the feedback network should be included for greater precision but have been left out of the present discussion.

3.2 Gate Drivers

The large, narrow capacitive and short-circuit current pulses drawn while switching (discussed in section 3.1.3) not only cause excess power dissipation but can be a significant source of power supply noise. It is therefore desirable to reduce or eliminate these currents, not only increasing efficiency but also potentially quieting the supply rails for the rest of the system.

Capacitive current can only be reduced through reducing the minimum gate length by scaling the technology (aside from decreasing W_p) and is largely unavoidable. Short-circuit current can be reduced by careful design. First some background on driving large on-chip loads is covered along with a way of dealing with this short-circuit current.

3.2.1 Background

Inverter Chains

The load presented by the output device gates is very large and capacitive. Typically the solution for driving large on-chip loads (e.g. bonding pads) with minimum delay is a geometrically-sized inverter chain [16]. Figure 3.3 is a graphical depiction of such a chain. This sizing scheme fixes the ratio of the load seen by the previous stage to the drive strength as equal throughout the chain. Varying the "tapering" factor, t, trades total delay for implementation area; typical values being around $t \geq 4$. The number of stages needed is then $N \approx \log_t (C_{load}/C_{in})$ [16], where C_{in} is the input capacitance of the first stage inverter.

In the context of switching and short-circuit current dissipation, this means that there are now $N + 1$ switching nodes. This is the origin of the T_{sum} term in equation (3.4), as all other transistors are sized parametrically from the PMOS output device.

Dead Time

Given that the short-circuit current originates when both devices are simultaneously on, this situation can be avioded by guaranteeing that only one device is on at any given time. Table 3.2.1 shows the desired additional state, commonly called "dead time." This dead time state is critical in large systems employing discrete transistors

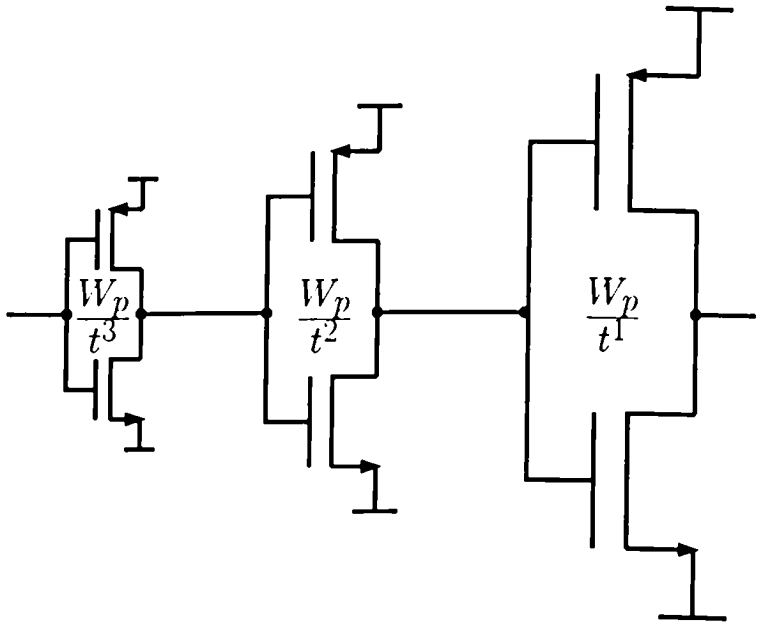

Figure 3.3: Geometrically-sized inverter chain for driving large loads, $t > 1$.

Table 3.1: Insertion of additional "dead time" state in output stage transition

State	NMOS	PMOS	
1	on	off	t_{low}
$\Longrightarrow$2	off	off	t_{dead}
3	off	on	t_{high}

where short-circuit current could exceed tens or hundreds of amperes, destroying components and generating extra electromagnetic interference (EMI).

During the dead time, current flowing in the inductor will cause the MOSFET's body diode to conduct. This must be considered when adding the extra state. Finally, dead time causes extra distortion in the open loop amplifier which varies nonlinearly with input signal amplitude [17]. These factors make dead time generation a balance between short-circuit current, body diode conduction, and (open loop) distortion.

3.2.2 Modification

Dead time is created by separating the drive to each output transistor. This allows separate on/off control for the P and N switches allowing control over dead time. One way to achieve the OFF-OFF state is to turn each device on slowly and off quickly.

Creating this condition in a CMOS process is easy. Propagation delay through an inverter is a strong function of drive strength (size) and load (output device gate size). Varying the drive strength is a simple matter of changing the size of the inverter driving the load. Therefore non-symmetrical rise/fall (on/off) times can be created by skewing the P/N ratio by "skew" parameter s. Usually this ratio is set to $\alpha = \mu_n/\mu_p \approx 3$ for symmetrical delay or ≈ 2 for minimum average delay.

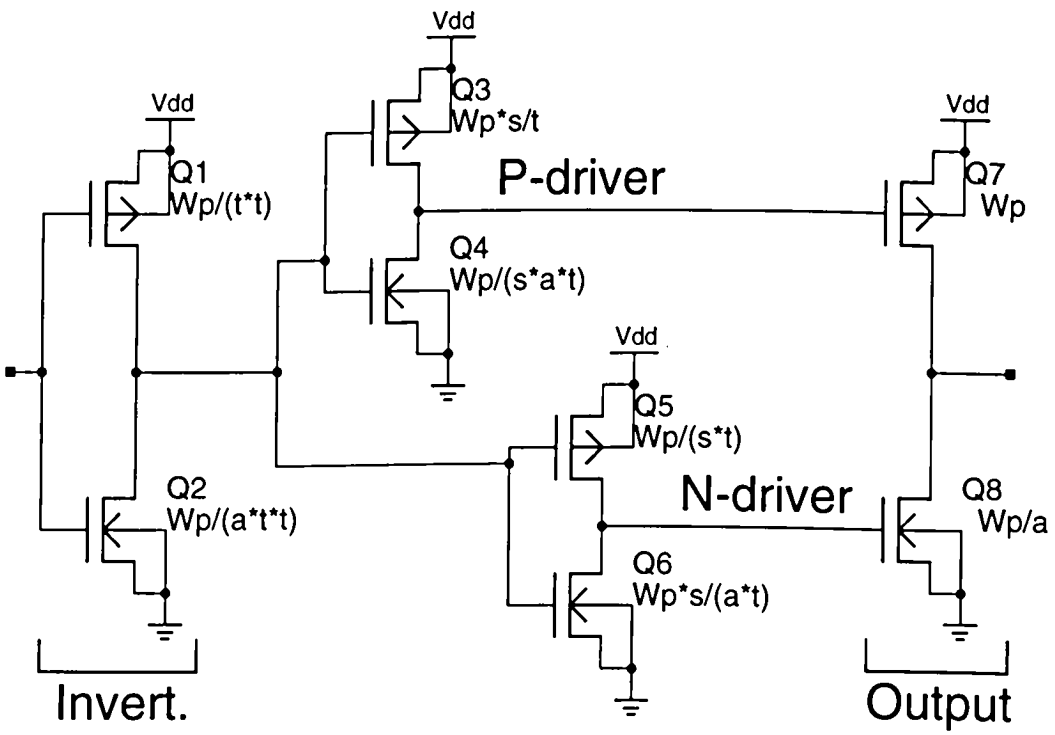

Figure 3.4: Modified gate drivers to simply generate dead time in output devices. Channel lengths are minimum. (a = α)

Figure 3.4 shows a schematic of the modified gate drivers. A non-parametric version of this circuit was previously mentioned in [8]. Each output device is now

driven separately by an appropriately sized inverter which causes slow "on" and fast "off" transitions. Sizing of the entire power stage and drivers can be parametrized from the P transistor size, using W_p, α, t, and s. This allows a partial separation of design parameters from physical dimensions (efficiency, R_{on} symmetry, the tapering factor, and dead time, respectively).

Though the modified gate drivers in Figure 3.4 are placed immediately before the output devices, they are not constrained to that location. The purpose of separating the gate drive signals is only to implement a transition-dependent delay. Also, the single inverter shown may itself represent a chain of inverters. The effects of positioning this simple dead-time generator within the inverter chain on power dissipation and delay precision have not been studied; section 5.1 discusses future research directions for this modification.

3.3 Optimization

Figure 3.5 graphically shows the effects of an improperly sized output stage for a 16Ω load. Efficiency was calculated using process parameters from the fabricated design and equations given in section 3.1. At large modulation indices, efficiency increases as the power stage size increases. However at low output levels, efficiency is greater for smaller output devices. Maximum power dissipation is dominated by the resistive mechanism, as shown in equation (3.2), while at low output levels dissipation is dominated by the capacitive switching, short-circuit, and inductor ripple current mechanisms, shown in equations (3.3), (3.4), and (3.5), respectively.

Optimization of the efficiency with respect to the power stage size implies minimizing the power dissipation mechanisms. Equation (3.6) shows the general approach.

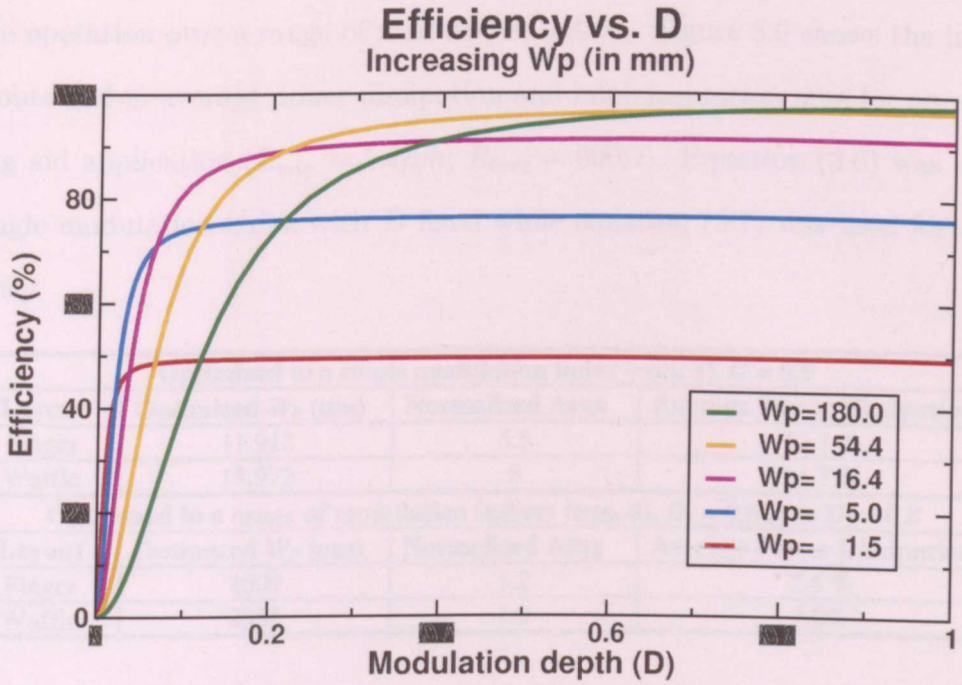

Figure 3.5: Efficiency versus D for various output stage sizes

$$\eta(W_p, D) = \frac{1}{1 + (P_{diss}/P_{load})} \tag{3.6a}$$

$$P_{diss}(W_p, D) = P_{res}(W_p, D) + P_{cap}(W_p) + P_{sc}(W_p) + P_{react}(W_p, D) \tag{3.6b}$$

$$\frac{\partial}{\partial(W_p, D)} P_{diss}(W_p, D) = 0 \tag{3.6c}$$

3.3.1 Previous Approach

Chang, et al. [2] analyzed the power dissipation mechanisms within the chain-of-inverters class D output stage. Their analysis assumed a full-bridge topology and constant switching frequency. Comparisons were made between the "finger" and "waffle" layout techniques. Their conclusion was almost equal efficiencies can be attained using either technique, but the waffle layout used about 12% less IC area.

Key to the analysis was the observation that a better efficiency metric should

include operation over a range of modulation indices. Figure 3.6 shows the improvement obtained in average power dissipation and implementation area for an example hearing aid application ($L_{min} = 1.2\mu m$, $R_{load} = 600\Omega$). Equation (3.6) was used for the single modulation index with D fixed while equation (3.7) was used for average efficiency.

Optimized to a *single* modulation index (eqn. 1), $D = 0.9$			
Layout	**Optimized W_P (μm)**	**Normalized Area**	**Average Power Dissipation**
Finger	11,913	5.8	12.1 %
Waffle	13,972	5	11.7 %
Optimized to a *range* of modulation indices (eqn. 4), $D_1 = 0.025$ to $D_2 = 0.8$			
Layout	**Optimized W_P (μm)**	**Normalized Area**	**Average Power Dissipation**
Finger	2609	1.2	7.4 %
Waffle	2965	1.0	7.0%

Figure 3.6: Comparison of output stage design optimized to a single D and a range of D's in a $1.2\mu m$ process, from [2]

$$\eta_{avg}(W_p) = \frac{1}{D_2 - D_1} \int_{D_1}^{D_2} \eta(W_p, \delta) d\delta \tag{3.7a}$$

$$\frac{\partial}{\partial W_p} \eta_{avg}(W_p) = 0 \tag{3.7b}$$

3.3.2 Modification

The previous approach can yield impressive gains in both average efficiency and implementation area and goes a long way to providing a framework for class D power stage design. However, several modifications are needed to both update the procedure and better tailor the optimization to real-world conditions, specifically to portable media devices.

Additional dissipation mechanisms

The first modification is to include the additional power dissipation mechanisms from section 3.1.4 into the optimization equations. These should be included both for accuracy considerations and because they are nonlinearly dependent on modulation depth. Besides the resistive dissipation, the other mechanisms are proportional to device size and usually most pronounced at zero input in a self-oscillating topology.

Modulation index distribution

Implicitly assumed while optimizing over the range of modulation indices in [2] was a uniform signal amplitude distribution. The probability density of D is identical to the input signal statistics when the amplifier is not clipping and is rarely uniform.

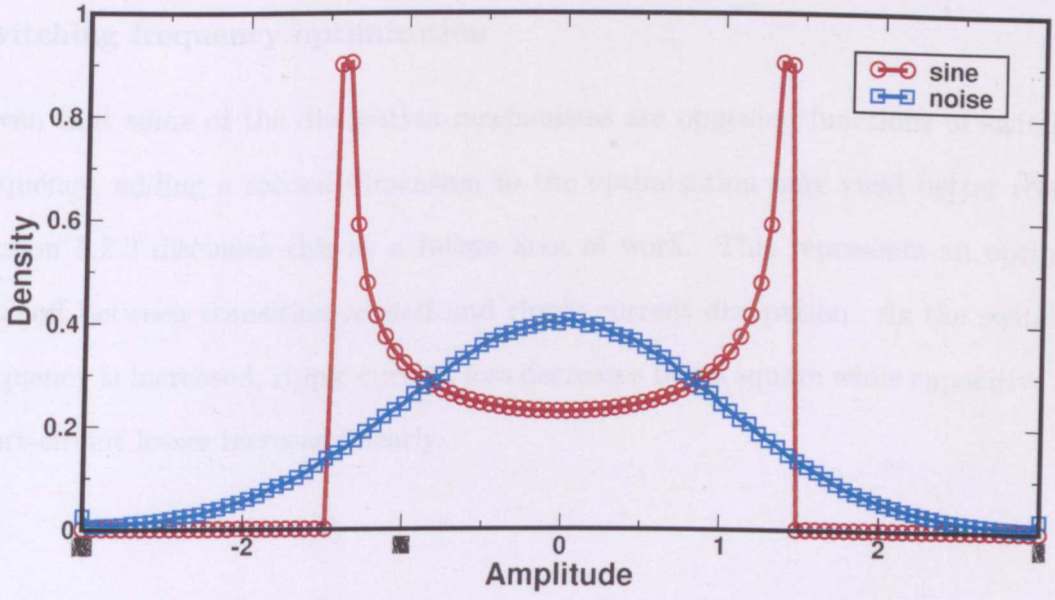

Figure 3.7: Amplitude distributions for sinewave and noise signals at 1V RMS

Figure 3.7 plots equal-power amplitude histograms for a sinusoidal signal and a Gaussian noise signal. Temme and Brunet use these distributional differences to help explain why distortion metrics vary with input signal type in [5] due to the very nature

of nonlinear systems. The same reasoning applies to efficiency measurements, where efficiency is a function of the modulation depth. This means that given any amplifier class with an increasing efficiency versus modulation curve (the author knows of none that do not), the efficiency measured with a sinusoidal input will always measure higher than noise (or music) of equal power content due to the heavy weighting at the maxima for sinusoids.

Quoted efficiency measures such as "92% efficient at 100W output" should specify the test signal. Unless driven into clipping, an amplifier cannot obtain these sinusoidal efficiency levels with typical input signals. Since the whole point of optimizing the output stage is to obtain higher *real-world* efficiencies, it follows that design and testing for efficiency should use signals similar to the target application.

Switching frequency optimization

Given that some of the dissipation mechanisms are opposing functions of switching frequency, adding a second dimension to the optimization may yield better results. Section 5.2.2 discusses this as a future area of work. This represents an optimum tradeoff between transition-related and ripple current dissipation. As the switching frequency is increased, ripple current loss decreases by its square while capacitive and short-circuit losses increase linearly.

Chapter 4

Implementation

An amplifier utilizing the basic LC phase-shift topology and optimized using a technique similar to [2] was designed and fabricated in a standard $0.5\mu m$ CMOS technology. Simulations and testing confirmed the viability of mapping this topology to chip-scale dimensions.

4.1 Design

The target application for this design was a stereo amplifier for headphones within a portable device. Given that almost all headphones use a three wire connection scheme (left, right, and common return), each channel was constrained to a half-bridge output stage.

Normally, the common return is connected to the system ground and the outputs AC-coupled for single supply operation as split power supplies are uncommon in portable applications. A new IC [22] includes an optional $V_{dd}/2$ output to allow DC coupling of the headphone connection, eliminating the large coupling capacitor; this section does not use a class D amplifier, however.

It is possible to drive the return line with the "sum" signal and drive the Left

and Right channels by complementary "difference" signals resulting in a pseudo Mid-Side configuration where the headphones perform the conversion back to Left-Right. Effectively this gives a bridged output for the mono signal and half-bridge output for the difference signal. Appropriate signal processing could then ensure that none of the channels are overdriven by balancing power content in the sum and difference signals. It is unknown whether this technique can give greater overall efficiencies even when including the extra power stage and signal processing.

4.1.1 Channel

Figure 4.1 shows a block schematic of an amplifer channel. In this circuit, the comparator operates with a small common mode range centered around $V_{dd}/2$. Since the system's DC offset is blocked by the necessary coupling capacitor, and shorter delay generates faster than desired switching frequencies, the comparator's requirements can be relaxed. Switching frequency was targeted to be around 300kHz and simulations confirmed the fact that a high-performance comparator was unnecessary. Therefore, a simple two-stage op-amp was used for the comparator block.

The power stage size W_p was chosen to be $5.19mm$ through the procedure modified from [2]. A semi-empirical approach averaged the calculated optimum sizes for several typical loads to obtain the final value. Section 5.2 discusses future work for finding a practical optimization method. The tapering factor and skew parameter used to size the gate drivers were 10 and 4.5 respectively, the P-N ratio α was set to 3.

Given the large tapering factor, only a single inverter was required to drive the split gate driver inverters as shown. Larger output devices or smaller delay through the power stage would require a longer chain with a smaller tapering factor. Simulations showed that the current design was sufficient for the given application.

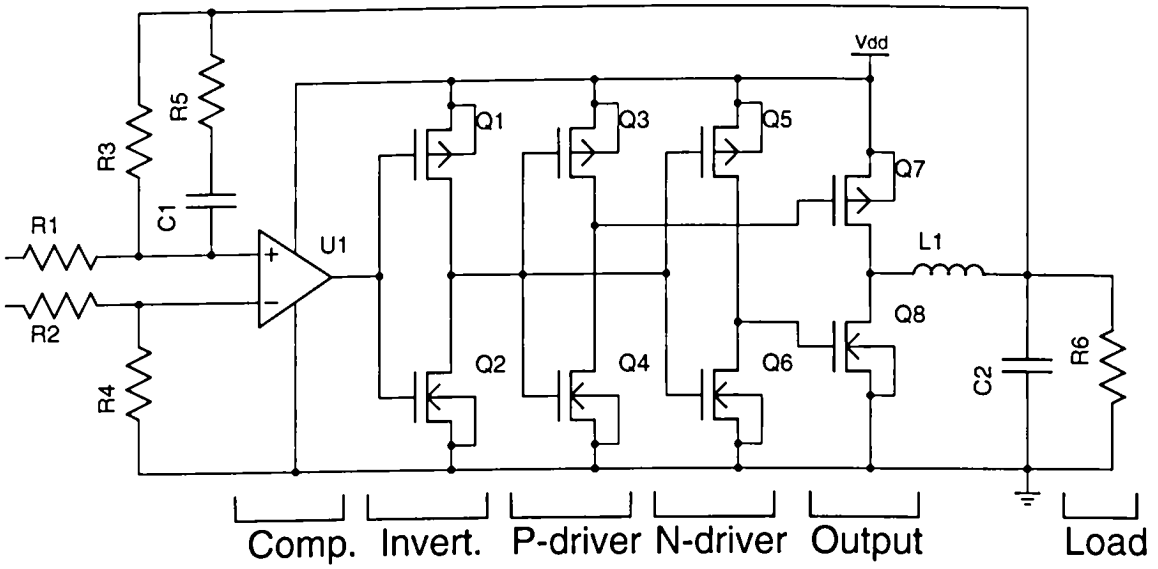

Figure 4.1: Schematic of fabricated amplifier

4.1.2 Bias Generator

The opamp bias was generated by a standard asymmetrical cascode current mirror with an external resistor. Bias loop startup was guaranteed by a simple level sensitive current shunt; the complete generator is shown in Figure 4.2. External switches were used to provide on-off bias control to each half of the chip which allowed testing only two channels at a time.

To aid in the testing phase, the relationship between generated bias current and external resistor value was simulated, shown in Figure 4.3. Given the two-stage opamp used for the comparator, bias current is proportional to delay and is useful for tuning the switching frequency.

4.1.3 Layout

Mask layout was performed in both Cadence and Magic to facilitate workflow, the layout for a single channel is shown in Figure 4.4. Though the waffle layout technique was recommended in [2], large transistors were drawn fingered due to the MOSIS

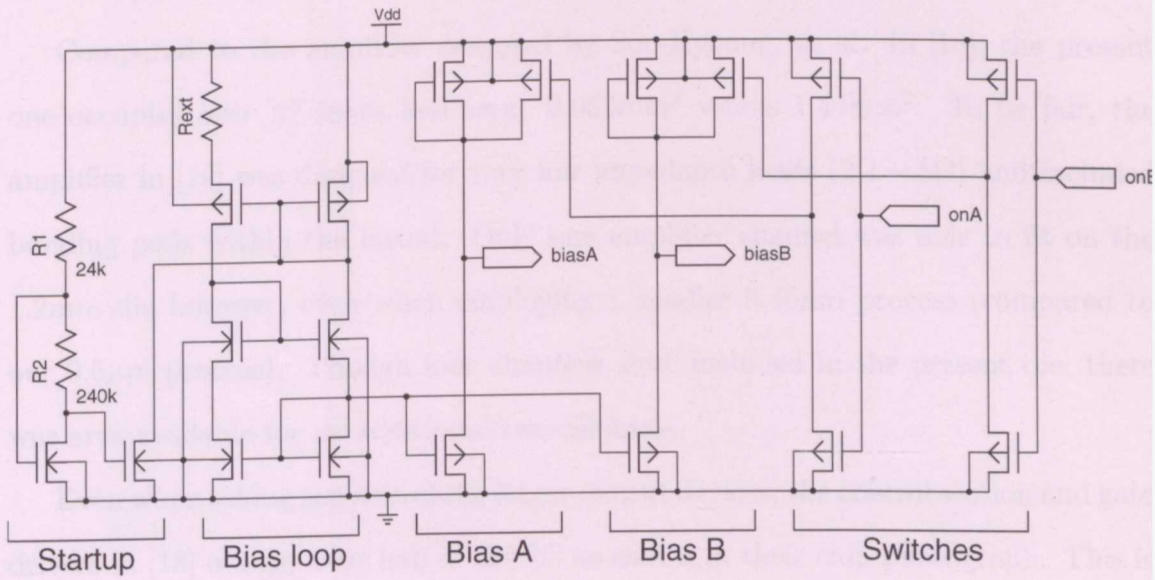

Figure 4.2: Bias generator and startup circuit

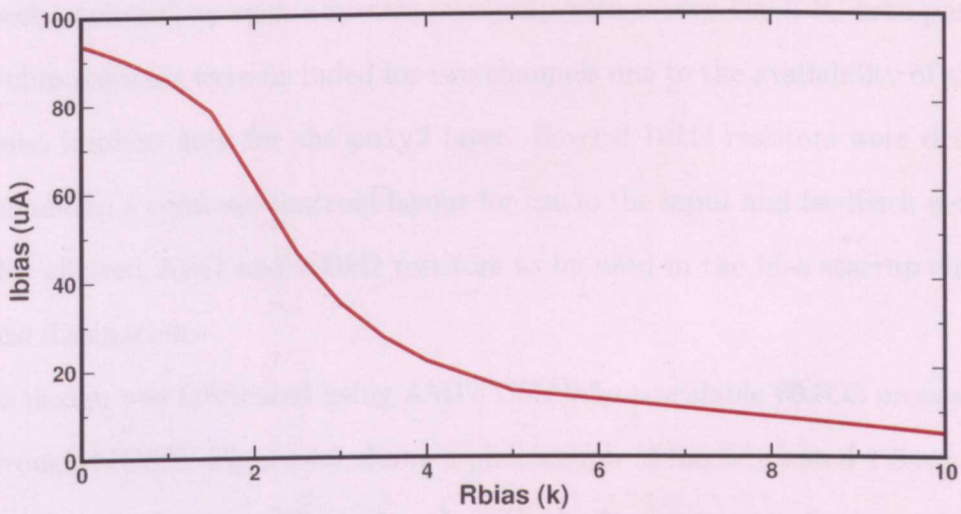

Figure 4.3: Generated bias current versus R_{ext} simulation.

constraint of Manhattan-only geometries. Each channel measures $260\mu m \times 200\mu m$ and occupies $0.052mm^2$.

Compared to the amplifier designed by Soo-Hyoung, et al. in [18], the present one occupies *over 27 times* less area: $0.052mm^2$ versus $1.44mm^2$. To be fair, the amplifier in [18] was designed for very low impedance loads ($2\Omega - 8\Omega$) and included bonding pads within the layout. Only one amplifier channel was able to fit on the $1.2mm$ die however, even when employing a smaller $0.35\mu m$ process (compared to our $0.5\mu m$ process). Though four channels were included in the present die, there was area available for an additional two channels.

Even when taking account of the larger output devices, the control section and gate drivers in [18] occupy over half of the IC as shown in their chip photograph. This is in stark contrast to the present design where output devices occupy the vast majority of the channel area. Though performance is good, the additional area consumed by the design in [18] could prevent it from being included on the same die as the rest of a portable media chip, increasing system size and cost. The design presented here can be directly included on such a system-on-a-chip with a very small IC area penalty.

On-chip resistors were included for two channels due to the availability of an extra high-resist implant step for the `poly2` layer. Several $10k\Omega$ resistors were drawn for each channel in a common centroid layout for use in the input and feedback networks. This also allowed $20k\Omega$ and $200k\Omega$ resistors to be used in the bias startup circuit to minimize dissipation.

This design was fabricated using AMI's C5N $0.5\mu m$ scalable CMOS process available through MOSIS. Figure 4.5 shows a photograph of the fabricated $1.5mm$ die. It clearly shows the four amplifier channels with the bias generator in the center. The left two channels included on-chip passive components ($R1 - R5$ and $C1$ in Figure 4.1), requiring that only the LC output filter be external.

Figure 4.4: Channel layout in Cadence AMS

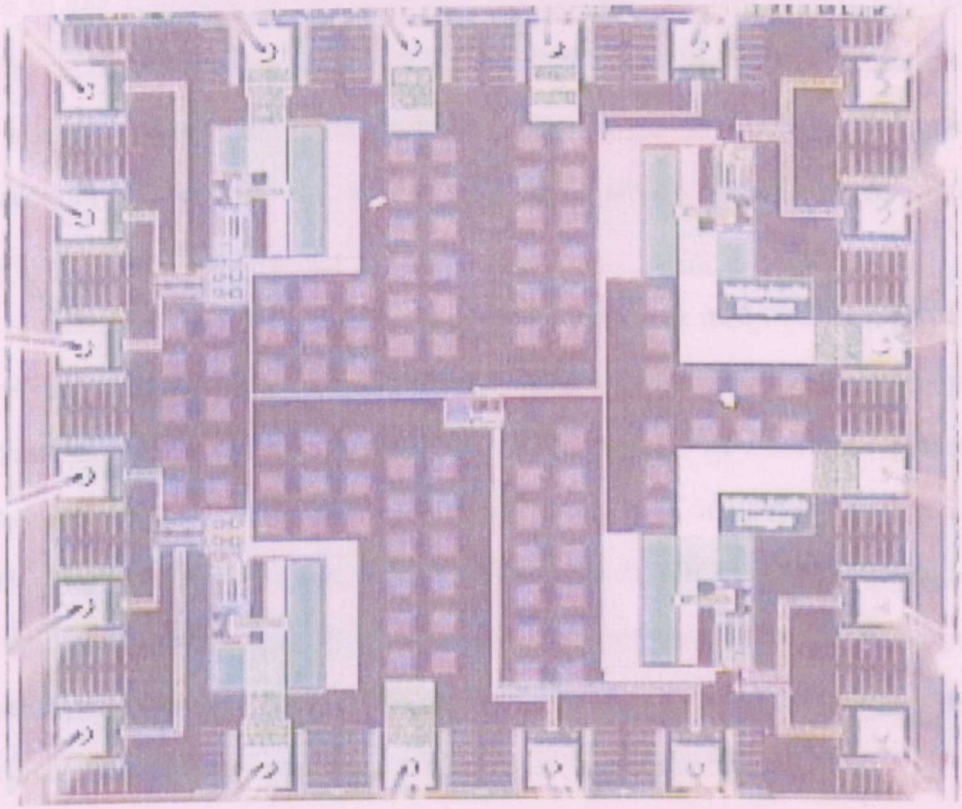

Figure 4.5: Chip photograph of fabricated die, 1.5mm square.

The checkerboard pattern seen over the die are `substrate-nwell-poly1-poly2-metal1` power supply bypass capacitors that also fulfill the chemical-mechanical polish process step's minimum layer density requirements in otherwise unused areas. Custom padframe cells were also designed that included `substrate-nwell-poly1-poly2` capacitors between the bonding pads for additional bulk capacitance. By utilizing a large portion of the unused die area for bypass capacitance, there was over 400pF of on-chip charge storage available for transient current flow.

4.2 Simulation

System and channel simulations were performed with Synopsys' HSPICE software. Transistor models provided by MOSIS were extracted from recent fabrication runs.

Due to the topology of this amplifier, there exists no convergent DC operating point for simulation purposes. Some self-oscillating and bi-stable circuits do have a stable operating point and must be disturbed to begin oscillating. No such condition exists for this amplifier, guaranteeing a rapid oscillation startup as soon as the comparator begins functioning.

All simulations must be run in the time domain and be initiated with a set of node voltages and currents. The initial node set was set to be close to the idle operating conditions; this allowed rapid convergence to the average idle inductor currents and capacitor voltages. Transient simulation ran at a rate of about $100\mu s/min$ when using the `.option fast` switch. This option causes HSPICE to skip the updating of nodes that change very little, reducing amplitude accuracy in the switching portions. Simulation without the `.option fast` switch was only used for startup and lead network calculations and was approximately 20 times slower.

4.2.1 Netlist Reduction

Simulations were performed using a netlist extracted from the chip layout. Fingered transistors were extracted as individual transistors connected in parallel. The same was true for parasitic and drawn capacitors. This resulted in a huge number of elements to be simulated.

To reduce simulation time, a Python script [3] was created which combines parallel capacitors and MOSFETs and deletes capacitors smaller than an optional value. The script takes advantage of HSPICE's "m" parameter which emulates multiple identical elements in parallel by scaling device currents. This technique was not used for capacitors to allow easier visual inspection of the netlist for parasitic internodal capacitance values.

Table 4.1: Results of pre-processing extracted netlist with `pyspice.py`. All (combined) capacitors smaller than 100fF were dropped.

# elements	Before	Combined	Dropped	After
Capacitors	910	380	299	231
MOSFETs	722	616	-	106
Total:	1632			337

Table 4.1 shows the almost five-fold reduction in netlist elements obtained by pre-processing. From inspection of the netlist, extracted capacitors smaller than about 100fF were mostly extracted from wiring overlap and node-to-bulk capacitances. Though this would degrade simulation accuracy, those capacitances were deemed to make such degradation insignificant given the relatively low frequencies encountered in the project.

MOSFET combination was anticipated to give the greatest simulation speed increase because there is only one model evaluation per effective device per time step instead of "m" calculations per parallel transistor. No accuracy degradation was an-

ticipated by the parallel combination operation since on-chip interconnect impedance was not modeled.

4.2.2 Efficiency

Efficiency was measured using two cycles of a 1kHz sinusoidal tone. Transient simulations were run for various input amplitudes and average supply current and RMS load current were measured. Only one extracted channel and the bias generator was included in the netlist to reduce simulation times. Output filter cutoff was fixed at 30kHz and filter characteristic impedance set to 32Ω, critically damped by the 32Ω load impedance. This yielded filter values of $167\mu H$ and $0.169\mu F$.

Figure 4.6 shows simulated efficiency for several typical loads. Similar to the $W_p = 16.4mm$ line in Figure 3.5, efficiency increases rapidly with output power initially and levels to the maximum. This allows higher efficiency even at low output levels.

4.2.3 Distortion

Distortion measurements were made by simulating 20 cycles of a sinusoidal tone at several frequencies at an output power of 10mW. Given a typical headphone efficiency of 104dBSPL/mW (Sony MDR-Q66LW ear clips), this output power corresponds to a very loud 114dBSPL. Harmonic amplitude calculations were made using the `.disto` and `.fft` commands provided by HSPICE.

The `.option fast` switch was used in these simulations, as in the others, and it is predicted that distortion figures are slightly worse as a result. Given that the distortion versus frequency simulations used around 32 hours of CPU time with the switch enabled, they may still be running had the switch not been used!

Figure 4.7 shows simulated total harmonic distortion for two typical supply levels.

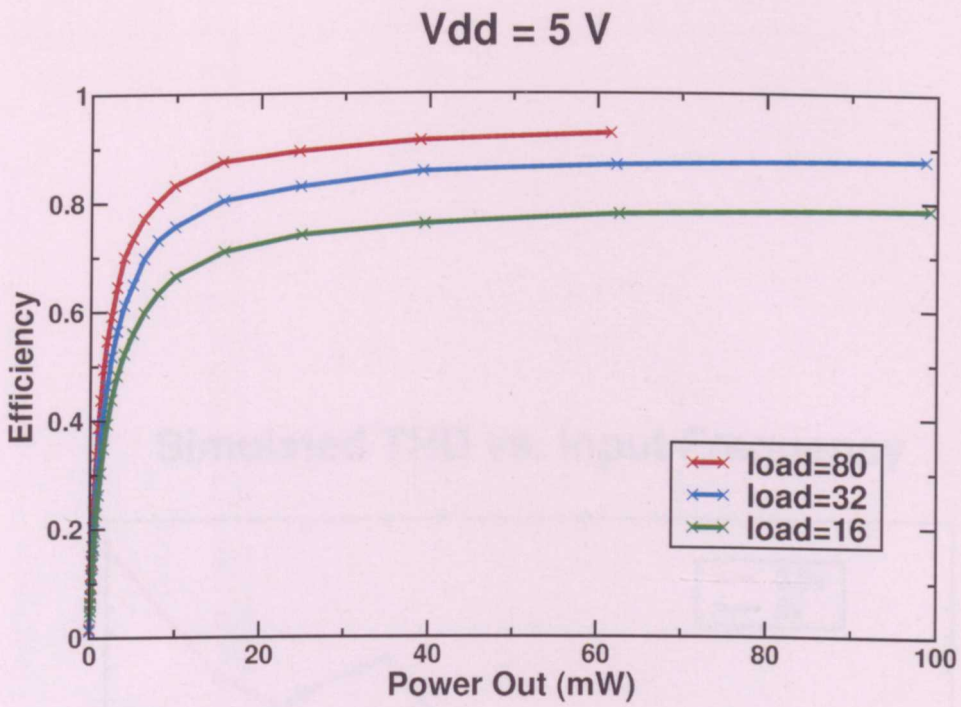

Figure 4.6: Extracted netlist efficiency simulations

Distortion generally decreases for increasing input frequency partially due to the attenuation found in the output filter. Values around 0.1% were expected for this amplifier, given its low estimated loop gain of 34 dB. Extra passive or active poles in the amplifier would have reduced distortion figures in proportion to the extra loop gain provided.

4.3 Testing

A printed circuit board (PCB) was designed and built to allow testing of the fabricated amplifier. Figure 4.8 is a photograph of the test PCB, the amplifier is in the center. The board included a rail-to-rail instrumentation amplifier for each channel input and a separate low-dropout (LDO) voltage regulator for the chip itself. Regulator voltage was variable over the range of $2.7 - 5.5V$ to test performance over typical supply values.

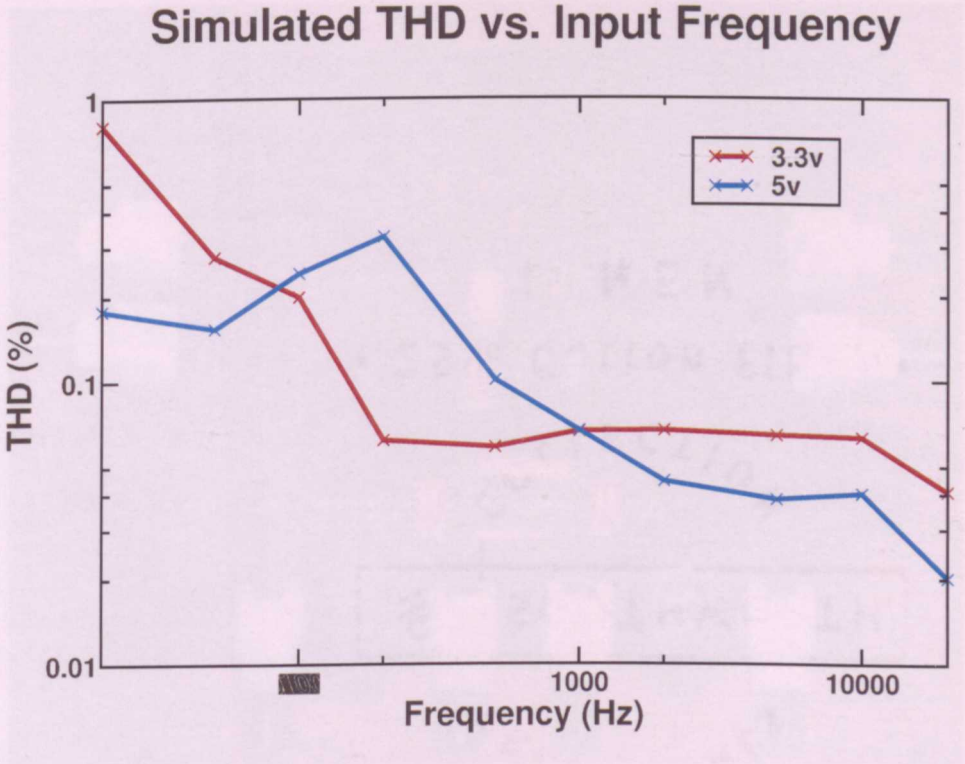

Figure 4.7: Extracted netlist Total Harmonic Distortion simulations for a single channel

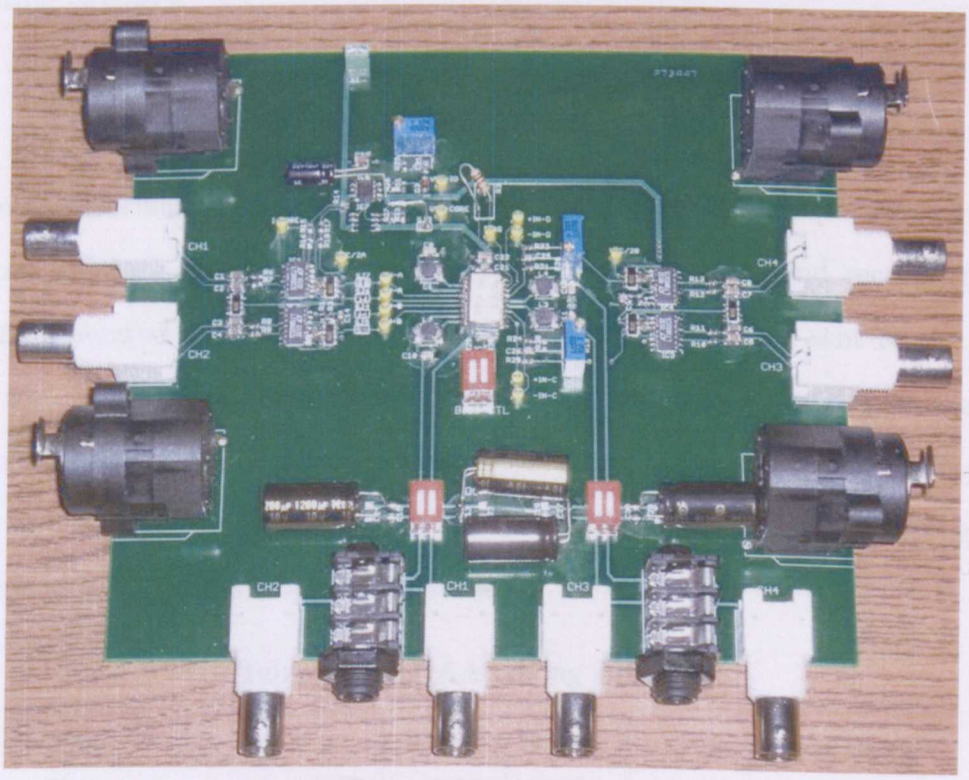

Figure 4.8: Photograph of PCB for testing fabricated amplifier

Several opamps were used to provide a stable $V_{dd}/2$ reference to bias the input signals for single-supply operation. A series resistor was inserted into the chip's LDO regulator input to use a current sense amplifier for measuring supply currents drawn by the chip only. Unfortunately, the LDO regulators selected for the test board required heavier compensation than was initially provided for output stability. Necessary modifications to the PCB required disabling the on-board supply current measuring circuitry.

4.3.1 Dynamic Performance

Dynamic performance tests were performed using the *RightMark Audio Analyzer* (RMAA) software and a PC soundcard for signal generation and recording. The software generated a series of tones and noise signals which are sent to the device under test and the amplified signals recorded. A facility is provided to overlay a number of tests for comparison. Relevant plots are then generated and displayed for review and saving. Table 4.3.1 summarizes test results at several supply voltages and includes the soundcard's loopback response.

Table 4.2: RMAA testing summary.

Test:	**2.85V**	**3.30V**	**5.00V**	**Loopback**
Frequency response, dB 40 Hz – 15 kHz	+0.08 -0.11	+0.03 -0.11	+0.09 -0.37	+0.04 -0.21
Dynamic range, dB (A)	43.9	51.7	47.9	77.3
THD, %	0.851	0.053	0.261	0.0081
IMD + Noise, %	1.062	0.218	1.232	0.043
Stereo crosstalk, dB	-50.8	-58.2	-43.4	-73.1

Input signals were set such that 0dBFS corresponded to the onset of amplifier clipping. Recording levels were attenuated, due to the amplifier gain of 6dB, to

optimize the signal to noise ratio of the soundcard's ADC; full scale input signals suffered from excess distortion. There was a measurement "sweet spot" when $V_{dd} = 3.3V$ that caused significantly lower noise and distortion levels. This may be partially attributed to inter-channel f_{sw} synchronization discussed in [6] but its true origin is unclear.

Informal headphone listening tests revealed a somewhat high noise floor and switching frequency intermodulation products at specific supply voltages. Though the noise floor was higher than desired, distortion was not clearly audible with either test tones or music samples. Given maximum power output of over $60mW$, the amplifier was able to drive the headphones used for testing to a volume far greater than typical listening levels, even considering their below-average efficiency of 95dBSPL/mW and above-average impedance of 64Ω.

Frequency response and crosstalk

Figure 4.9 shows the measured frequency response of the amplifier. It shows no significant variations beyond the response of the soundcard itself. The cause of the rapid variations for the $V_{dd} = 5V$ curve is unclear. Figure 4.10 plots stereo crosstalk as a function of frequency. Though the crosstalk is on the order of a stereo LP record (around -40dB), the amplifier has a flatter response than the soundcard at low frequencies. It should be pointed out that all on-chip signals were single-ended and as such are more sensitive to coupling, converting the feedback network to use differential signals should both reduce crosstalk and coupled switching noise.

Distortion and noise

The RMAA software measures several kinds of distortion including total harmonic distortion plus noise (THD+N) and intermodulation distortion plus noise (IMD+N).

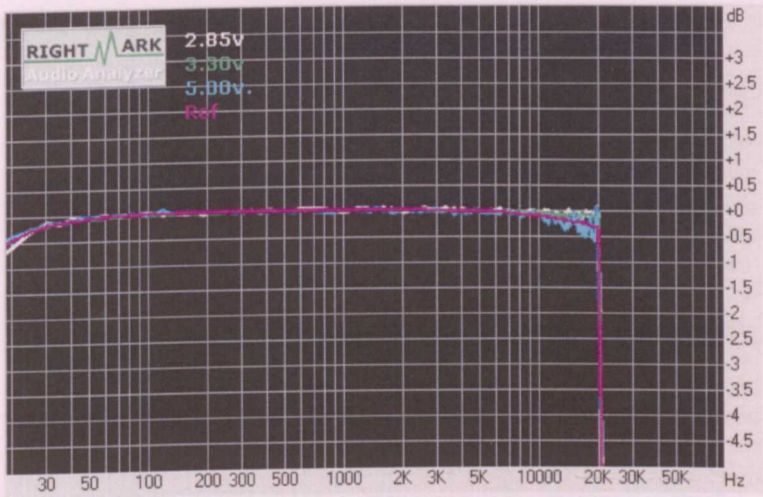

Figure 4.9: System frequency response for several supply voltages.

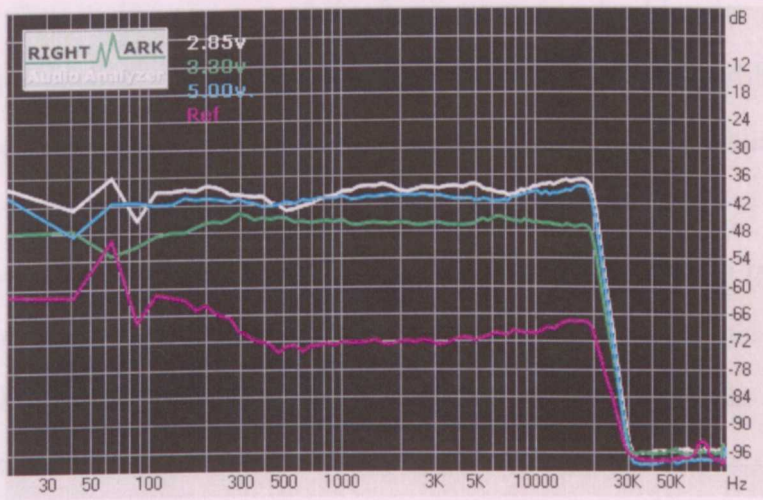

Figure 4.10: Stereo crosstalk versus frequency measurements.

Figure 4.11 plots the output noise spectrum with no input. The output noise is definitely audible, especially at $V_{dd} = 5V$ and is minimum at $3.3V$ but is relatively flat through the entire audio range as expected.

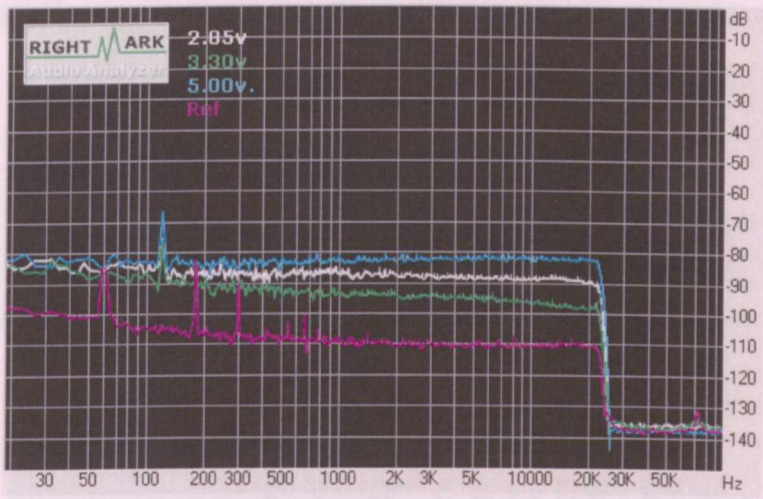

Figure 4.11: Output noise spectrum with no signal input.

Interestingly, the line frequency related peaks do not show up in both the loopback and amplifier plots as would be expected. There are two explanations for this phenomenon. First is the absence of the fundamental and odd-order line harmonics in the amplifier output. These harmonics are suppressed by the differential input implemented on the test PCB which reject common-mode noise while the loopback connection is single-ended.

Finally, the second line harmonic at 120Hz is most likely due to rectified ground currents flowing in the signal shields. This has been dubbed the "pin 1 problem" in reference to the standard XLR3 audio connector's shield connection to pin 1. It is a direct result of common-impedance coupling of shield currents into signal circuits and poor design. A recent standard has been adopted that specifically deals with this issue [21]. The origin of the current is likely due to capacitive coupling within the transformer "wall wart" used to provide power to the test board.

The distortion plus noise spectrum for a 1kHz input signal at −3dBFS is shown in Figure 4.12. Dominant harmonics are the 2^{nd} and 4^{th}, indicating an asymmetry in the amplifier. Causes of this asymmetry have not been investigated. The signal peaks above 40kHz are aliasing byproducts of the switching frequency.

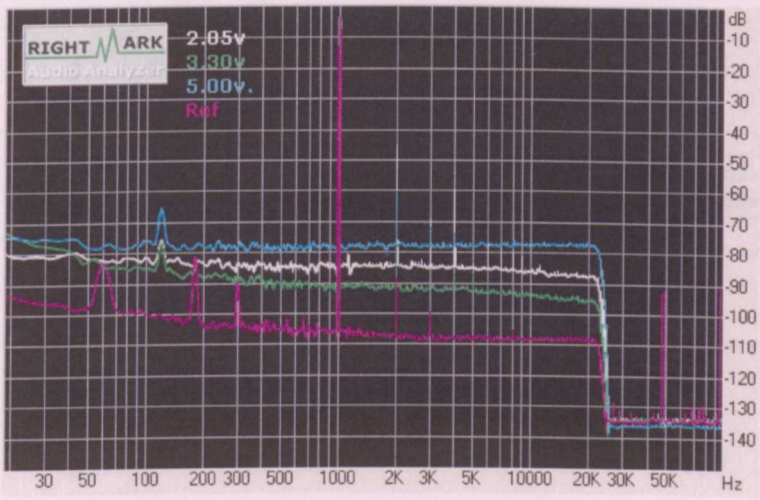

Figure 4.12: THD+N distortion spectrum at f_{in} = 1kHz, −3dBFS

4.3.2 Efficiency

Measurements of efficiency were taken by measuring test board supply current and load RMS voltage for various sinusoidal input amplitudes at 1kHz. Loads were 15Ω and 33Ω resistors connected directly to the headphone jack provided by the board. Ignoring reactive effects, these loads represent typical headphone impedances.

Since the current-sense circuit was disabled, supply current was measured with an ammeter in three states: bias off, no input signal, with input signal. Efficiency was calculated using equation (4.1). Figures 4.13 and 4.14 show measured efficiency for the two loads with supply voltages of $5V$ and $3.3V$, respectively.

$$\text{Efficiency}(\%) = 100\frac{(V_{loadRMS})^2/R_{load}}{V_{dd}(i_{sig} - i_{off})} \tag{4.1}$$

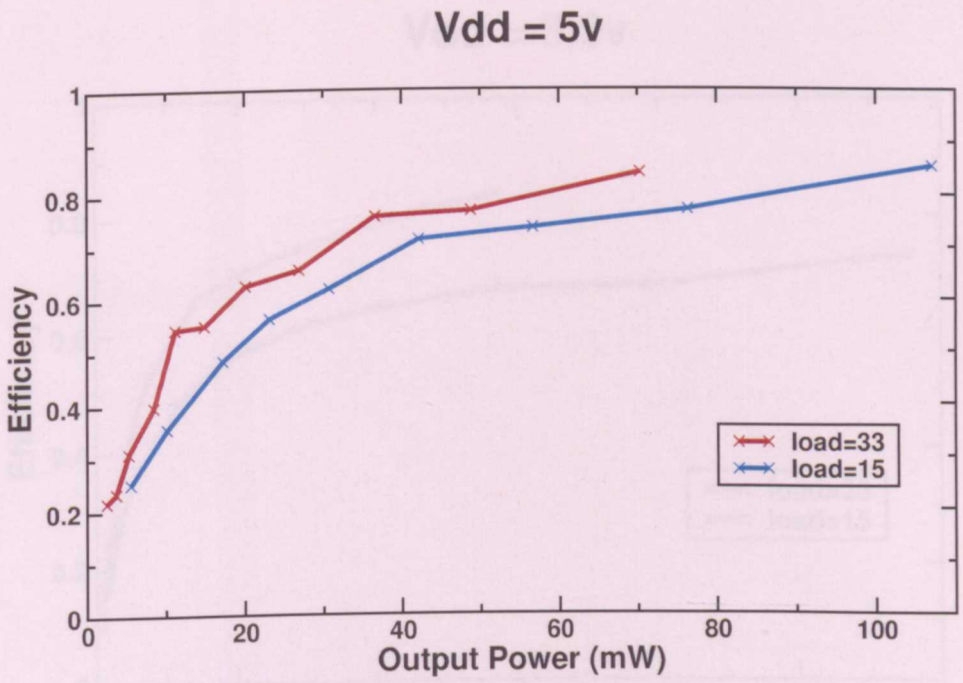

Figure 4.13: Efficiency measurements of test board

Comparing the two measured efficiency figures at similar output power levels, efficiency is greater with lower supply voltages. Primarily this is due to the capacitive and short-circuit losses that decrease quadratically with supply level. Also, increased load impedance increases efficiency as predicted.

While maximum efficiency is somewhat close to that predicted, performance at lower output levels is much poorer than predicted. The effects of inductor and capacitor ESR and supply impedance were not included in the simulations. Both of these dissipation mechanisms reduce efficiency at low modulation depths as described in section 3.1.4 and partially account for the discrepancy.

Finally, the multimeters used for the current measurements did not specify the frequency response of the ammeter function. There are supply currents at not only the signal frequencies but at harmonics of the $\approx$ 280kHz switching frequency. Inaccuracy in this measurement has a direct effect on efficiency calculations, especially since two different (but same model) meters were used for the measurements in two different

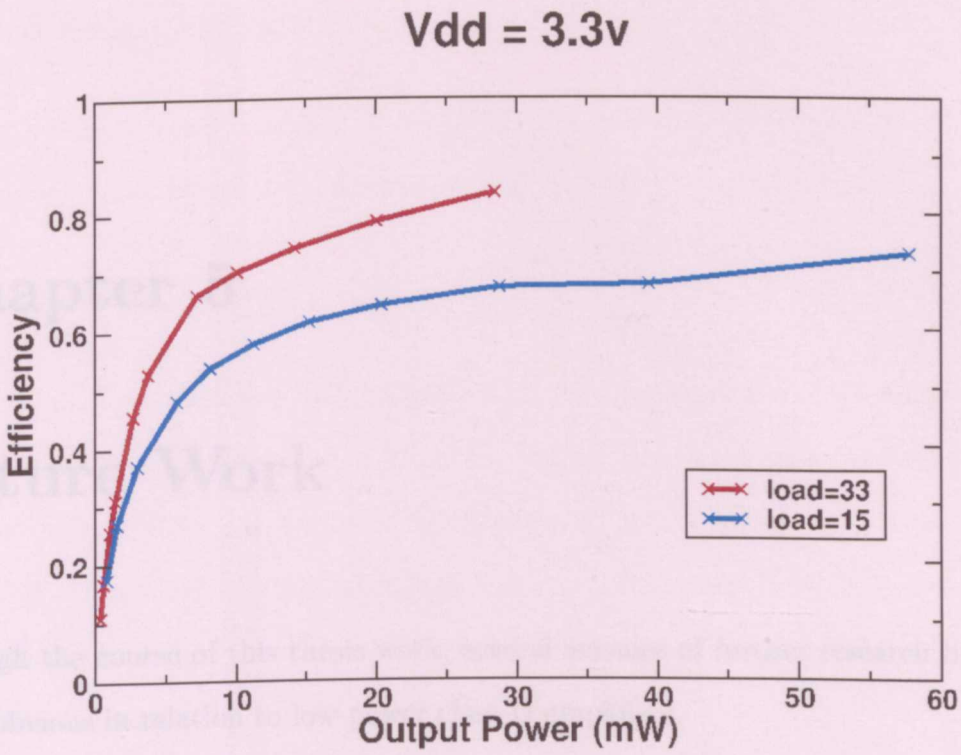

Figure 4.14: Efficiency measurements of test board

modes, load voltage and supply current, for calculation.

Chapter 5

Future Work

Through the course of this thesis work, several avenues of further research have become obvious in relation to low power class D amplifiers.

5.1 Dead Time

The split in the gate driver path from the standard chain of inverters was made immediately before the power devices. Since the purpose of the split is to create asymmetrical turn on/off delays, it is necessary that one of the transitions be longer than typical. From the short-circuit dissipation equations (3.4), it is desirable to have fast rise/fall times within an individual inverter. Given that short-circuit dissipation is also proportional to inverter size, it may be advantageous to generate the asymmetry earlier in the chain where devices are smaller.

Creating the dead time delays earlier in the chain would allow a reduction of the rise/fall times in the following inverters at the expense of more inverters in the parallel N-drive and P-drive chains. Tunable-strength inverters could also be used to provide a dead time control range for tuning to a given application.

5.2 Optimization

Mentioned in previous sections, the optimization procedure given in [2] leaves room for several improvements and extensions outlined below.

5.2.1 Inductor-related dissipation

Inductor-related dissipation was not included in either the predicted efficiency plot 4.6 or the determination of the power stage size for the current implementation. Section 3.1.4 introduces these mechanisms. Since these mechanisms are most prominent at low modulation levels and typical input signals spend a majority of time at these low levels, ripple current and hysteresis dissipation must be included in a more complete analysis and optimization procedure.

5.2.2 Switching frequency

The optimization procedure from Chang, et al. assumed a static switching frequency which is no longer valid for a self-oscillating topology. Capacitive and short-circuit current, ripple current, and hysteresis dissipation mechanisms all depend on f_{sw}. Switching rate is a function of input amplitude in a roughly parabolic sense for the self-oscillating amplifier. This has the effect of weighting the transition-based dissipation mechanisms more heavily at low output levels, serving to decrease the slope of the efficiency increase as output power increases.

A better solution could be found by optimizing both W_p and f_{sw} since filter reactance dissipation is inversely proportional to f_{sw} while capacitive, short-circuit, and hysteresis dissipation are linearly related. Ripple current dissipation also decreases by the square of the inductance. It would perhaps be just as easy to increase the inductor size and keep f_{sw} low.

5.2.3 Typical input signals

Section 3.3.2 has already introduced the need to weight the efficiency or power loss versus modulation with the probability density of typical input signals. More work can be done in including this weighting within an updated optimization procedure.

Tractable design procedure

Finally, the purpose of optimization is to strike the best balance between competing parameters, namely IC area and efficiency. While it is certainly a valid academic exercise to generate a huge equation that yields the optimum output stage size only solvable through numerical methods (as in the equation in [2]), a goal should be to make the design of class D output stages easier and less trial and error.

One way to ease the design effort is to specify the output stage parametrically as done in section 3.2.2 by mapping physical sizes to design parameters like dead time and delay. A tool could be developed that takes a process parameter file (such as a MOSFET (H)SPICE model) and application dependent parameters and generates the optimum device sizes.

There is already an open-source tool that performs general N-dimensional optimization using the differential evolution algorithm named ASCO (for: A SPICE Circuit Optimizer) [19]. Its effectiveness has been demonstrated in [20] with the design of a three stage opamp and a class E amplifier. Being a general optimizer, it evaluates its cost function through simulation runs which can take a considerable amount of time for a complex design.

Ultimately, the goal would be to create a tool that takes process parameters and application information, calculates the optimum gate drivers and output devices, and generates an IC layout, similar to the digital synthesis tools already available. Verification of the "compiler" would use a tool such as ASCO to compare optimized

sizes. This way, the design of IC class D or, in general, switching power stages, would be easy, allowing design effort to shift to overall topology or other system design.

5.3 Topologies

Another route of inquiry is to analyze the current-art topologies, both clocked and self-oscillating, with respect to efficiency and implementation area. A similar survey of topologies focused on linearity in switching output stages, while only listing power dissipation mechanisms [15].

Chapter 6

Conclusions

A recent self-oscillating class D amplifier topology [1] was mapped into a standard CMOS technology. This amplifier requires no extra fabrication features beyond what is provided in a general digital IC. The simple self-oscillating topology allows the output transistors to dominate implementation area, unlike other proposed topologies.

Four amplifiers were fabricated on a single $1.5mm$ die in a $0.5\mu m$ process as a proof-of-concept demonstration. Testing showed reasonable linearity for the core amplifier, creating a solid base for simple loop gain enhancements. Efficiency measurements of the fabricated amplifier and test fixture revealed discrepencies at low output power levels from predicted efficiencies. Section 4.3.2 discusses possible causes for the differrences.

Optimization of the power stage and its drivers can yield improvements in both average efficiency and area, further reducing the total area required for inclusion of a high-performance amplifier on-chip. This allows the migration of single-chip class D amplifiers onto the same die as other system components, reducing printed circuit board size and system cost.

Besides the mapping of a new topology, improvements to a general power stage

optimization procedure were proposed. These form the beginning of a unified output stage design algorithm, possibly terminating in a "class D output stage compiler." Such a tool would make available an application-specific class D output stage block to any designer without requiring their knowledge of the inner workings.

Bibliography

[1] Putzeys, B. "Simple self-oscillating class D amplifier with full output filter control," presented at the AES 118th convention, Barcelona, Spain, 28-31 May 2005.

[2] Chang, J. S.; Tan, M.; Cheng Z.; Tong, Y. "Analysis and design of power efficient class D amplifier output stages," IEEE Trans. on Circuits and Systems-I, vol 47, pp. 897-902, 2000.

[3] White, D. J. "`pyspice.py`, a SPICE pre-processor," `http://www.whiteaudio.com/soft/pyspice.html`.

[4] Magrath, A. "Design and evaluation of a high performance class D headphone driver," presented at the AES 121st convention, San Francisco, CA, 5-8 Oct 2006.

[5] Temme, S.; Brunet, P. "A new method for measuring distortion using a multitone stimulus and non-coherence," presented at the AES 121st convention, San Francisco, CA, 5-8 Oct 2006.

[6] Piessens, T.; Steyaert, M. "Oscillator pulling and synchronisation issues in self-oscillating class D power amplifiers," Proceedings of the 29th European Solid-State Circuits Conference, 2003. ESSCIRC '03. 16-18 Sept. 2003. pp.529-532. 10.1109/ESSCIRC.2003.1257189

[7] Smith Jr., K.M.; Lai, Z.; Smedley, K.M. "A new PWM controller with one-cycle response," IEEE Transactions on, Power Electronics, Volume 14, Issue 1, Jan. 1999. pp.142-150. 10.1109/63.737602

[8] Hai, C.; Xiaobo, W. "A class D audio power amplifier with high-efficiency and low-distortion," Design Automation Conference, 2005. Proceedings of the ASP-DAC 2005. Asia and South Pacific , vol.2, no.pp. 815- 818 Vol. 2, 18-21 Jan. 2005

[9] Li, S.C.; Lin, V.C.-C.; Nandhasri, K.; Ngarmnil, J., "New high-efficiency 2.5 V/0.45 W RWDM class-D audio amplifier for portable consumer electronics," IEEE Transactions on Circuits and Systems I: Regular Papers, vol.52, no.9pp. 1767- 1774, Sept. 2005

[10] Anderskouv, N.; Nielsen, K.; Andersen, M.A.E. "High Fidelity Pulse Width Modulation Amplifiers based on Novel Double Loop Feedback Techniques," presented at the AES 100th convention, Copenhagen, Denmark, 11-14 May 1996.

[11] Neilsen, K.; Fredericksen, T. "Controlled self-oscillation modulator and power conversion system using such a modulator," U.S. Patent 6362702 B1, 26 March 2002.

[12] Frederiksen, T.; Bengtsson, H.; Nielsen, K. "A Novel Audio Power Amplifer Topology with High Efficiency and State-of-the-Art Performance," presented at the AES 109th convention, Los Angeles, CA, 22-25 Sept. 2000.

[13] Poulsen, S.; Andersen, M.A.E., "Simple PWM modulator topology with excellent dynamic behavior," Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04. , vol.1, no.pp. 486- 492 Vol.1, 2004

[14] van der Hulst, P; Veltman, A.; Groenenberg, R. "An asynchronous switching high-end power amplifier," presented at the AES 112th convention, Munich, Germany, 10-13 May 2002.

[15] Nielsen, K. "Linearity and Efficiency Performance of Switching Audio Power Amplifier Output Stages - A Fundamental Analysis," presented at the AES 105th convention, San Francisco, CA, 26-29 Sept. 1998.

[16] Rabaey, J.M.; Chandrakasan, A.; Nikolic, B. *Digital integrated circuits: a design perspective*, 2nd ed. 2003. Prentice Hall NJ.

[17] Mosely, I.D.; Mellor, P.H.; Bingham, C.M. "Effect of dead time on harmonic distortion in class-D audio power amplifiers," Electronic Letters. 10th June 1999. Vol. 35 No. 12.

[18] Soo-Hyoung Lee; Jae-Young Shin; Ho-Young Lee; Ho-Jin Park; Lund, K.L.; Nielsen, K.; Jae-Whui Kim, "A 2W, 92% efficiency and 0.01% THD+N class-D audio power amplifier for mobile applications, based on the novel SCOM architecture," Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004 , vol., no.pp. 291- 294, 3-6 Oct. 2004

[19] Ramos, J. "ASCO (A SPICE Circuit Optimizer),"
`http://asco.sourceforge.net/`

[20] Ramos, J. "CMOS Operational and RF Power Amplifiers for Mobile Communications." PhD thesis, K. U. Leuven, Belgium, March 2005.

[21] Audio Engineering Society, "AES48-2005: AES standard on interconnections - Grounding and EMG practices - Shields of connectors in audio equipment containing active circuitry." 2005

[22] Wolfson Microelectronics Inc, "Highly Integrated Stereo CODEC with Class D Speaker Drivers," WM8960 datasheet. 2006.

Appendix A

Symbols

Symbols used in power dissipation and optimization formulas.

Symbol	Meaning
a or α	PMOS/NMOS transistor width ratio (μ_n/μ_p)
C_{gso}	Gate to source overlap cap. (F/m)
C_{gdo}	Gate to drain overlap cap. (F/m)
C_{jp}	Junction cap. P-diffusion to N-well (F/m^2)
C_{jn}	Junction cap. N-diffusion to P-bulk (F/m^2)
C_{jsw}	Sidewall diffusion capacitance (F/m)
C_{ox}	Gate capacitance (F/m^2)
C_{pad}	Bonding pad capacitance (F)
f_{sw}	Switching frequency (Hz)
I_o	Maximum RMS load current (A)
L_1	Diffusion contact width (m)
L_2	Diffusion contact spacing (m)
L_3	Contact to channel spacing (m)
L_{DS}	Drain/source diffusion length (m)

R_{ctp}	P-diffusion contact resistance (Ω)
R_{ctn}	N-diffusion contact resistance (Ω)
R_{load}	Load impedance (Ω)
R_L	Inductor DC resistance (Ω)
R_{shp}	P-diffusion sheet resistance ($\Omega/\square$)
R_{shn}	N-diffusion sheet resistance ($\Omega/\square$)
T_{sum}	Effective total transistor width $\left(\sum_{i=0}^{N} t^{-i}\right)$
μ_n	Electron mobility ($cm^2/(Vs)$)
μ_p	Hole mobility ($cm^2/(Vs)$)
V_{dd}	Power supply voltage (V)
V_{th}	Threshold voltage (average) (V)
W_p	PMOS output transistor effective drawn width (m)